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Reck, Kasper; Richter, Jacob; Hansen, Ole; Thomsen, Erik Vilain

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PIEZORESISTIVE EFFECT IN TOP-DOWN FABRICATED SILICON NANOWIRES

K. Reck, J. Richter, O. Hansen and E.V. Thomsen
Technical University of Denmark, Kgs. Lyngby, Denmark

ABSTRACT

Encouraged by the results of He and Yang [1], we have designed and fabricated silicon test chips to investigate the piezoresistive properties of both crystalline and polycrystalline nanowires using a top-down approach, in order to comply with conventional fabrication techniques. The test chip consists of 5 silicon nanowires and a reference resistor, each with integrated contacts for electrical 4-point measurements. We show an increase in the piezoresistive effect of 633% compared to bulk silicon. Preliminary temperature measurements indicate a larger temperature dependence of silicon nanowires, compared to bulk silicon. An increase of up to 34% compared to bulk polysilicon is observed in polysilicon nanowires with decreasing dimensions.

1. INTRODUCTION

Silicon nanowires have received immense interest the past two decades. This is partly due to the general down-scaling of electronics and their capabilities as interconnects and partly due to fundamental changes in electrical, thermal and mechanical behavior. Recently, a giant piezoresistance of up to $3,550e-11 \text{ Pa}^{-1}$ has been found in self-assembled silicon nanowires [1]. This increase in the piezoresistive effect is of great importance in the field of highly sensitive devices, e.g. cantilever based sensing for biomedical applications [2].

Self-assembly of silicon nanowires is still a relatively new technology, not yet a part of standard industrial micro/nano fabrication, and has several limitations compared to the conventional top-down approach. These include the tendency of self-assembled nanowires to grow along specific crystal directions, and the difficulty of positioning the catalyst particle, an often serial and sometimes even manual process. Contrary to top-down fabrication, creating electrical contact, e.g. for 4-point measurements, is not trivial when using self-assembled nanowires.

One of the main reasons that top-down fabricated nanowires have not received the same interest as self-assembled nanowires is the difficulty of fabricating nanostructures consistently and efficiently. In order to obtain an increase in the piezoresistive effect, dimensions should, according to ref. [1], be less than 350 nm. This can be achieved by use of e-beam lithography (EBL), however with exceedingly increased difficulty as dimensions shrink. Also EBL is a slow and costly method, not suitable for mass production. To overcome these obstacles, larger nanowires can be thinned by self-limiting oxidation thinning as shown by ref. [3], e.g. from 100 nm to 20 nm, and EBL can be parallelized by use of nano imprint lithography (NIL). As NIL has a minimum feature size of less than 10 nm [4], and

a processing time in the order of minutes or seconds, it is a perfect tool for industrial scale nanowire fabrication.

2. DESIGN

The test chips are 4 cm long, 5.3 mm wide and 340 μm thick, each carrying 6 dielectrically isolated p-type piezoresistors, see Figure 1. The resistors are placed at the centre of the chip and directed along the chip length, such that bending the chip in a four-point bending fixture (4PB) applies a uniform and uniaxial stress in the resistors along the current direction. The 6 resistors have different widths of 50, 100, 150, 250 and 350 nm, and one 25 μm reference resistor. All the resistors are oriented along the [110]-direction, and they all have a length to width ratio of 20. This layout makes it possible to investigate how much the cross sectional dimensions effect the piezoresistive properties with one chip.

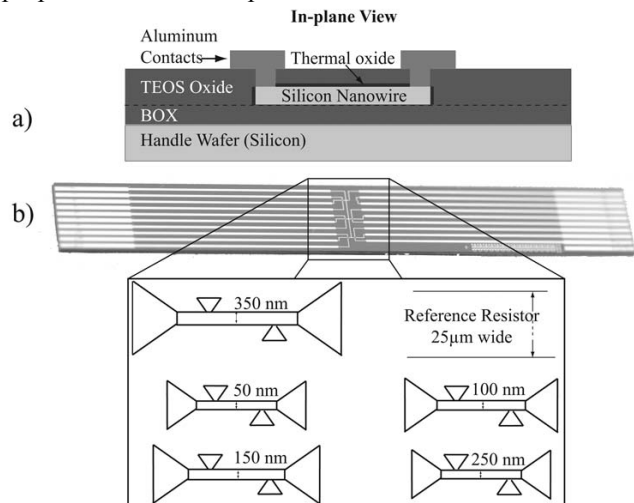


Figure 1 (a) The resistors are dielectrically isolated by oxide. (b) The test chip consists of 5 nanowires and a conventional sized reference resistor, all with a length to width ratio of 20. The illustration of the resistor configuration is not to scale.

Since the nanowires by nature have a small contact surface to any electrical contacts, the contact resistance can be comparable to the resistance of the nanowire itself. To avoid this, the design includes four contacts for four-point measurements integrated directly on each nanowire, see Figure 2.

As π_{44} is the largest piezocoefficient of p-type silicon, it is also the most interesting of the three piezocoefficients with respect to sensors. Applying a uniaxial stress along the [110] direction the effective piezocoefficient is

$$\pi_{eff} = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \approx \frac{1}{2}\pi_{44}, \quad (1)$$

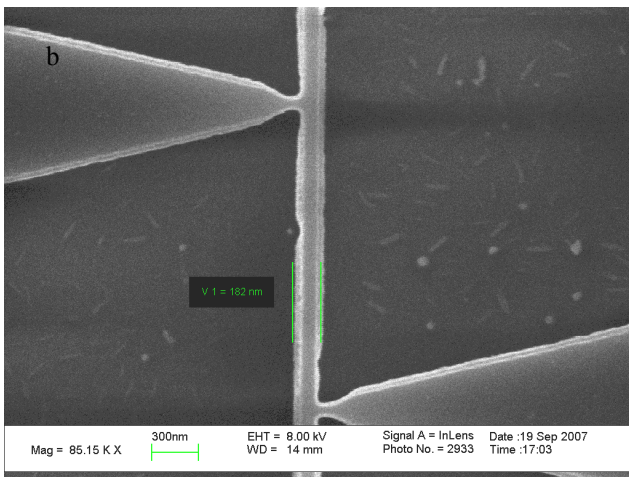
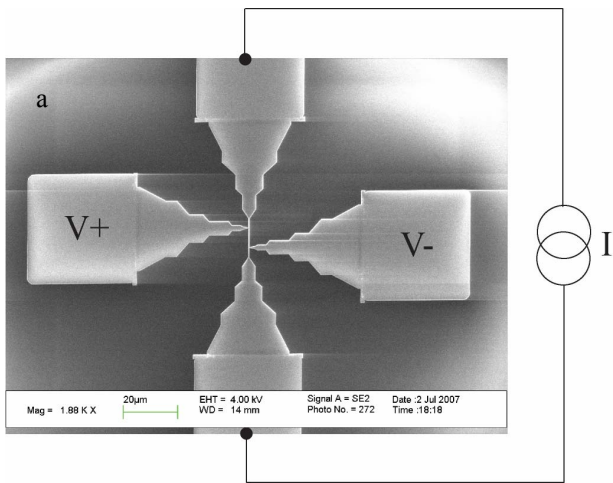


Figure 2 (a) A silicon nanowire etched in the 340 nm device layer of an SOI wafer by RIE. The four contacts are used for four-point resistance measurements, in which a constant current is applied and the resistance is calculated from the voltage drop along the resistor. (b) SEM image of a 182 nm wide and 300 nm thick silicon nanowire on 1000 nm silicon dioxide.

when taking into account that π_{44} is much larger than π_{11} and π_{12} , which is the case for bulk p-type silicon [7].

3. FABRICATION

The main fabrication steps are illustrated in Figure 3. An SOI wafer with a device layer of 340 nm of either crystalline or LPCVD polysilicon (deposited at 620 °C), on top of a 1000 nm buried oxide (BOX) is implanted with boron (Figure 3a). Test structures are defined in 60 nm e-beam evaporated gold on top of 10 nm titanium by UV-lithography liftoff on the device layer (Figure 3b). The nanowire structures are defined with a JEOL JBX9300FS e-beam writer in the positive resist ZEP520A at a dose of $250\mu\text{C}/\text{cm}^2$, followed by a second gold/titanium liftoff (Figure 3c). These UVL and EBL steps can be exchanged by a single NIL to minimize fabrication time. The gold is then used as mask to etch the device layer in a highly anisotropic reactive ion etch (Figure 3d), and subsequently

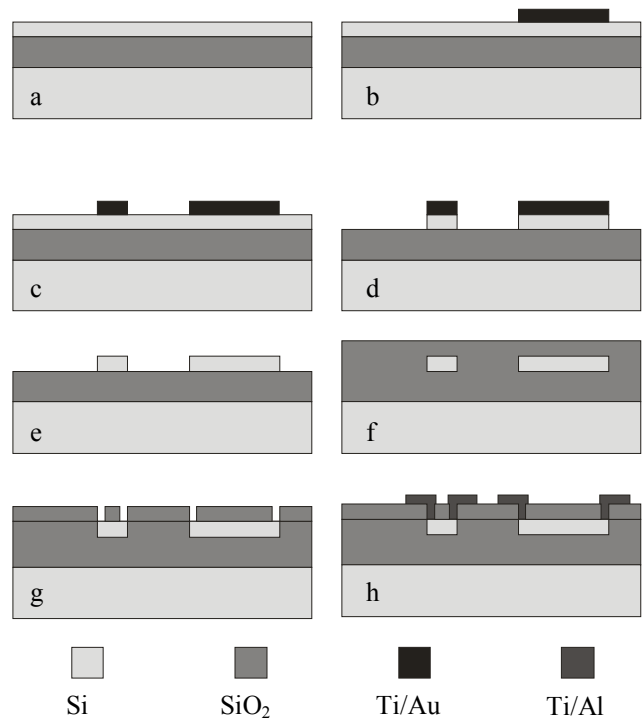


Figure 3 An SOI wafer or polysilicon on top of thermal oxide is implanted with boron (a). Nanowires and test structures are transferred to a gold mask by liftoff using UVL (b) and EBL (c). Reactive ion etching defines the structures in the device layer (d). The mask is removed (e) and a thin dry oxide and a TEOS are applied (f). Contact holes are opened in the oxide (g). After implantation of contacts and annealing, aluminum wires for electrical contact are made by liftoff (h).

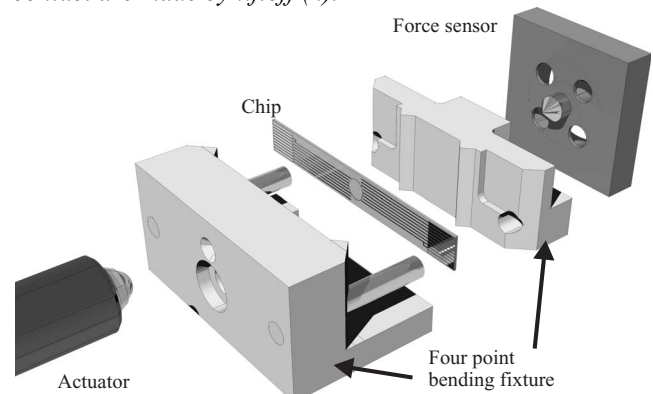


Figure 4 The test chip is stressed using a 4PB fixture. The force is applied by a microstep actuator and measured with a conventional force sensor.

removed by potassium iodide. The titanium is removed by an ammonium hydroxide/hydrogen peroxide solution (Figure 3e). A thin dry oxide is applied for passivation of the nanowire, followed by 140 nm TEOS (Figure 3f). After opening contact holes in the oxide, and implantation of the contacts (Figure 3g), the wafers are annealed at 1000 °C for 30 min. Aluminum wires are deposited by e-beam evaporation (Figure 3h) for electrical contact. A SEM image of a finished silicon nanowire is shown in figure 2b.

4. SETUP

To measure the stress dependence of the resistance of the nanowires, a fully automated 4PB fixture setup was used, see Figure 4. The test chip is placed between the two pair of blades, and force is applied using a microstep actuator. The resulting force on the 4PB fixture is measured using a conventional force sensor. The stress in the test chip, σ , is calculated from the measured force, F , assuming the test chip behaves as a beam subjected to pure bending, as

$$\sigma = -\frac{6 \cdot F \cdot a \cdot z}{w \cdot t^3},$$

where a is the distance between inner and outer blades, z is the distance to the neutral plane (i.e. half the thickness), w is the width and t is the thickness [5]. The bending fixture is located in an aluminum box with built-in resistive heating. The DC current is applied to the nanowires using a HP4145A parameter analyzer, and the resulting voltage drop is measured with a Keithley 2182A nanovoltmeter. Electrical contact to the test chip is made using zero insertion force flat flexible cable (FFC) connectors, attached directly to each end of the test chip.

Due to the small size, the nanowires have resistances of up to several M Ω , depending on the doping level. As the piezocoefficients of bulk silicon is known to be temperature dependent, especially at low doping levels, it is critical to avoid Joule heating during measurements. Finite element calculations of the thermo-electric behavior have been made to estimate an interval of acceptable currents for each nanowire. The model includes a decrease in the thermal conductivity of silicon at the nanoscale as discussed by [6]. It is found that to avoid temperature increases of more than 0.05 $^{\circ}\text{C}$, the current should be in the order of 10^{-12} to 10^{-9} A.

Due to the low-level nature of the measurements, thermal noise and thermo-electric voltages are minimized by the use of low-pass filters and the current reversal method (also known as delta measurement).

5. RESULTS

The absolute relative change in resistance, as function of applied compressive stress, is shown in Figure 5 for four different sized nanowire piezoresistors and a reference resistor. The slope of the linear least squares fit to each data series is increasing with decreasing dimensions; hence the effective piezocoefficient is increased. Due to the large piezoresistive effect of the $140 \times 200 \text{ nm}^2$ nanowire it is plotted on both the left and right hand side scales, while the remaining piezoresistors are plotted only on the left hand side scale.

Using Equation (1), the shear piezocoefficient π_{44} is estimated and the results are listed in Table 1. The piezocoefficient of the $140 \times 200 \text{ nm}^2$ nanowire show an increase of approximately 633% compared to the reference resistor. The gauge factor for this wire is 1547. While the shear piezocoefficient of the reference resistor is 10% smaller than the values obtained by Smith [7], which is due to the lower resistivity of the reference resistor, it is 9% larger than the results of Tufte and Steltzer in ref. [8] at an

Table 1 The obtained values of π_{44} show an increase of up to 7.3 times the piezocoefficient of the reference resistor and of the values obtained by Smith. This piezocoefficient is equivalent to a gauge factor of 1547.

Resistor	ρ [$\Omega \cdot \text{cm}$]	π_{44} [10^{-11} Pa]	$\pi_{44}/\pi_{44,\text{ref}}$
Reference	0.02	124	-
$480 \times 340 \text{ nm}^2$	0.02	140	1.1
$280 \times 340 \text{ nm}^2$	0.02	165	1.3
$140 \times 340 \text{ nm}^2$	0.02	212	1.7
$140 \times 200 \text{ nm}^2$	0.4	910	7.3
Smith [7]	7.8	138.1	1.1
Tufte et al. [8]	0.02	113	0.9

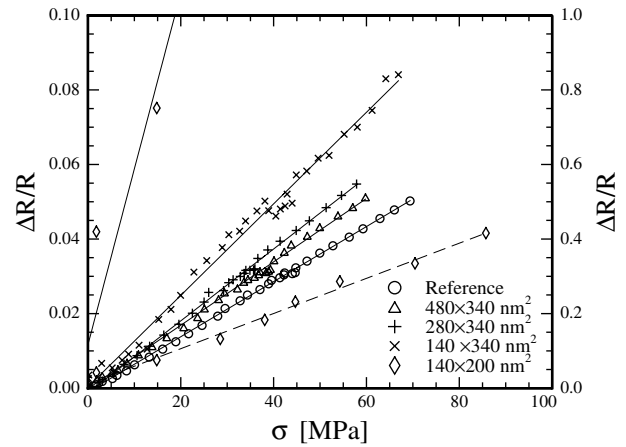


Figure 5 The absolute relative change in resistance as function of compressive stress for four crystalline nanowires, compared to a conventional sized reference resistor. The shear piezocoefficient is approximated from Equation 1 as two times the slope. Note that all piezoresistors are measured on the left hand side scale, except the $140 \times 200 \text{ nm}^2$ nanowire which has been plotted on both the left (solid) and right (dashed) hand side scales.

approximately equivalent resistivity.

The temperature dependence of the $140 \times 340 \text{ nm}^2$ nanowire is shown in Figure 6, together with the reference resistor, for 25 to 80 $^{\circ}\text{C}$. The temperature dependence of the reference resistor is marginally decreasing, as expected for highly doped silicon. However, the nanowire shows a large decrease in the effective piezocoefficient as the temperature is increased. At 80 $^{\circ}\text{C}$ π_{44} has decreased by 35% compared to its value at 25 $^{\circ}\text{C}$.

The effective piezocoefficients for five polysilicon nanowires and a reference resistor, all on the same chip, are shown in figure 7. With an effective piezocoefficient of approximately $20 \text{e-}11 \text{ Pa}^{-1}$, the polysilicon nanowires are much less piezoresistive than the crystalline silicon nanowires. These piezocoefficients equal a gauge factor of approximately 32, consistent with ref. [9]. Comparing the smallest and largest nanowire there is, however, an increase in the effective longitudinal piezocoefficient of up to 34%, when decreasing dimensions.

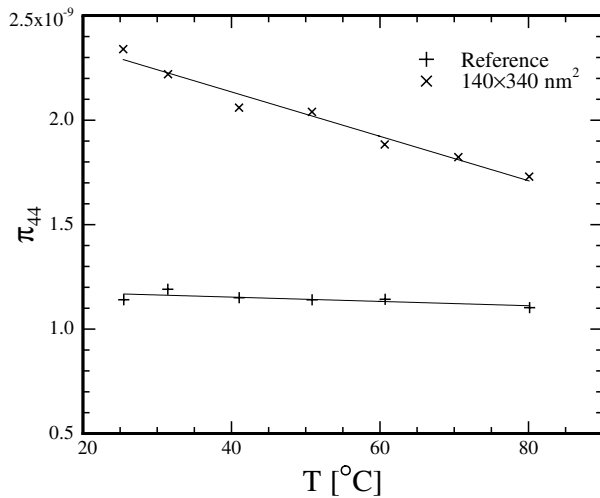


Figure 6 The π_{44} piezocoefficient for a $140 \times 340 \text{ nm}^2$ nanowire is decreased by approximately 35% as the temperature is increased from 25 to 80 °C. The linear fit has a slope of $-1.05 \times 10^{-11} \text{ Pa}^{-1}/^\circ\text{C}$. The reference resistor is less temperature dependent, which is expected for high doped piezoresistors.

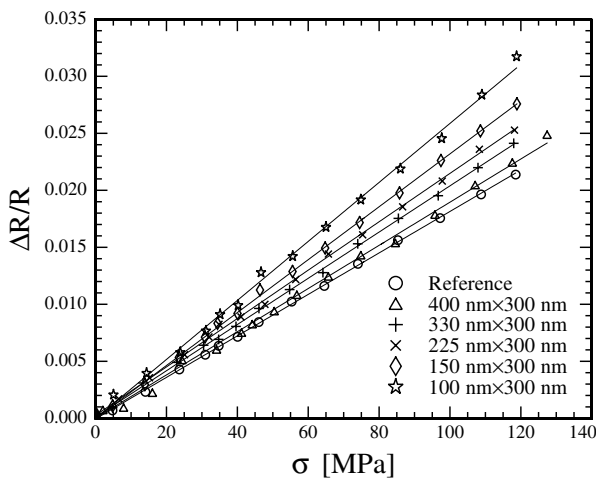


Figure 7 The absolute relative change in resistance as function of compressive stress for five polysilicon nanowires. The effective piezocoefficient, i.e. the slope of the linear fits, is increased by approximately 34% from $400 \times 300 \text{ nm}^2$ to $150 \times 300 \text{ nm}^2$ in polysilicon nanowires. This increase is not comparable to the much larger increase seen in crystalline silicon.

6. CONCLUSION

Polysilicon and crystalline silicon nanowires have been fabricated by EBL. An increase in the piezoresistive effect has been observed in nanowires as large as $480 \times 340 \text{ nm}^2$. The largest measured increase in the piezoresistive effect was of more than 7 times that of bulk silicon in a top-down fabricated crystalline silicon nanowire with dimensions of $140 \times 200 \text{ nm}^2$. The resistance change was found to be linear under compressive stress of up to 80 MPa.

Temperature measurements from 25 to 80 °C indicate an increase in the temperature sensitivity of silicon

nanowires compared to bulk silicon. Using a linear fit, the change in effective piezocoefficient with temperature was found to $-1.05 \times 10^{-11} \text{ Pa}^{-1}/^\circ\text{C}$. A linear fit for the reference resistor yields a temperature dependence of $-1.03 \times 10^{-12} \text{ Pa}^{-1}/^\circ\text{C}$, an order of magnitude less than for the nanowire.

An increase in the piezoresistive effect was also found in polysilicon nanowires of up to 34%. While this is not comparable to the large increase found in crystalline silicon, it is still a considerable improvement, and may help in the future analysis of the increased piezoresistive effect in silicon nanowires. The absolute value of the effective piezocoefficient is approximately four-five times smaller than p-type crystalline silicon. The piezoresistivity of polysilicon is, however, highly dependent on the fabrication process, and a larger absolute piezoresistive effect seems obtainable by process optimization.

The measurements show that decreasing the cross-sectional dimensions causes a large increase in the sensitivity of piezoresistors. This enables fabrication of high sensitivity devices where fabrication complies with conventional microfabrication techniques. Implementing NIL in the fabrication process, enables mass production of highly sensitive piezoresistive nanowire sensors, with several applications e.g. in biomedicine.

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