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A Versatile Discrete-Time Approach for Modeling Switch-Mode Controllers

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Abstract—**This paper presents a universal method for modeling the frequency response of comparators in switch-mode controllers. As the main non-linearity in most switch-mode controllers, understanding the comparator is the key to understanding the system. Based on discrete-time modeling, the proposed method is demonstrated to allow very precise predictions of comparator frequency response in a variety of control schemes. In the presented work, the modeling method is exemplified for the standard PWM and two different self-oscillating (a.k.a. sliding mode) control schemes. The proposed method is believed by the authors to be the first method that is able to handle these fundamentally different control schemes within a single modeling framework. Experimentally measured output impedance and comparator magnitude responses are compared to the model results. Great accuracy is achieved from DC to frequencies far beyond the switching frequency.**

I. INTRODUCTION

Accurate system modeling is essential in the design, optimization and verification of switch-mode control loops and has been studied intensely for many decades. This work is motivated by the need for better models for high-performance switch-mode control systems, as required in e.g. class-D audio power amplifiers or envelope tracking power supplies for RF power amplifiers. Such systems need to accurately reproduce reference waveforms with relatively high frequencies and thus need a very high loop-bandwidth relative to the switching frequency. Moreover, these switching circuits may get subjected to frequency components in far excess of their switching rate: Audio amplifiers may receive high frequency noise components from over-sampled digital to analog converters and a power supply is subjected to very high frequency load current components, e.g. from a CPU core. Power conversion systems with multiple power converters operating at different frequencies prescribe that converters may be subjected to supply ripple and harmonics at frequencies far above their switching frequency.

Consequently, accurate control system modeling from DC to far beyond the switching rate is important.

Currently a wide array of models and methods exist for use with different types of switch-mode control loops. A simple averaging-based text book example [1] is the continuous-time, fixed-gain model of the standard pulse width modulator (PWM). Discrete-time models based on cycle-by-cycle averaging are capable of better high-frequency accuracy [2], but are generally not accurate above half the switching frequency. Self-oscillating (a.k.a.

sliding mode) control loops are arguably the most difficult systems to model due to the merging of oscillator, control system and modulator functions. A common approach is the "sliding mode" approximation [3] (error/carrier/sliding signal is always zero), which can work very well in some cases [4], but not in others [5]. More accurate, continuous-time approaches use describing function techniques [5], [6], but are only accurate below the switching frequency. While other prior art [8] also accounts for aliasing effects, DC-to-above-f_{sw} accuracy has yet to be demonstrated.

A discrete-time modeling framework was proposed in [7] in the context of switch-mode audio power amplifiers. This model provides a linearized small-signal model accurate at any frequency and it elegantly accounts for frequency aliasing/imaging. The essence of the model is that the comparator acts as a sampler with a frequency-independent finite gain being inversely proportional to the slew-rate of the carrier waveform on its input, in accordance with the textbook model [1]. This finite and constant gain property is seemingly contradicted by other modeling work [9] yielding a theoretically infinite comparator DC gain for the simple 1st-order hysteretic control (sliding mode assumption).

As the present paper will demonstrate, the reason for this discrepancy is the constant-gain behavior only applies in the discrete-time domain. A gain-phase analyzer however, treats all signals as being in continuous-time and performs a narrow-band analysis centered on the stimulus frequency. The resulting narrow-band or continuous-time equivalent comparator gain consequently becomes frequency dependent due to the mixing of continuous-time and discrete time signals.

The presented work aims at deriving the single frequency, narrow-band in/out transfer function of the comparator (ideally the only non-linear control loop component) using the framework from [7]. Using the derived comparator frequency response $K_s(f)$, the single frequency stimulus small-signal response of the entire system can be found using conventional continuous-time (s-domain) analysis techniques without entering the z-domain.

A. Definitions

The following definitions are used throughout the paper, where f is the stimulus frequency and f_{sw} is the switching frequency:

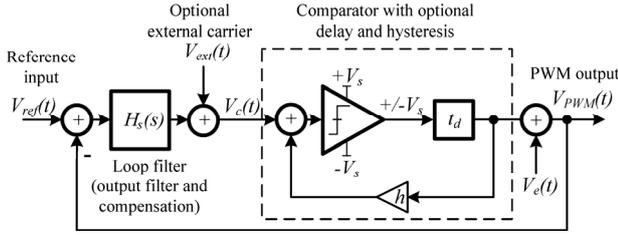$$s = j2\pi f \quad T_s = \frac{1}{2f_{sw}} \quad z = e^{sT_s}$$

Figure 1. Generic model of a switch-mode control loop [7]

II. DISCRETE-TIME LOOP MODEL

The modeling approach proposed in this paper is based on the generic switch-mode control loop model from [7], as shown in Fig. 1. The physical comparator in the control loop is combined with the switching power stage, time delay t_d and positive feedback h (for providing hysteresis) to form the comparator block shown. The output filter (e.g. an LC filter), compensation network (e.g. a PID) and phase-shift network (as required for a phase-shift self-oscillating controller) are lumped together in the loop filter $H_s(s)$ which represents the combined s-domain transfer function from the comparator (which notionally includes the switching power stage) output back to the comparator input. An optional carrier signal $V_{ext}(t)$ is added to the comparator input when the system is clocked (e.g. using triangle waveform in a conventional clocked PWM control loop).

A. Model Scope

The modeling framework to be presented is applicable when the system is in a periodic steady-state condition with a 50% duty cycle PWM signal. The model then describes the system dynamics for infinitesimal perturbations around the periodic steady-state. This gives thus a small-signal AC model that is valid at any frequency but only for very low amplitude stimulus signals. The model will thus not reflect large-signal behavior. A large-signal model only accurate near DC was presented in [13].

B. Sampling Comparator Model

At steady state with no stimulus applied on the input V_{ref}, the comparator input signal $V_c(t)$ is a periodic carrier waveform composed of the optional external carrier added to the ripple signal coming from the feedback path via the loop filter $H(s)$. The zero-crossings of $V_c(t)$ aligns with the 50% duty cycle transitions of the comparator PWM signal. If we superimpose a small-amplitude perturbation signal $V_p(t)$ on top of $V_c(t)$ we will perturb the PWM transition time instants by a small amount. We further assume that the perturbation is so small that it does not change the carrier signal $V_c(t)$. If we subtract the PWM waveform of an un-perturbed system, we get a pulse train of narrow pulses around each PWM edge. These narrow error pulses have either $+2V_s$ or $-2V_s$ in amplitude depending on the polarity of the perturbation signal and the slope polarity of the carrier $V_c(t)$. As shown in Fig. 2, for small perturbations, the area of each perturbation error pulse can be approximated by:

$$A_n \cong 2V_s \cdot \frac{V_p(n \cdot T)}{|\dot{V}_{c0}|} \tag{1}$$

This means that the comparator samples the perturbation waveform at every zero crossing and
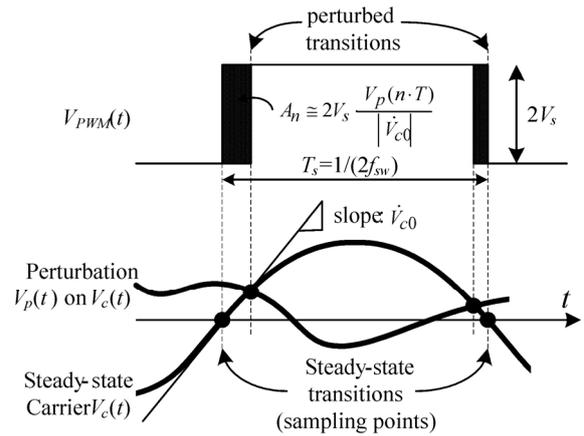

Figure 2. Gain computation concept for sampling comparator model.

produces a narrow output pulse (approximating a Dirac delta pulse) having an area proportional to the sampled amplitude. If we assume that the zero-crossings of the steady-state carrier $V_c(t)$ are symmetrical (same absolute value of the slope) then the comparator samples uniformly at a frequency of $2f_{sw}$. The comparator also acts as a gain K_z which is the proportionality between the sampled amplitude and the average pulse area over one sampling period:

$$K_z = \frac{A_n}{V_p(nT_s) \cdot T_s} = \frac{2V_s}{|\dot{V}_{c0}|T_s} = \frac{4V_s f_{sw}}{|\dot{V}_{c0}|} \tag{2}$$

Note that this gain corresponds to the classical model used for pulse-width modulators [1].

As known from digital signal processing theory, the sampling process gives rise to frequency aliasing and imaging. This means that the sampler does not tell the difference between frequency components that deviate by a multiple of the sampling frequency – also known as frequency aliasing. For example, a signal near the sampling frequency is treated the same way as a close-to-DC signal. The sampler also produces identical frequency images replicated at every multiple of the sampling frequency (called frequency images). This aliasing /imaging behavior may for example shift high-frequency circuit noise into the audible band of a switching amplifier. Another example is harmonic distortion due to aliasing of high-frequency image components generated by the Pulse-Width Modulation (PWM) [13].

C. Closing the Loop

The Dirac delta pulses of the comparator propagate back via the loop filter and produce a waveform superimposed on the carrier. This feedback waveform is then sampled again by the comparator and we have a closed-loop system around a sampler. It is first noted that the comparator input (perturbation) waveform is ignored at all other time instants but the sampling time points. This means again that we can replace the loop filter $H_s(s)$ with a suitable discrete-time domain (z-domain) filter $H_z(z)$ and achieve a loop fully in discrete-time as shown in Fig. 3.

This z-domain equivalent of $H_s(s)$ has the property that its impulse response matches exactly with the impulse response of its s-domain counter-part at the sampling time points. This transformation from s- to z-domain is known as the Impulse Invariance Method [11] and is obtained by performing a partial fraction expansion and mapping the
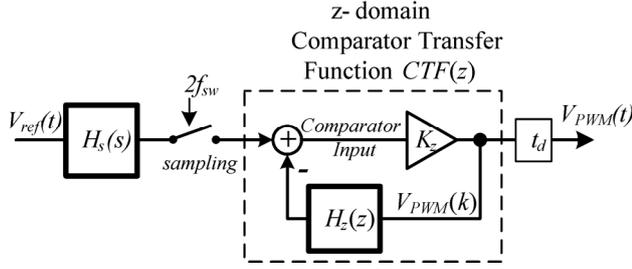
Figure 3. The comparator transfer function, $CTF(z)$

s-domain poles and zeros to the z-plane by using the transformation $z = \exp(s/(2f_{sw}))$ and scaling down the gain by the sampling rate. Note that the comparator delay t_d has to be included in the s-domain before transforming to the z-domain loop transfer function $H_z(z)$, e.g. by using a Padé approximation.

Once the comparator has made a transition, the feedback path cannot can not change the timing of the current transition but only affect the timing of the following transition. In other words, the current sampled value will first affect the comparator in the next sampling time. Consequently, this causality constraint forces the $H_z(z)$ impulse response to zero at time zero. Practically, this can be enforced in the model by taking the impulse invariance transform $\hat{H}_z(z)$ and subtracting the impulse response at time-lag zero $\hat{h}_z(k = 0)$:

$$H_z(z) = \hat{H}_z(z) - \hat{h}_z(k = 0) \tag{3}$$

The impulse response for a z-transfer function at time-lag zero can be found by normalizing the transfer function so that the highest order term in the denominator z-polynomial is unity. In this case, the time-lag zero response is equal to the numerator z-term with order equal to the denominator order.

For example, an s-domain integrator:

$$H_s(s) = \frac{1}{\tau \cdot s} \tag{4}$$

The pole at $s = 0$ is mapped to $z = 1$ which leads to the z-domain integrator with no delay (and scaling by $2f_{sw}$). By eliminating the impulse response at time zero by subtraction we then get a z-domain integrator with one sample delay:

$$H_z(z) = \frac{z^{-1}}{2\tau \cdot f_{sw}\left(1 - z^{-1}\right)} \tag{5}$$

Note that $H_z(z)$ is invariant to any pure delay added in the s-domain being less than one sample interval. Such a small delay just shifts the $H_s(s)$ impulse response (which is a step function) in time and results in the same discrete-time sequence when sampled. This delay-invariance only applies to a pure integrator.

The 2nd-order ($1/s^2$) integrator has an impulse response being a linear ramp starting at zero amplitude at time zero. Consequently, the Impulse Invariant transform obeys the causality constraint with no further correction. The resulting z-domain function becomes a double integrator with just one sample delay.

Note that the described s to z transformation is linear meaning that for a sum of s-functions we can transform each term individually and sum in the z-domain. For example, a loop filter may be a linear combination of a 1st- and a 2nd-order integrator. However, the transform of a
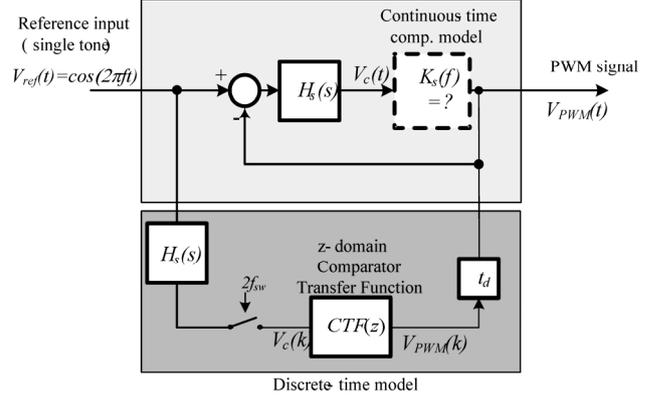

Figure 4. Using $CTF(z)$ for finding the continuous-time comparator frequency response $K_s(f)$.

product is not in general the same as the products of the transform of the multiplicands.

D. Comparator Hysteresis

A consequence of the feedback causality constraint mentioned above is that comparator hysteresis does not affect $H_z(z)$ since the hysteresis can be modeled as a positive feedback path (with gain h, see Fig. 1) that only shows up in the impulse response at time-lag zero and is thus removed. Moreover, the hysteresis does not change the slope of the carrier signal $V_c(t)$ since the positive feedback only adds a square wave (50% duty cycle) with zero slope at the sampling instants. Consequently, the comparator gain is unaffected so hysteresis does not factor in to the closed-loop z-domain transfer function either. The only effect of adding hysteresis is that the switching/sampling/oscillation frequency is changed when the loop is self-oscillating.

E. The Comparator Transfer Function CTF(z)

We now have a feedback loop that is described fully in discrete-time (z-domain) consisting of loop filter $H_z(z)$, comparator and gain K_z. However, external input signals (such as $V_{ref}(t)$) need in general to be treated as being in continuous-time until they get sampled by the comparator and injected into the z-domain loop at the equivalent z-domain comparator input node. Consequently, a closed-loop model accepting continuous-time input is shown in Fig. 3. The loop dynamics are governed by the z-domain Comparator-Transfer-Function $CTF(z)$:

$$CTF(z) = \frac{K_z}{1 + K_z H_z(z)} \tag{6}$$

Note that the z-domain part needs to be treated as a "black-box" that we only can be affected by adding sampled signals via the comparator sampling process. The z-domain part also fully accounts for the feedback path.

F. Modelling Continuous-time Input

The reference signal $V_{ref}(t)$ will thus first be filtered by $H_s(s)$ – in continuous-time – prior to being sampled and subjected to $CTF(z)$ and then delayed by t_d. This gives the following input output transfer function:

$$G_{ref-out}(s) = \exp(-s \cdot t_d) \cdot H_s(s) \cdot CTF(z) \tag{7}$$

This transfer function mixes s- and z-domain and needs to be interpreted carefully. It is well-known that a continuous-time single-frequency sinusoidal input to an s-domain filter such as $H_s(s)$ gives a steady-state response
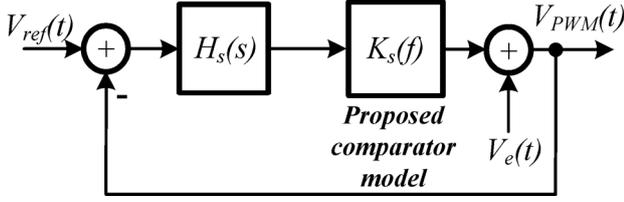
Figure 5. Versatile system model with $K_s(f)$

being a sinusoidal with an amplitude and phase given by the s-domain transfer function. When this sinusoid is sampled we get a frequency component of exact same frequency, amplitude and phase plus an infinity of spectral images (with same amplitude/phase) shifted by any multiple of the sampling frequency. The z-domain $CTF(z)$ describes then how the amplitude and phase is modified by the z-domain loop which has cyclical transfer function being periodic with $2f_{sw}$, i.e. the sampling frequency. When the z-domain loop output signal is interpreted as a "real-world" continuous-time PWM signal we have a periodic spectrum with a component at the original system input frequency and at any frequency image. If we observe the PWM signal with a narrow-band filter centered on the stimulus frequency then the stated mixed-domain transfer function accurately describes the steady-state amplitude/phase change causes by the system. This is in fact true for any frequency even far beyond the switching rate. Such a narrow-band measurement is indeed what the popular gain-phase analyzer performs.

III. CONTINUOUS-TIME COMPARATOR MODEL

This section derives the theoretical continuous-time transfer function $K_s(f)$ of the comparator corresponding to what a gain-phase analyzer will measure. The approach is that we apply a continuous-time single-frequency stimulus on $V_{ref}(t)$ and use the modeling frame-work presented to calculate the single-frequency response at both the comparator output (PWM node) and the comparator input. This procedure is shown in Fig. 4. The response at the output PWM node is directly given by (7). However, the comparator input has to be constructed as shown in Fig. 4 as the difference between $V_{ref}(t)$ and $V_{PWM}(t)$ being filtered by the loop filter $H_s(s)$. The resulting transfer function from V_{ref} to the comparator input is given by:

$$G_{ref-Cin}(s) = H_s(s)[1 - \exp(-s \cdot t_d) \cdot H_s(s) \cdot CTF(z)]$$ (8)

The comparator transfer function $K_s(f)$ is then given by the ratio of (7) and (8):

$$K_s(f) = \frac{\exp(-s \cdot t_d) \cdot H_s(s) \cdot CTF(z)}{H_s(s)[1 - \exp(-s \cdot t_d) \cdot H_s(s) \cdot CTF(z)]}$$
$$= \frac{K_z \cdot \exp(-s \cdot t_d)}{1 + K_z H_z(z) - K_z \cdot \exp(-s \cdot t_d) \cdot H_s(s)}$$ (9)
$$= \frac{K_z \cdot \exp(-s \cdot t_d)}{1 + K_z (H_z(z) - \exp(-s \cdot t_d) \cdot H_s(s))}$$

By using the derived comparator transfer function $K_s(f)$ above, the loop can be modeled purely in the s-domain in the sense that the model accurately yields the single frequency in/out response. This property is a simple consequence of the fact that $K_s(s)$ is fitted to match the results obtained by the discrete-time model. However, such s-domain model does not account for the frequency images produced by the sampling (that are ignored by a narrow-band gain-phase analyzer).

When examining (9) we note first that if $H_s(s)$ plus delay-term is equal to its z-domain counter-part $H_z(z)$ at any frequency then the $K_s(f)$ would be frequency-independent and equal to the sampling gain K_z with the delay-term. The z-domain $H_z(z)$ can be viewed as $H_s(s)$ plus the delay-term being sampled. The sampling aliases the high-frequency response of the s-domain function and produces a periodic z-domain function. For example: a near infinite low-frequency gain of $H_s(s)$ results in near infinite gain peaks at every even multiple of f_{sw} in the z-domain counterpart. As seen from (9) this result in a near zero comparator gain $K_s(f)$ which can be explained by discrete-time loop treating a single frequency component near an even multiple of f_{sw} as a near DC component which gets suppressed by the high low-frequency s-domain loop-gain.

Conversely, the comparator gain $K_s(f)$ may become infinite at some frequencies when the denominator of (9) becomes zero which occurs when the difference between the z- and s-domain transfer functions (i.e. the aliasing error) is equal to $1/K_z$.

A. Closed-loop Continuous-time Single-frequency Response

We can now replace the comparator block in Fig. 1 (comparator, delay and hysteresis) with $K_s(f)$ and obtain a system model (shown in Fig. 5) entirely in the s-domain which can be analyzed with standard methods. This s-domain model is accurate for a single-frequency narrow-band analysis but does as previously stated not account for frequency images due to the sampling.

For example, we can calculate the closed-loop response to an error-signal injected just prior to the feedback point on the PWM output node ($V_e(t)$ in Fig. 1 and Fig. 5) to the output. This error-suppression transfer function $ETF(s)$ (a.k.a. the sensitivity function) is given by:

$$ETF(s) = \frac{1}{1 + K_s(s) \cdot H_s(s)}$$ (10)

Note that this small-signal transfer function is valid at any frequency even beyond the switching rate.

For example, a current injected into the system output terminals causes some error voltage due to the open-loop output impedance (power stage and LC filter) which can be modeled as an error voltage $V_e(t)$. The control loop compensates by adjusting the power stage duty cycle in order to reduce the error voltage. Consequently, $ETF(s)$ represents the ratio by which feedback changes the open-loop output impedance.

IV. THE 1ST-ORDER INTEGRATOR LOOP

We will analyze the simple 1-order loop with a pure integrator loop filter with integration time-constant τ according to (4) and (5). Note that $H_z(z)$ does not depend on the comparator delay t_d (if less than one sample) or the hysteresis h.

We add an external triangular carrier $V_{ext}(t)$ with amplitude V_t. The slope of the carrier $V_c(t)$ just prior to the transitions is the sum of the triangle wave slope and the slope of the triangular feedback ripple. This leads to the following expression for the comparator sampling gain:

$$K_z = \frac{4 f_{sw} V_s}{4 f_{sw} V_t + \dfrac{V_s}{\tau}}$$ (11)
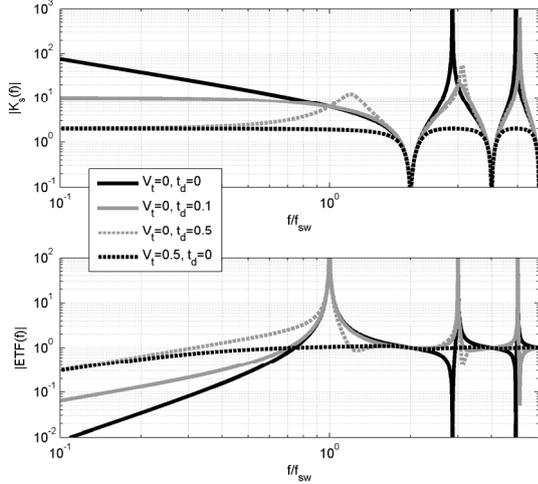
Figure 6. Calculated $K_s(f)$ and $ETF(f)$ for different loop configurations with an integrator loop filter.

Note that the comparator sampling gain K_z is reduced by the presence of feedback ripple. This means that K_z with the loop closed is less than traditionally assumed [1]:

$$K_{z[1]} = \frac{V_s}{V_t} \qquad (12)$$

By finding the zero-frequency limit value of the rather complex expression for K_s (9) we can after some calculation find the continuous-time DC comparator gain:

$$K_{s,0} = \frac{V_s}{Vt + V_s \cdot \dfrac{t_d}{\tau}} \qquad (13)$$

We note that for zero delay t_d, the DC gain is the ratio between the supply voltage and the triangle amplitude which is in perfect agreement with classical theory. When the triangle is removed, the loop will self-oscillate when a suitable hysteresis h is applied. For zero delay, it is noted that the DC gain is infinite which is in perfect agreement with sliding mode theory [3]. This can be visualized by comparator input waveform that will ramp linearly between the symmetrical hysteresis-bands which gives a zero input average for any output duty cycle and thus an infinite delay [9]. However, introducing a non-zero delay, the hysteresis-bands are exceeded giving a non-zero input average voltage and thus a finite gain as reflected in (13) [6], [9]. Notice that the delay also reduces the DC gain when using a triangular carrier contrary to classical theory [1].

For the self-oscillating case with hysteresis, the carrier slope is given by:

$$\left| \dot{V}_{c0} \right| = \frac{V_s}{\tau} \qquad (14)$$

This means that the hysteretic comparator DC gain can be written as:

$$K_{s,0,HC} = \frac{V_s}{\left| \dot{V}_{c0} \right| \cdot t_d} \qquad (15)$$

which is in perfect agreement with the expression found in [9].

The continuous-time comparator gain $|K_s|$ is plotted versus frequency in Fig. for 4 different configurations all using an integrator loop with $\tau=1$, $V_s=1$, $f_{sw}=1$. It is noted that all configurations have notches at even harmonics of f_{sw} reflecting that the z-domain loop filter has infinite gain here due to the frequency aliasing. The self-oscillating delay-free loop has a comparator gain that asymptotically at low frequencies behaves like an integrator in accordance with [9]. The integrator-like behavior combined with a finite DC gain due to a small delay lead to a simple 1-pole approximation to $K_s(f)$ in [9].

Note that all self-oscillating loops have a comparator gain equal to 2π at the switching frequency. This gives a total loop gain of unity (and -180 degree phase) when the integrator transfer function is included which is in agreement with the oscillation (e.g. the so-called Barkhausen criteria for oscillation). This is contrary to [12] that assumes a -6dB loop gain at f_{sw} which will not cause the desired oscillation. The underlying z-domain model always has a pole at $z = -1$ that accounts for the oscillation.

At frequencies just below odd harmonics of f_{sw} the self-oscillating loops have very high gain peaks, actually infinite gain peaks for the zero-delay hysteretic loop. These peaks give a very high error suppression at the peak frequencies which can be seen on the Error Transfer Function $ETF(s)$ plot. This means that the control loop can suppress errors at certain frequencies far beyond the switching rate. It is also noted that the hysteretic self-oscillating loop has far better error suppression compared to the triangular-carrier PWM loop at low frequencies due to the integrator-like behavior of the self-oscillating comparator. For zero comparator delay the errors-suppression of the self-oscillating loop exceeds the suppression of the triangle PWM loop by about 2 orders of magnitude at 5% of the switching rate (e.g. at the upper audio bandwidth for a 400kHz switching amplifier). Note here that $V_t=0.5$ is the lowest triangle amplitude (thereby the highest loop gain) that can be used without ripple instability at full modulation. However, the self-oscillating loops are extremely sensitive around odd-harmonics of the switching rate where $ETF(s)$ has high (infinite) gain.

V. EXPERIMENTAL RESULTS

An experimental buck-converter was studied in three quite different control topologies; namely the standard PWM control, a phase-shift self-oscillating (SO) controller, and a hysteretic self-oscillating controller [10]. In all cases, voltage-mode feedback was used from the output terminal after an LC filter with 23kHz resonance. A PID control block with 10kHz double zeros was used to compensate for the 2nd-order response of the LC filter. The switching frequency was in all cases held around 400kHz. The three studied control schemes are illustrated in Fig. 7 and the experimental hardware shown in Fig. 11.

As demonstrated in prior art, the comparators in these different configurations can be expected to behave very differently, and no prior art modeling method has been demonstrated to account accurately for these differences.
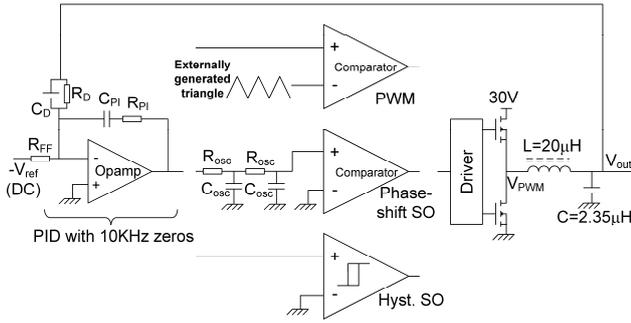
Figure 7. Experimentally tested control system configurations.
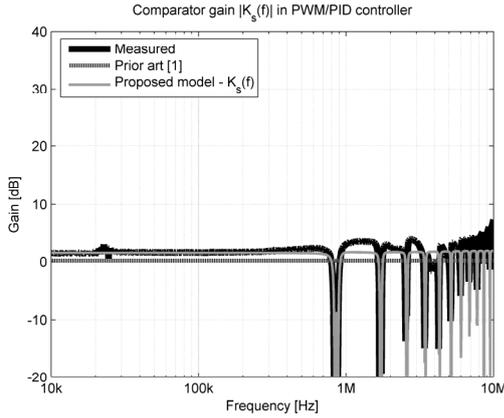

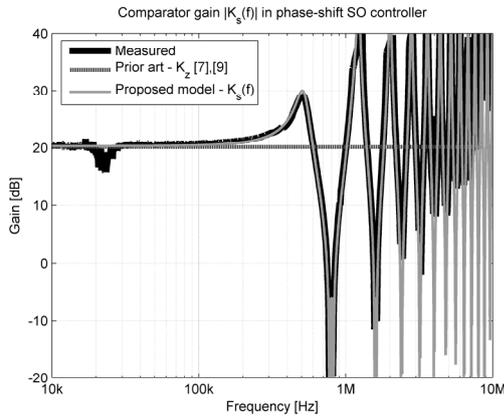Figure 8. Measured and modeled PWM comparator gains.

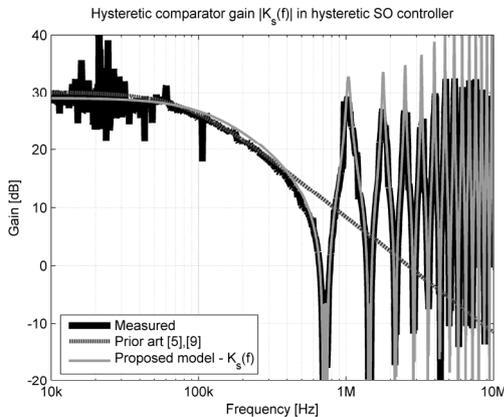Figure 9. Measured and modeled phase-shift SO comparator gains

Figure 10. Measured and modeled hysteretic SO comparator gains

For verification of the proposed modeling approach, comparator magnitude responses and output impedances were measured using an AP Instruments Model 200 gain-phase analyzer. In all cases, 1000 points were measured, logarithmically spaced between 1kHz and 10MHz, and the variable injection generator feature was used to provide a good signal/noise ratio at low frequencies (by the use of a large perturbation) while avoiding injection locking at high frequencies (requiring a small perturbation.)

The continuous-time loop transfer function $H_s(s)$ was modeled in MATLAB as the product of the LC and PID s-transfer functions calculated from circuit component values. In the phase-shift self-oscillating controller case, two poles of the oscillation network (R_{osc}/C_{osc}) were added. The comparator and power stage delay was estimated to $t_d = 80ns$ and modeled using a 2nd-order Padé approximation.

The carrier waveform $V_c(t)$ was found as the steady-state response of $H_s(s)$ to a 50% duty-cycle square-wave and calculated using a state-space representation. From this the carrier slope at the zero-crossings was found and used to calculate the comparator sampling gain K_z.

Figures 8-9-10 show comparisons between measurements of comparator magnitude responses and predictions made using relevant prior art models and the proposed modeling approach. In general, the proposed modeling method allows an unprecedented level of accuracy to be obtained from DC to above 10 times the switching frequency. In particular, the +6dB magnitude response increase at the switching frequency (needed to ensure oscillation) for the phase-shift SO controller [9] is accounted for, likewise is the single-pole behavior [5] of the hysteretic comparator. At the same time, the model handles the standard PWM block nicely, although there are 2-3dB errors at some frequencies above the switching frequency. Note that in all measurements, the LC filter resonance at 23kHz produces visible measurement noise, especially in the hysteretic SO controller, which has the highest loop gain (and therefore is the most noise sensitive at the LC resonance) among the studied controllers. As expected, the standard clocked PWM controller has the lowest gain followed by the phase-shift and hysteretic self-oscillating controllers. The gain of the hysteretic loop could possible be increased further by aligning the PID zeros with the LC resonance so that the total response is closer to an integrator. In this case, the DC gain is only limited by the power stage delay and not by the phase shift due to mismatching pole/zeros. An intuitive explanation of the lower gain of the phase-shift SO controller is that the oscillation poles add excessive phase lag that results in a DC gain reduction similar to a very large delay. For example, the theoretical $K_s(f)$ graph in Fig. 6 for a hysteretic 1st-order loop with an extreme delay equal to half a switching period shows a gain-peaking just above the switching rate very much similar to the plots for the phase-shift controller.

A. Output Impedance Measurements

Figures 12 and 13 show the measured and modeled output impedances for the three controller configurations. The modeled output impedance is the product of the open-loop LC filter impedance multiplied by the error transfer function (sensitivity function) $ETF(s)$. The clocked PWM controller only reduces the impedance up to around 60kHz while the self-oscillating controllers are effective at much
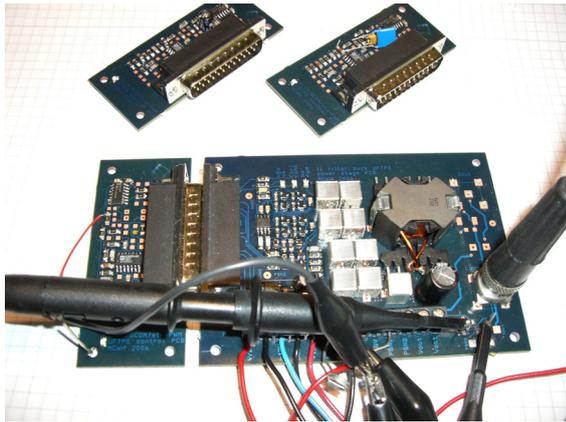
Figure 11. Experimental hardware – a common buck power stage with exchangeable control PCBs.
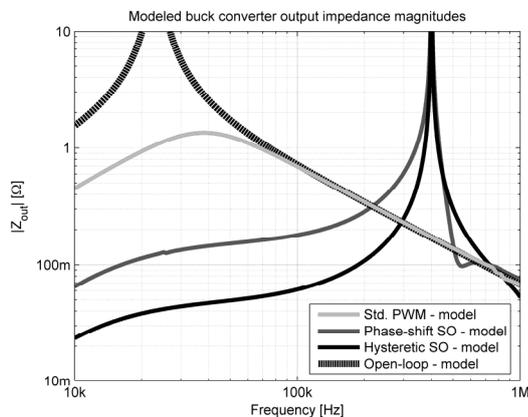

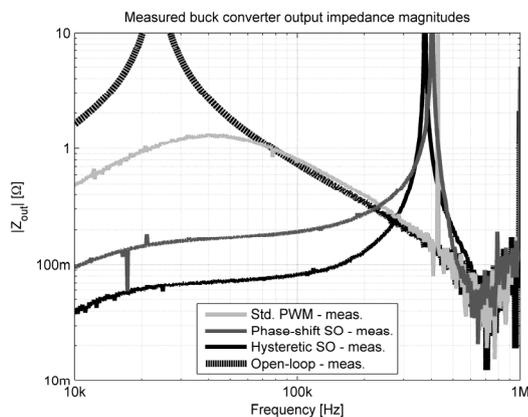Figure 12. Modeled output impedances of studied control systems, all systems switch at 400kHz.

Figure 13.Measured output impedances; systems switch at 420khz, 400khz and 380kHz respectively.

higher frequencies (up to the 200-300kHz range). The output impedance goes to infinity as expected at the switching frequency. However, in certain narrow frequency bands above the switching rate the model predicts that the controller actually reduces the output impedance compared to open-loop. Moreover, the impedance drops faster above f_{sw} for the phase-shift controller than for the hysteretic. This is in excellent agreement with the measurements. However, the measurements diverge at

high frequencies above 700kHz from the model due to stray inductance around the filter capacitor.

VI.   CONCLUSION

A versatile modeling approach has been proposed applicable to a large class of switching control systems The model is fully in continuous-time thanks to the introduction of the comparator gain $K_s(f)$ which reflects the underlying sampling nature but uses readily observable continuous-time signals.

The model gives valuable insights into the very different behaviors of various control schemes that now can be modeled and compared in the same framework. In this paper, the model has been used to demonstrate a close connection between the often separately considered clocked PWM and self-oscillating (sliding mode) control techniques. Furthermore, the model has been verified against measurements with excellent accuracy even far beyond the switching frequency.

One important limitation of the model is that it only applies to 50% duty cycle operation. Future work will hopefully extend the model to any duty cycle.

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