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A 0.2 V, 7.5 μ W, 20 kHz $\Sigma\Delta$ modulator with 69 dB SNR in 90 nm CMOS

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Abstract— This paper presents a frequency-to-digital $\Sigma\Delta$ modulator designed in a digital 90 nm CMOS process, operating with a supply voltage of 0.2 V. For a 7.5 μ W power consumption, the SNR is 68.9 dB and the SNDR is 60.3 dB over a 20 Hz-20 kHz bandwidth. This work shows that the SNR/SNDR performance of this kind of $\Sigma\Delta$ converter can be adjusted over a wide range, while maintaining a state-of-the-art figure-of-merit of 82 fJ/conversion.

I. INTRODUCTION

Traditional $\Sigma\Delta$ converters, either continuous- or discrete-time, make use of operational amplifiers, and need therefore a supply voltage slightly higher than the threshold voltage of the MOS devices used. Although very-low-voltage, operational-amplifier-based $\Sigma\Delta$ designs have been demonstrated with excellent performances [1] [2], alternative $\Sigma\Delta$ architectures are worth investigating, if radical improvements in terms of power consumption are desired.

A power-efficient alternative topology is the frequency-to-digital $\Sigma\Delta$ modulator (FDSM), where the input signal is frequency modulated in a voltage-controlled oscillator (VCO), typically making use of an inverter ring (RVCO). The topology used in this work is based on the work from [3]. This topology has no feedback, which means that the input signal does not need to be amplitude-limited as in traditional $\Sigma\Delta$ converters; if the RVCO is controlled through the bulk terminal, it is even possible to let the input (control) voltage exceed the supply rails. Furthermore, multi-bit quantization can be incorporated without any performance degradation from a feedback DAC. A 0.2 V FDSM with an SNR of 47.4 dB, an SNDR of 44.2 dB, and a figure-of-merit (FoM) of 57 fJ/conversion was demonstrated in [4]. In this work, we show that much higher SNR and SNDR are achievable by increasing power consumption, for the same exceedingly low supply voltage, at an almost constant FoM. Furthermore, the use of a differential design results in an improved SNDR, and a multi-bit FDSM is shown to reduce the quantization noise at basically no extra power consumption.

II. $\Sigma\Delta$ MODULATOR WITH INTERMEDIATE FREQUENCIES

It is well-known that feedback attenuates the non-linearities in the forward path of feedback-based $\Sigma\Delta$ modulators. When

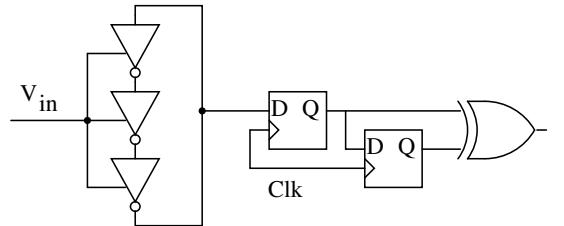


Fig. 1. First-order single-bit FDSM.

a higher quantization noise suppression is needed, however, single-loop higher-order feedback $\Sigma\Delta$ modulators tend to become unstable, and when a multi-bit quantizer is used, linearity problems are introduced through the non-ideal D/A conversion in the feedback path. Since the FDSM avoids feedback, it does not suffer from these problems, but the intrinsic linearity of the FDSM becomes more important, in order to avoid introducing harmonic distortion into the output signal.

In the FDSM, the input signal $v_{in}(t)$ is first integrated by the RVCO, which encodes the signal in the phase $\theta(t)$ of the oscillation waveform, since $\theta(t)$ is given by [3]

$$\theta(t) = 2\pi \int_{-\infty}^t (f_c + K_o v_{in}(\tau)) d\tau \quad (1)$$

where f_c is the carrier frequency and K_o is the sensitivity of the RVCO. The phase is then applied to a single- or multi-bit quantizer. The output of the quantizer is a digital signal containing both the integrated input signal and quantization noise. A digital differentiator follows the quantizer, which means that the input signal is now found at the output in digital form, while quantization noise is high-pass filtered, as in a traditional $\Sigma\Delta$ modulator. In a single-bit FDSM, the differentiator consists of one flip-flop as delay cell, and a XOR gate performing a modulo-2 subtraction [4]. Since the RVCO inverters and all digital circuitry are capable of weak-inversion operations, a supply voltage well below MOS threshold voltages is possible [5]. A first-order single-bit modulator is shown in Fig. 1.

The fact that the FDSM is an open-loop architecture makes it vulnerable to non-linearities, which produce harmonic dis-

tortion; it is therefore important to reduce as much as possible any signal-dependent component of K_o in (1). In fact, it has been shown [6] that a bias transistor placed between power supply and RVCO is quite effective in mitigating the impact of a non-constant K_o .

III. IMPROVED FDSM DESIGNS

To improve the performance of the FDSM, compared to [4], the noise floor must be lowered. There are several potential noise sources in a FDSM, but the primary source is the phase noise in the RVCO. Since the input signal of the FDSM is converted into phase, phase noise is directly added to the input signal itself. Since the phase noise in an oscillator is inversely proportional to the consumed power [7], doubling the oscillator power ideally results in a 3 dB higher SNR. We notice that the figure-of-merit (FoM) usually adopted for data converters is [8]

$$FoM = \frac{P}{2 \cdot BW \cdot 2^B} \quad (2)$$

where P is the power consumption of the modulator, BW the signal bandwidth, and B the number of bits delivered by the modulator. However, since a doubling of power consumption usually only results in a 3 dB SNR improvement, this well-known FoM actually favors low resolution modulators [9].

It should also be recognized that an increased SNR will in general require an increased sampling frequency as well, to reduce quantization noise accordingly. Since the power consumption of the digital blocks is dominated by leakage in low-frequency applications, the attending increase in power consumption is in our case minor, and the FoM is only marginally affected.

While an increased power consumption will increase the SNR, linearity is not affected by power consumption in a direct way; therefore, the SNDR is only marginally increased. One solution is to decrease the maximum signal, which will increase the SNDR, but reducing the SNR as well, which is not desirable. A more efficient way to improve the SNDR is to use a differential version of the FDSM, implemented with two identical single-ended FDSMs driven by a differential signal. In this way, even-order distortion products are highly attenuated. Since the noise sources in the two single-ended FDSM are uncorrelated, the SNR of the differential FDSM increases by 3 dB. In terms of FoM, this is as efficient as a direct increase in power consumption, but since the area is increased, it is less efficient in terms of area.

A brute-force approach to decrease quantization noise is to increase the sampling frequency, which can be difficult at extremely low supply voltages. Fortunately, there is a more intelligent way to reduce quantization noise, i.e., adopting a multi-bit FDSM. This is easily implemented using multiple RVCO outputs (taps), where each tap is still single-bit quantized.

It can be shown that multiple taps improve the signal-to-quantization-noise (SQNR) of the digital version of $\theta(t)$ in

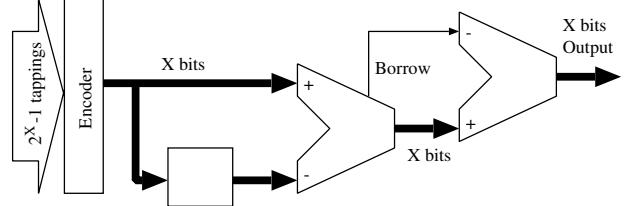


Fig. 2. Digital section of the general multi-bit FDSM with $2^X - 1$ taps.

proportion to the number of taps used [3]. For a first-order single-bit modulator using m taps, the SQNR is given by [3]

$$SQNR = 20 \log \left(\frac{m\sqrt{2}\Delta f}{f_s} \right) - 10 \log \left(\frac{\pi^2}{36} \left(\frac{2f_{max}}{f_s} \right)^3 \right) \quad (3)$$

where Δf is the maximum frequency deviation from f_c when the maximum input voltage is applied, f_s is the sampling frequency, and f_{max} is the maximum input frequency. This result is important, as it shows that the SQNR increases by 6 dB for each doubling of the number of used taps. The multi-bit solution requires extra digital circuitry, but since the power consumption in a medium-resolution modulator is dominated by the RVCO, the cost in terms of total power consumption is marginal. Idle tones exist in the FDSM [10], but another advantage of the multi-bit solution is that the amplitude of idle tones follows the size of the quantization steps. Thus, any idle tone issue is much reduced in a multi-tap FDSM.

It could also be expected that the multi-bit approach would be effective for increasing the SNR as well (limited by $1/f$ and white noise); however, quite disappointingly, this is not the case. This is due to the fact that the phase noise at one oscillator output is totally correlated to the phase noise at any other output [11]; thus, the phase noise at different outputs adds up amplitude-wise and not power-wise, and there is no net SNR improvement by processing several outputs instead of only one.

In a multi-bit FDSM, the RVCO is the same as the RVCO used in the single-bit solution. The quantization is still performed in a single-bit fashion on each tap using flip-flops, while the differentiation is given by the number of taps travelled by a signal transition during one clock period, and is calculated with a subtraction. The general solution for the digital circuit in a multi-bit FDSM with $2^X - 1$ taps (where X is an integer) is seen in Fig. 2.

The FDSM implemented in this work has 3 taps, and since the number of taps is low, it is more efficient to implement a customized circuit with digital gates, shown in Fig. 3, instead of the general circuit of Fig. 2.

IV. MEASUREMENT RESULTS

One single-tap differential FDSM and one 3-tap single-ended FDSM have been designed in a digital 90 nm CMOS process and tested. The differential, larger FDSM has an area of $160 \times 85 \mu m^2$ (photograph not included, as metal fillings hide all details). All measurements are taken with a power supply of 0.2 V.

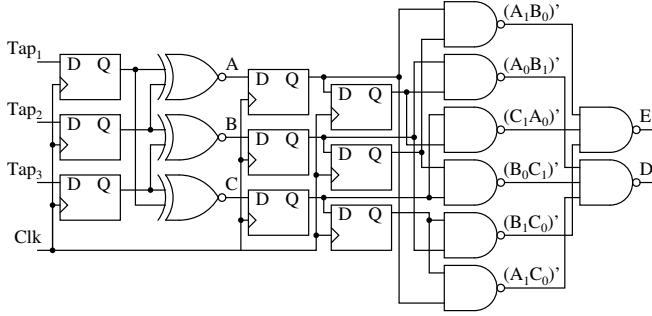


Fig. 3. The implemented digital section of the 3-tap FDSM.

To increase SNR the power consumed by the RVCOS has been increased by a factor 6 to $3.0\mu\text{W}$, compared to [4]. An additional 3 dB SNR improvement is yielded by the differential topology.

The implementation of the differential FDSM requires some attention, as its linearity performance largely relies on the matching between two independent single-ended FDSM circuits, which are therefore carefully laid out as mirrored versions of each other, surrounded by dummy components.

An additional potential problem, associated to the asynchronous nature of the FDSM, is metastability. This issue has been much alleviated, compared to [4], by a custom flip-flop redesign optimized for a very low supply voltage, and by increasing the steepness of the signals at the flip-flop inputs by inserting buffers between RVCO and flip-flops.

How well the two channels in the differential FDSM are matched has been assessed by applying a common-mode signal at the differential FDSM input, and measuring the differential output. With perfect matching, both the signal and all its harmonics should disappear at the differential output. As is clearly seen in Fig. 4, the differential signal is some 35 dB below the signal at either single-ended output, indicating as good a matching as can be realistically expected. Furthermore, the differential second-harmonic distortion is swamped by the quantization noise, while the single-ended one is clearly above it.

The $1/f$ and white noise floor is higher in the differential measurement, although it is difficult to establish whether it is exactly 3 dB higher, as expected from theory. It is, however, clear that the increase in noise power is higher when the spectrum is dominated by quantization noise. This indicates that quantization noise is not completely uncorrelated, which is reasonable. The differential circuit should also be advantageous to reduce 50 Hz noise. While this is seen in Fig. 4, there is still some 50 Hz noise left in the differential output as well, indicating that this noise source is not only appearing as a common-mode signal.

The spectrum of the differential FDSM is shown in Fig. 5, for the differential input signal giving maximum SNDR with a frequency slightly higher than 4 kHz and a sampling frequency of 12 MHz. Third-order distortion is clearly dominating, as expected. SNR and SNDR curves are shown in Fig. 6, with maximum values of ~ 69 dB and ~ 60 dB, respectively, for a

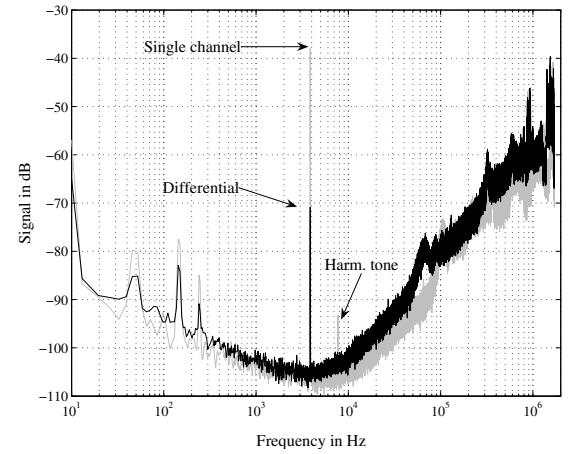


Fig. 4. Measured single-ended and differential outputs for the differential FDSM, with common-mode input signal.

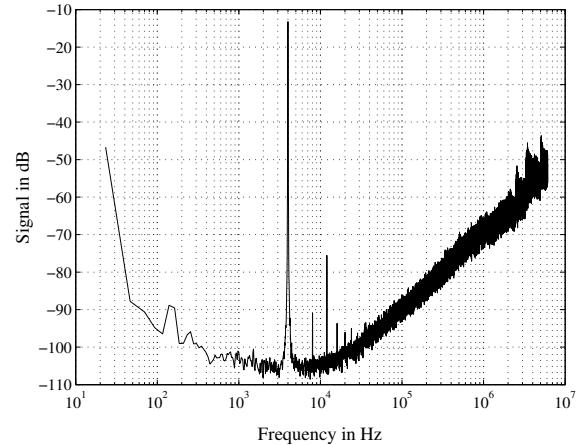


Fig. 5. Measured spectrum for the differential FDSM.

power consumption of $7.5\mu\text{W}$ ($2 \times 3.0\mu\text{W}$ in the RVCOS, $1.5\mu\text{W}$ in the digital circuitry). Thus, although the differential FDSM makes it possible to improve the SNDR, compared to previous single-ended solutions [4], the SNDR itself is limited to a somewhat lower level than the SNR. This probably means that the linearization approach used here [6] needs to be improved, if higher SNDRs are required. The differential FDSM performance is summarized and compared to other state-of-the-art audio-band $\Sigma\Delta$ converters in Table I. As expected, the FoM is slightly higher, compared to [4], but it is still much below that of other low-voltage modulators.

For the three-bit, single-ended FDSM, an SQNR improvement of $20 \log 3 \approx 9.5$ dB is expected, compared to the single-bit single-ended design, as is clear from (3). This improvement is clearly seen in Fig. 7, where the single-bit curve is obtained by utilizing only one tap in the same design. This also means that we could obtain the same SQNR for a much lower sampling frequency in a multi-tap design. It is also noteworthy

TABLE I
PERFORMANCE OF THE DIFFERENTIAL FDSM.

Parameter	This work	[4]	[1]	[2]
V_{dd} [V]	0.2	0.2	0.5	1
SNR [dB]	68.9	47.4	81	85
SNDR [dB]	60.3	44.2	74	81
Bandwidth [kHz]	20	20	25	20
Power [μW]	7.5	0.44	300	140
FoM [fJ/conv]	82	57	654	241

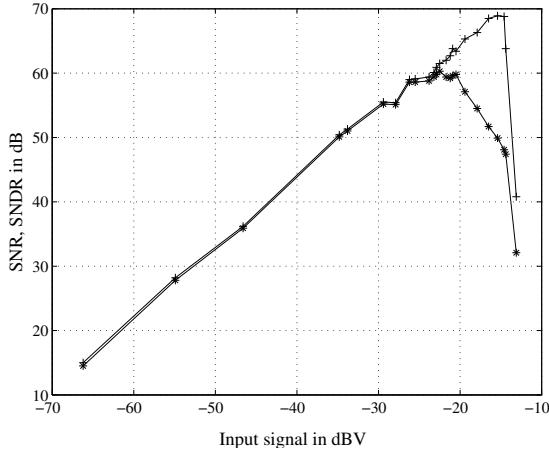


Fig. 6. SNR (+) and SNDR (*) vs. input signal for the differential FDSM.

that the $1/f$ and thermal noise floor also increase by some 9.5 dB, so that the SNR is unchanged, as previously stated on the basis of the properties of phase noise. The FoM of the three-bit FDSM is 93 fJ/conversion. This is slightly higher than what was found for the FDSM with a single tap, and is due to the increased power consumption of the digital circuitry.

Together with the prototype discussed in [4], this work proves that the SNR/SNDR of an FDSM can be traded with its power consumption, while ensuring a very low FoM in presence of the same very low supply voltage of 0.2 V. Thus, as seen in Table I, we can increase the SNR of the FDSM by some 20 dB, compared to [4], and still retain a FoM that is only marginally higher.

It is also important to realize that, unlike $\Sigma\Delta$ converters relying on MOS devices working as gain stages or current sources, an FDSM actually improves its performance when ported to newer CMOS generations. This is because an FDSM is basically a digital architecture, with only the RVCO working as an analog block, where, however, only the delay time of the basic inverter cell is of real importance.

V. CONCLUSIONS

Two first-order FDSM circuits making use of inverter-ring VCOs were implemented in a digital 90 nm CMOS process. It was shown that improved SNR/SNDR performances are possible by straightforwardly increasing the power consumption in the VCOs, operating all circuits at only 0.2 V power

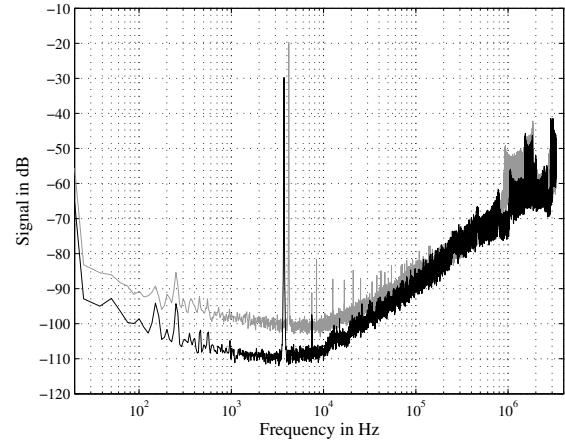


Fig. 7. Spectra for multi-bit (grey) and single-bit FDSMs.

supply. To reduce harmonic distortion, a differential FDSM was realized, which resulted in a superior performance with an SNR of 68.9 dB and an SNDR of 60.3 dB, for a power consumption of only 7.5 μW , yielding a state-of-the-art FoM of 82 fJ/conversion. A multi-bit version of the FDSM exploiting 3 VCO outputs was also implemented, with a FoM of 93 fJ/conversion, showing that this approach is very efficient in reducing quantization noise, while, according to both theory and measurements, it has no impact on thermal or $1/f$ noise.

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