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***Abstract*— This paper presents a 90 nm CMOS $\Sigma\Delta$ A/D modulator operating with a supply voltage of 0.2 V, well below the threshold voltage of the transistors. The modulator is an open-loop first-order architecture based on a frequency-modulated intermediate signal, generated in a ring voltage-controlled oscillator. The linearity of the modulator is greatly improved by the adoption of a so-called soft-rail in the oscillator. Measurements show a dynamic range of 52 dB over a 20 kHz signal bandwidth with a sampling frequency of 3.4 MHz, for a total power consumption as low as 0.44 μW. The corresponding peak SNDR is 44.2 dB, while the peak SNR is 47.4 dB.**

I. Introduction

A consumer market demanding ever smaller portable devices is, together with technology scaling, increasing the requirements on low voltage supply and low power consumption. Even though the MOS threshold voltage in future technologies can be assumed to continue decreasing, circuits containing transistors operating in strong inversion will very likely become even more problematic to design than they already are.

Traditional $\Sigma\Delta$ converters, both continuous- and discrete-time, make use of operational amplifiers, and are thus dependent on a supply voltage sufficiently higher than the MOS threshold voltage. In these converters, the feedback signal needs to be higher than the input signal, which reduces the input signal to a fraction of the supply voltage. Thus, if high resolution is required, the noise in the amplifiers needs to be very low, at the expense of power consumption.

The system presented in this paper is a frequency-to-digital $\Sigma\Delta$ modulator (FDSM) [1], where the input signal undergoes frequency modulation. An advantage of using frequency modulation is that the noise requirements in the internal circuits are not directly related to the available supply voltage. Furthermore, the FDSM does not make use of feedback, so that the maximum amplitude of the input signal is not constrained as in feedback-based $\Sigma\Delta$ converters.

This type of modulator includes a voltage-controlled oscillator (VCO) providing an integration of the input signal, a technique that has been previously demonstrated with an inverter-ring VCO (RVCO) controlled from the supply voltage [1]. In the present work, the VCO is an RVCO where the control terminal is the bulk contact of the transistors, which, thanks to a dual-well process, is possible for both nMOS and pMOS devices. This RVCO topology enables operations at extremely low supply voltages, provides a high impedance to the input signal, and even opens up the possibility of having input voltages exceeding the supply voltage in both the positive and the negative direction.

Since the modulator operates in an open-loop fashion, the intrinsic linearity of its blocks becomes extremely important, to avoid introducing distortion in the output signal. For this reason, linearity is the main concern in the design of the RVCO, since the RVCO itself does not provide a linear frequency modulation. However, the RVCO linearity is greatly improved by the adoption of a soft-rail, where the supply voltage to the RVCO is delivered through a voltage-biased transistor. The feedback provided by the soft rail enhances the linearity of the system by some 20 dB.

II. $\Sigma\Delta$ Conversion with Intermediate Frequency Modulation

The FDSM is, unlike the traditional $\Sigma\Delta$ converter, a $\Sigma\Delta$ modulator without feedback. The major advantage of feedback is that nonlinearities in the forward path of the modulator are suppressed by a high loop gain. This means that low-order single-bit modulators are simple to design. When a higher quantization noise suppression is needed, though, the single-loop higher-order modulators tend to become unstable, and when a multi-bit quantizer is used, nonlinearities are introduced by the D/A conversion in the feedback path.

Modulators without feedback, on the other hand, are always stable. However, since their nonlinearities are not mitigated by feedback, they must exhibit a sufficiently high intrinsic linearity. It may be worth noticing that digital correction of the nonlinearity is possible, to the extent that the nonlinearity itself is known.

The block diagram in Fig. 1 shows the implemented FDSM, where the input signal is first integrated, and subsequently applied to the quantizer, which can be single-bit or multi-bit. The output of the quantizer is a digital bit stream containing the integrated input signal with the additional quantization noise. A digital differentiator follows the quantizer, which means that the digital representation of the analog input signal

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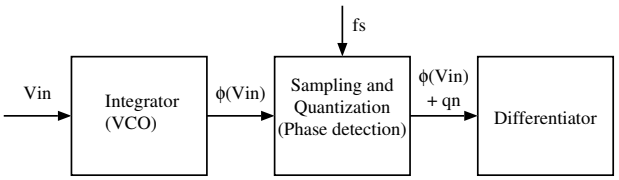

Fig. 1. Block diagram of the FDSM.

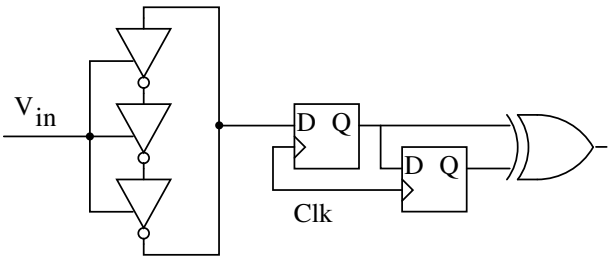

Fig. 2. First-order single-bit FDSM.

is found at the output of the modulator. The quantization noise, however, is subjected to differentiation only, which is equivalent to high pass filtering. Thus, the signal transfer function and noise transfer function in the FDSM are the same as in a traditional first-order $\Sigma\Delta$ modulator.

A digital differentiation $D(z)$ is given by

$$D(z) = (1 - z^{-1})$$

which, in a standard single-bit architecture, is easily accomplished with one flip-flop implementing the delay, and a XOR gate performing the modulo-2 subtraction.

The integrator could theoretically be a traditional operational-amplifier-based voltage integrator, but this solution would require a high supply voltage, and would therefore be inferior to the standard $\Sigma\Delta$ converter employing feedback. In the FDSM, the integration is obtained inside an RVCO, where the free-running oscillation frequency f_c is modulated by the control (input) signal $v_{in}(t)$ via the RVCO gain constant K_o. The phase $\theta(t)$ of the oscillation waveform is therefore written as

$$\theta(t) = 2\pi \int_{-\infty}^{t} (f_c + K_o\, v_{in}(\tau))d\tau \qquad (1)$$

which shows that the desired integration of the input signal has indeed been obtained. At the same time, the integration of f_c gives, after the following digital differentiation, an easily removed DC offset. The key advantage afforded by the RVCO integrator is that inverters are capable of operating in weak inversion, where they have been shown to be functional at supply voltages as low as 93 mV in a 0.6 μm process [2]. Signal quantization must be performed in combination with a phase detector; however, only zero-crossings need to be detected in a single-bit quantizer; in this case, phase detector and quantizer together turn out to be embodied by a single flip-flop.

A complete first-order single-bit FDSM is shown in Fig. 2, where the RVCO is made of an odd number of bulk-controlled inverters. One RVCO node is tapped into a flip-flop quantizing the phase signal, followed by a second flip-flop and a XOR gate implementing the signal differentiation. The XOR output is the desired $\Sigma\Delta$ bit stream.

In a first-order single-bit modulator, the signal to quantization noise ratio (SQNR) is given by [1]:

$$SQNR = 20\log\left(\frac{\sqrt{2}\Delta f}{f_s}\right) - 10\log\left(\frac{\pi^2}{36}\left(\frac{2f_{max}}{f_s}\right)^3\right) \qquad (2)$$

where Δf is the maximum frequency deviation from f_c (corresponding to the maximum amplitude excursion of the input signal), f_s is the sampling frequency, and f_{max} is the maximum frequency of the input signal. The SQNR can be improved by adopting a multi-bit quantizer, which, however, increases the complexity of the circuit in Fig. 2. A simpler way to increase the SQNR is to take advantage of the multiple output nodes in the RVCO; in fact, it can be shown [1] that the SQNR increases by $20\log(m)$, when m RVCO nodes are utilized.

From (2), it would seem that the SQNR does not depend on f_c; however, considering that Δf is proportional to f_c itself, it is clear that a way of improving the SQNR is to increase f_c.

III. VCO DESIGN

It has been mentioned that the fundamental advantage of the RVCO-based FDSM is the capability of deep subthreshold operations, thereby allowing the use of unprecedentedly low supply voltages in the $\Sigma\Delta$ modulator. Associated with this, however, is the important drawback that nonlinearities in the RVCO gain K_o are not suppressed by feedback on the input signal.

The oscillator frequency in the RVCO is [3]

$$f_c = \eta\frac{I_{ds,max}}{2NC_LV_{dd}} \qquad (3)$$

where N is the number of inverters in the ring, C_L is the load capacitance seen by each inverter, V_{dd} is the supply voltage, $I_{ds,max}$ is the maximum drain current charging C_L during a transition, and η is a scaling parameter, where $\eta I_{ds,max}$ is the mean current consumed by the oscillator. In principle, f_c can be controlled through one or more of the parameters C_L, V_{dd} and $I_{ds,max}$ in (3). Control of C_L can be obtained with different types of varactors, resulting in a possibly wide tuning range, but a very limited linearity. Using V_{dd} as control terminal results in a good linearity, but also in a quite limited input range, and a low and time-variant input impedance, which is undesirable. Controlling $I_{ds,max}$ through the bulk terminal of the transistors (i.e., by modulating the transistor threshold voltage V_{th}) yields a much more optimal input impedance. In weak inversion, the drain current I_{ds} in the MOS transistor depends exponentially on the gate-source

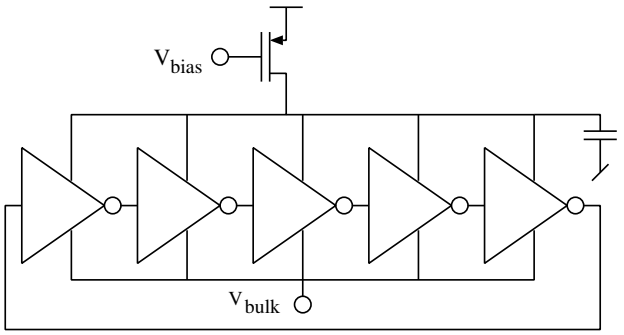

Fig. 3. RVCO with soft V_{dd} rail.

voltage V_{gs} as in a bipolar transistor, according to [4]

$$I_{ds} = I_0 e^{(V_{gs}-V_{th})/nV_T}\left(1 - e^{-\delta\frac{V_{ds}}{V_T}}\right) \tag{4}$$

where I_0 is a process-dependent current, V_{ds} is the drain-source voltage, δ and n are fitting parameters, and V_T is the thermal voltage, amounting to approximately 26 mV at room temperature. From (4), it can be shown that the maximum drain current $I_{ds,max}$ has the following proportionality [5]:

$$I_{ds,max} \propto e^{-\gamma\sqrt{2\phi_f - V_{bs}}/nV_T} \tag{5}$$

where γ is a process constant, ϕ_f is the surface potential of the MOS transistor, and V_{bs} is the bulk-source voltage. Clearly, $I_{ds,max}$ is a function of V_{bs} to a power higher than unity, and this will inevitably introduce distortion.

It can be noticed that, since the second-order derivative of $I_{ds,max}$ with respect to V_{bs} is always positive, the first-order derivative of the RVCO gain K_o is positive as well, and thus a negative feedback reducing the oscillation frequency when V_{bs} is increased is highly desirable, as this results in a more linear K_o. Since the maximum value of V_{gs} in (4) is equal to V_{dd}, it is clear that $I_{ds,max}$ is exponentially dependent on V_{dd}, which results in a strongly reduced current when V_{dd} is decreased. This can be used to improve the linearity of the RVCO by using a soft-rail technique, where V_{dd} is delivered to the RVCO through a pMOS bias transistor, as shown in Fig. 3.

The principle is that, when V_{bs} is increased, I_{ds} increases as well, resulting in an increased mean total current consumption in the RVCO, which flows through the soft-rail transistor. This, in turn, has a fixed gate-source voltage, and thus its drain-source voltage will increase with an increased drain current. Seen from the RVCO, this is equivalent to a reduction in the supply voltage, and the desired negative feedback on I_{ds} and K_o is thus obtained. Seen from another point of view, this approach trades modulation depth (since both V_{dd} and I_{ds} are reduced in (3)) for an improved linearity.

The amount of linearization obtained can be controlled through the dimensions and the bias voltage of the soft-rail transistor.

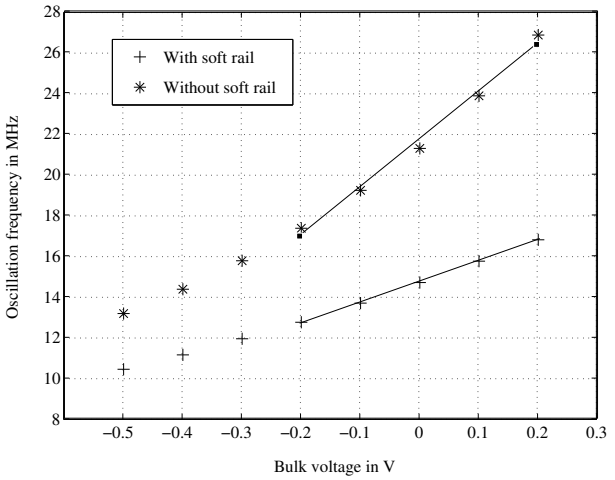

Fig. 4. Modulation linearity improvement with the soft rail technique.

IV. Measurement results

A complete single-bit FDSM has been implemented in a standard 90 nm CMOS process. The core of the modulator includes a 15 stage RVCO, where both nMOS and pMOS bulk terminals are controllable. The flip-flops are standard master-slave realizations, and the XOR gate is built with NOR logic cells. The design includes also a readout circuit consisting of five additional flip-flops and output buffers. The active die area is 100μm$\times 200\mu$m; a chip photograph is not included, since all details are hidden behind dummy metal patterns added by the foundry.

The FDSM was found to be operational with a power supply down to 0.18 V, while all measurements presented here are obtained with $V_{dd} = 0.20$ V. With the pMOS bulk tied to the supply and the nMOS bulk tied to ground, f_c is approximately 14 MHz, with a sensitivity of 10 MHz/V. This result is obtained with a soft-rail transistor bias voltage of approximately 0 V, which is also the bias voltage providing maximum linearity. Such a value of f_c is too high to allow oversampling in the quantizer and in the differentiator; this is not, however, a severe limitation, since undersampling is allowed [1], trading a reduced SNR for a reduced power consumption. The power consumed by the oscillator is $0.18\,\mu$W ($0.2\,\text{V}\times 0.9\,\mu$A). The total core power consumption is $0.44\,\mu$W ($0.2\,\text{V}\times 2.2\,\mu$A) at the sampling frequency of 3.4 MHz.

The influence of the soft-rail transistor is illustrated in Fig. 4, where the oscillation frequency of the RVCO is plotted as a function of the input voltage. The bias voltage of the soft-rail transistor was adjusted to linearize K_o for values of the input (control) signal in the vicinity of 0 V. The soft-rail transistor can not be bypassed, but by applying a large negative voltage (e.g., -1 V) to its gate, it was effectively turned into a short circuit. The linearity of the curves in Fig. 4 is clearly improved when the soft-rail is active, at the expense of a reduced modulation depth. The increased linearity results in a 20 dB higher spurious-free dynamic range (SFDR) in the output spectrum, when the input signal is 10 dB below its

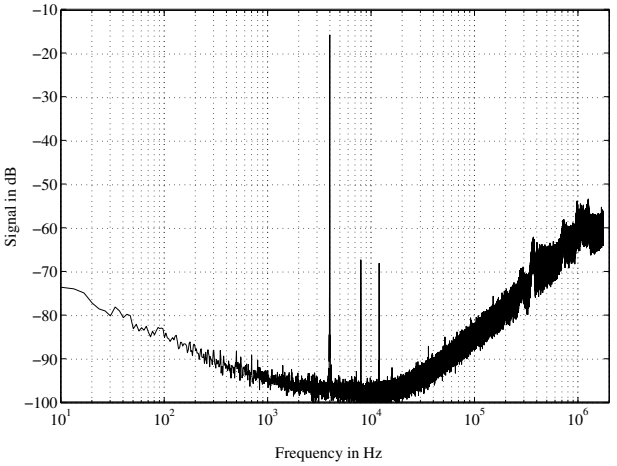

Fig. 5. Output spectrum providing maximum SNDR over a band from 20 Hz to 20 kHz.

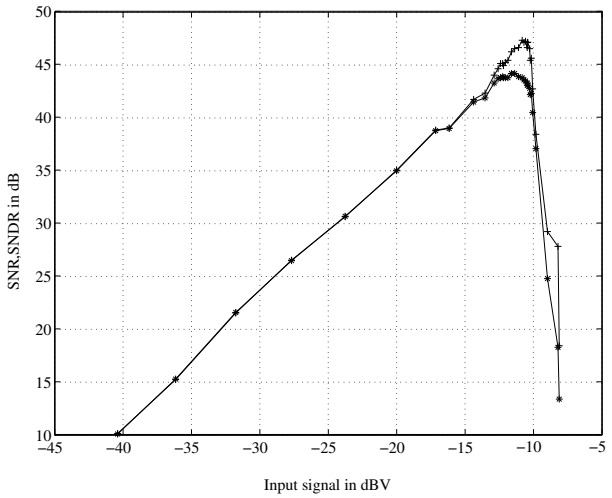

Fig. 6. Measured SNR and SNDR versus peak to peak input signal amplitude.

maximum level.

The output spectrum corresponding to maximum SNDR is shown in Fig. 5. The SNR is limited by white noise up to the audio band limit of 20 kHz. Fig. 6 shows both SNR and SNDR as functions of the amplitude of the input signal. The maximum SNDR is 44.2 dB, and the maximum SNR is 47.4 dB, both measured with a 4 kHz input tone over the full audio band from 20 Hz to 20 kHz. The dynamic range (DR) is approximately 52 dB.

No previously demonstrated modulators have been operating on supply voltages as low as 0.2 V. Therefore, the performance of the modulator is compared to the state-of-the-art through the well-known figure-of-merit (FoM) [6]

$$\text{FoM} = \frac{P}{2BW \cdot 2^N} \tag{6}$$

TABLE I

SUMMARY OF MEASURED PERFORMANCE.

Clock frequency	3.4 MHz
Signal bandwidth	20 kHz
DR	52 dB
Peak SNR	47.4 dB
Peak SNDR	44.2 dB
Supply voltage	200 mV
Power consumption	0.44 μW
Active chip dimensions	100x200μm^2
FoM	57fJ/conversion
Technology	90 nm triple well CMOS

where P is the power consumption, BW is the signal bandwidth, and N is the effective number of bits of the converter, which is here calculated to 7.6 from the SNR data. This results in the very low FoM of 57 fJ/conversion. Compared to other state-of-the-art audio converters (see e.g. [7] [8]), the achieved result is very competitive. The performance of the modulator is summarized in Table I.

V. CONCLUSIONS

A complete analog-to-digital modulator providing first-order $\Sigma\Delta$ noise shaping has been presented. The modulator, which adopts an open-loop architecture, is based on a VCO integrating the input signal, followed by a digital differentiation. The 90 nm CMOS prototype allows operations at a 200 mV supply voltage, for a power consumption of only 0.44 μW. To improve the linearity of the frequency modulation performed in the VCO, a soft-rail bias transistor is used in the VCO, which results in a 20 dB linearity improvement. The SNDR, SNR and DR performances of the modulator were measured to 44.2 dB, 47.4 dB and 52 dB, respectively, over a full 20 kHz audio signal band.

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