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Fully Integrated 1.7GHz, 188dBc/Hz FoM, 0.8V, 320μW LC-tank VCO and Frequency Divider

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Abstract

This paper presents a 0.13μm CMOS 1.7GHz VCO with frequency divider, suitable for ultra-low-power hearing-aid applications. The circuit has a 16% tuning range, a minimum power consumption of 320μW from a 0.8V power supply, power-supply and temperature compensation, an excellent 188dBc/Hz figure-of-merit without the need of off-chip components, and an area of 0.2mm^2.

Introduction

The continued silicon process scaling has enabled a wide range of new applications for wireless technology with very low power consumption, including pagers, high quality headsets with long battery lifetime, camera pills transmitting pictures from the intestines of the body, sensor networks with node battery lifetimes of several years, RFID transponders operating only on the received RF power, and FM receivers for hearing aids and cochlear implants.

Recently published ultra-low-power (ULP) radio circuits (see e.g. [1][2]) have single-digit mW power consumption and use a number of off-chip components, particularly inductors with a high quality factor (Q), in order to resonate out parasitic capacitances to achieve a (narrowband) high node impedance at high frequencies. However, apart from the ever-present cost considerations, also the physical volume of off-chip components may be of the utmost importance in some cases. This is definitely true for the most advanced hearing-aid applications: in the smallest hearing aids fitting completely inside the ear canal (completely-in-canal, CIC) volume is so precious, that even an 0201 SMD component can be too bulky. Regarding power consumption, many applications will become possible when sub-mW radios are available. As an example, wireless audio streaming to and from a CIC hearing aid will only be possible at sub-mW levels, as the total CIC power budget is in the order of a few mW.

Another trend in ULP radios is the increasing frequency of operations: if several MHz of spectrum are needed, the unlicensed spectra located between 700MHz and 930MHz are the first practical option in most countries. Unlicensed spectrum, however, can be very crowded; therefore, it is important that strong interferers at small frequency offsets do not harm the desired signal. This is especially true for the weak wanted signals that are typical in ULP radios. This requirement implies that a high quality voltage-controlled oscillator (VCO) is a key block in an ULP radio, which again explains why micro-power LC VCOs normally use off-chip high-Q inductors. Another important function in an ULP radio is the generation of quadrature LO signals, since direct conversion is the most power effective solution in the transceiver design. Whenever frequency pulling from the transmitter chain is an issue, the safest choice on the receiver side is to let the VCO oscillate at double frequency, and then recovering both the desired frequency and the quadrature phases needed in direct conversion by means of a frequency divider.

This paper presents a fully integrated 1.7GHz sub-mW VCO and a quadrature frequency divider, intended to cover unlicensed spectrum in the 750-900MHz band. The circuit, targeting a CIC hearing aid application, is fully functional for temperatures between 0°C to 60°C and for a power supply as low as 0.8V, where power consumption is only 320μW; it displays a frequency tuning range of 16%, a state-of-the-art phase noise performance, and occupies an area of only 0.2mm^2 in a 0.13μm standard CMOS process.

VCO design

The schematic of the VCO is shown in Fig. 1, together with the automatic amplitude control (AAC) loop. It is the standard implementation of an LC-tank oscillator with complementary switches (M1-M4), with the frequency tuning performed by a combination of a 4-bit binary-weighted switched-capacitor array (coarse tuning) and accumulation-mode MOS varactors (fine tuning). The power budget of the VCO is $\sim$250μA, and the resulting oscillation amplitude must be large enough to drive the following frequency divider with a safe margin. Given these specifications, the obvious topology for the oscillator is that with complementary switches, which results in twice as high oscillation amplitude, compared to the topology with a single switch pair and the same inductance with a center tap. Moreover, the inductor with the largest inductance value compatible with the desired oscillation frequency and tuning range was selected, resulting in the largest equivalent parallel tank resistance, and thereby the largest oscillation amplitude for a given bias current. The final choice was a 9nH inductor with a Q in excess of 12 at 1.8GHz. Standard copper metal layers and copper vias allow this combination of a relatively high Q with a large inductance value. Simulations show a peak oscillation amplitude of 200mV under nominal working conditions ($V_{dd} = 1.0$V, T=27°C).

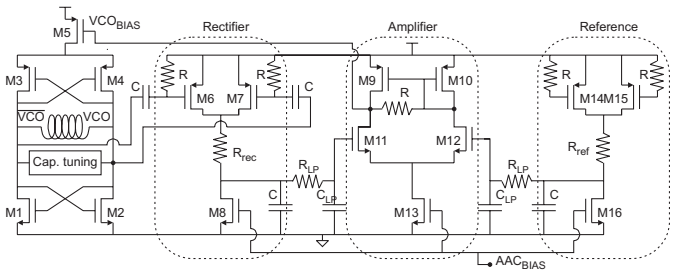

Fig. 1. Oscillator schematic consisting of both VCO and AAC circuitry.

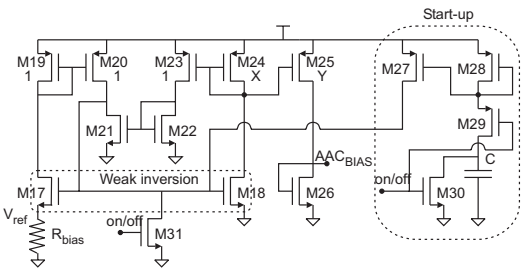

Fig. 2. Bias circuit for the AAC.

Automatic control of the oscillation amplitude

The automatic amplitude control (AAC) circuit (see again Fig. 1) is based on a high-frequency rectifier (M6-M8), an on-chip reference generator (M14-M16), and a differential to single-ended error amplifier (M9-M13) comparing the rectified VCO signal to the reference voltage [3]. The output signal of the error amplifier is fed back to the bias transistor of the VCO (M5), providing a feedback for the VCO bias current. For the configuration in Fig. 1, negative feedback is ensured if R_{rec} is larger than R_{ref}; further, the VCO signal amplitude A_{vco} established by the feedback loop is an almost linear function of the ratio R_{rec}/R_{ref} for a given AAC_{bias}, at least for the amplitude range relevant in this application. The ratio R_{rec}/R_{ref}=50kΩ/25kΩ results in A_{vco}=200mV, which is the desired nominal peak amplitude. The C-R-C filter in the rectifier removes the residual oscillation ripple from the rectified signal. An advantage of the chosen AAC circuit is that the start-up VCO current is large, compared to the steady-state current, which helps reducing the initial transient response of the circuit. The AAC loop has been designed for a total current consumption of 15μA.

The bias circuit chosen for generating the AAC bias voltage (Fig. 2) is based on the current reference originally proposed in [4], which exploits the $I_{ds} - V_{gs}$ characteristics of MOS transistors working in weak inversion. The improved circuit [5] adopted here, introducing the gain stage M20-M23, greatly reduces the impact of channel-length modulation on M17 and M24, which can not be neglected in modern deep sub-micron technologies. The current I_{bias}, which is mirrored and scaled-up in the AAC circuit though the AAC_{bias} signal, is given by V_{ref}/ R_{bias}. It can be shown that

$$V_{ref} = n\, V_t\, \ln\left[(S_1 S_2)\,/\,(S_8 S_3)\right], \qquad (1)$$

where n is slope factor for transistors working in weak inversion, V_t is the thermal voltage, and S_x is the aspect ratio of transistor Mx. As is clear from (1), I_{bias} increases linearly with temperature, which counteracts the temperature impact on the transistors of the VCO and of the frequency divider. In this way, both simulations and measurements show that the VCO and the cascaded frequency divider are able to work properly for temperatures between 0°C and 60°C. Equally important, corner and Monte Carlo simulations indicate that the design performs properly for all corners allowed by the process.

The bias circuit contains also a start-up circuit (forcing the bias circuit to evolve to the desired state), and the power-down switches M30 and M31. When the on/off signal goes high, the bias circuit is disabled, which disables the whole circuitry as well, resulting in a total power-down current consumption of only 800nA. When active, the bias circuit consumes approximately 2.5μA.

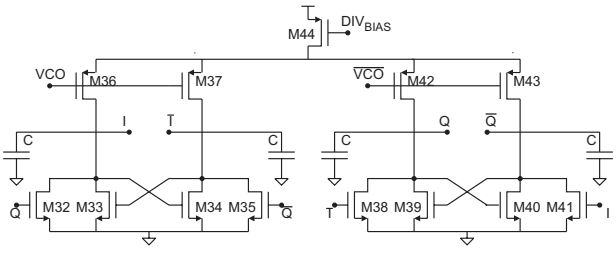

Fig. 3. Injection-lock quadrature frequency divider.

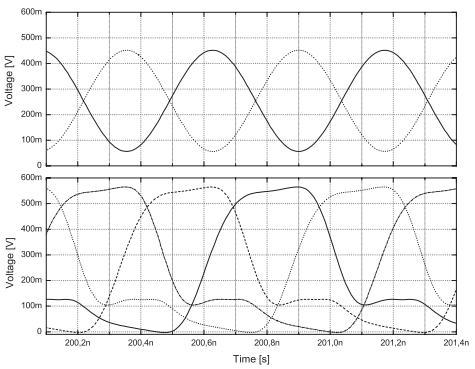

Fig. 4. Input (top) and output signals for the frequency divider.

Frequency divider

It is well-known that frequency division can be accomplished both in the digital and in the analog domain, the latter choice having the advantage of lower power consumption and lower noise. For these reasons, an analog divider exploiting injection lock has been used in this work. The circuit, shown in Fig. 3, is an adaptation of the digital divider proposed in [6]. In the original implementation the pMOS transistors were completely turned on and off by large LO signals, while in our case the LO signals have a reduced amplitude and a DC value close to zero, which means that the pMOS transistors are always on, with a (trans)conductance modulated by the LO signals. In case the LO signals are absent, or possess too small an amplitude, the pMOS transistors deliver a constant current whose magnitude is dependent on the DC voltage at their gates, and the divider works as a quadrature oscillator made of two transconductor cells coupled in quadrature. Injection lock en-

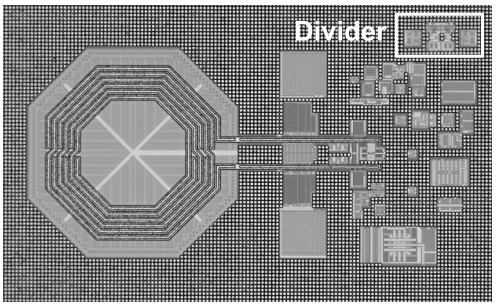

Fig. 5. Die photo of the entire circuit (570μm $\times$ 340μm).

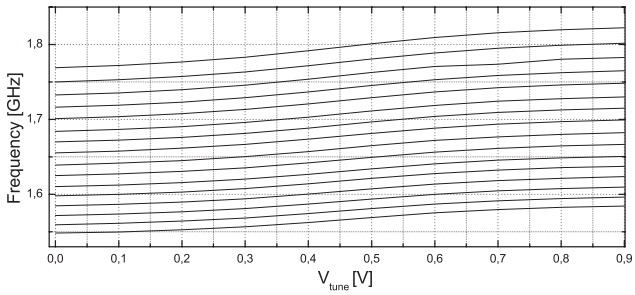

Fig. 6. VCO tuning range as a function of the 4-bit switched-capacitor array and of the control voltage of the accumulation-mode MOS varactors.

sues for large-enough variations of the pMOS current, when the natural current at each output node, itself at double the frequency of the output voltages, locks onto the injected current. Fig. 4 shows the input and output voltages of the divider for a nominal current consumption of 150μA, the divider remaining operational for currents as low as 100μA. An injection-lock LC-tank divider of the kind presented in [7] would probably work with an even lower power consumption; however, there are three reasons why our choice is preferable for the targeted application. The Þrst and most obvious is the negligible area needed in an inductorless implementation; the second is that LC-tanks tuned at half the LO frequency may very well capture disturbances coming from the transmitter chain, which is transmitting very close to that frequency; as a consequence, the divider may become injection-locked to the power ampliÞer of the transmitter, which is the very problem we endeavor to avoid with the present architecture. The third reason is that an inductorless oscillator has an equivalent quality factor Q of approximately unity, which means that the locking range is very large, being proportional to the inverse of Q [7]. When driven by the previously described VCO, our frequency divider displays a measured locking range of $\sim$1GHz for the nominal current consumption, which is well in excess of what is needed to cover process tolerances, temperature and power supply variations. Measurements taken on a standalone version of the divider yield results very close to those obtained previously through simulations. The signals at the output of the divider are large enough to drive a passive quadrature mixer, without the need of intermediate buffering.

Measurement results

The VCO and frequency divider were fabricated in a 6M 0.13μm CMOS process with high-Q inductors and varactors, all available as parametric cells in the design kit. A die photograph of the circuit is shown in Fig. 5, where unfortunately the lower-level metals are hidden by upper-level metal Þllings to comply with the speciÞc design rules. Fig. 6 shows the VCO tuning range as a function of the 4-bit switched capacitor array and the varactor tuning voltage. The VCO covers the spectrum from 1.55GHz to 1.82GHz, giving a tuning range of 16%.

A. Measurements versus power supply and temperature

In the following, several measurements versus power supply voltage V_{dd} and temperature will be shown, demonstrating the excellent performances of both VCO and frequency divider. Measurements performed on two different chips will be compared to the typical simulated values. All measured values are within the process corners.

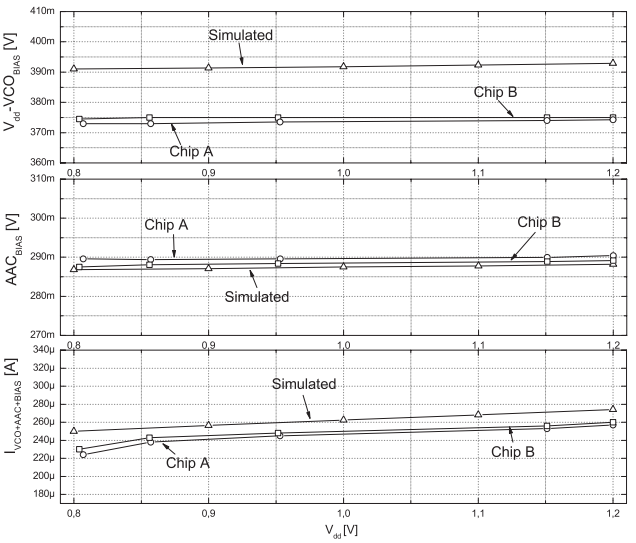

Fig. 7. Bias voltages VCO_{bias} (top, referred to V_{dd}) and AAC_{bias} (middle), and total VCO current (bottom) versus V_{dd}.

Fig. 7 shows the voltage output (VCO_{bias}) of the error ampliÞer (i.e., the bias voltage of the VCO bias transistor M5, Fig. 1), the voltage output of the bias circuit (AAC_{bias}), and the total current consumption of VCO, AAC, and bias circuit together, as functions of V_{dd}. The measured data is very close to the simulated data. Both voltages vary negligibly with V_{dd}, indicating that both AAC and bias circuits perform as desired within the 0.8V-1.2V supply range. As the bias current of the VCO is controlled through VCO_{bias}, it is clear that also the bias current is a ßat function of the supply voltage, the main variation being caused by channel-length modulation of the bias transistor M5. In fact, as shown in the bottom of Fig. 7, the total current consumption of VCO, AAC, and bias circuit together is almost constant, varying by less than 6% across the voltage range.

Plots of VCO_{bias} and AAC_{bias} versus temperature are displayed in Fig. 8, while Fig. 9 shows the measured total current consumption of the VCO, AAC and bias circuits, again versus temperature. Apart from a small offset between simulated and measured values, the behavior is as expected. This also means that the variation of the oscillation amplitude, whose simulation is also visible in Fig. 9 (measurements were not possible for this internal and very sensitive node) are $\pm 10\%$ around the nominal value, which is safely covering the amplitude range needed by the frequency divider. It is also important to note

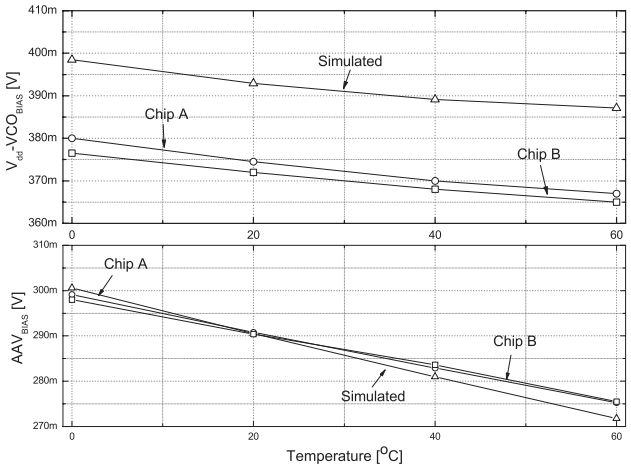

Fig. 8. Bias voltages VCO_{bias} (top, referred to V_{dd}) and AAC_{bias} (bottom) versus temperature.

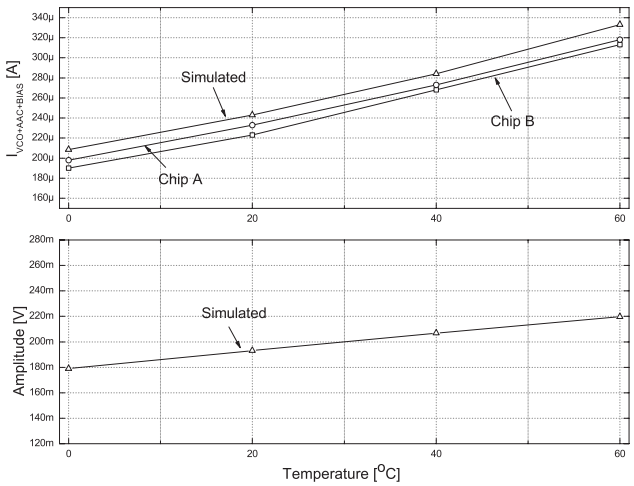

Fig. 9. Total current of VCO, AAC and bias circuit (top), and simulated amplitude of VCO oscillation (bottom), as functions of temperature.

that these variations are considerably smaller than the $\pm 25\%$ variations undergone by the total current over the same temperature range. As mentioned earlier, the frequency divider draws a nominal current of 150μA, but measurements show that it is able to divide the incoming frequency correctly under all working conditions for a bias current as low as 100μA. The overall current consumption is $\sim$400μA, resulting in a power consumption of $\sim$320μW when the chip is operated at V_{dd}=0.8V.

B. Phase Noise

The measured phase noise of the VCO is very constant across the whole tuning range, with phase noise variations of less than 2dB. Fig. 10 shows a typical phase noise plot, taken in the middle of the fine tuning range, where the AM-to-PM phase noise generation mechanism is highest. The agreement between simulations and measurements is very good, especially at higher offset frequencies (the drop for offsets higher than 5MHz is an artifact of the measurement system, which employs a 100ns delay line). The phase noise measured at the output of the frequency divider (consuming 150μA) is $\sim$6dB lower, which is the expected improvement when dividing the frequency by two.

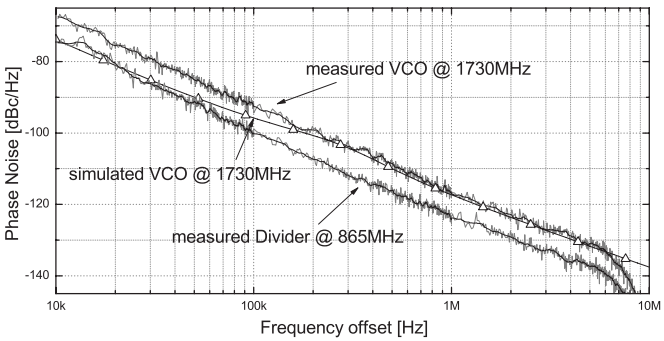

Fig. 10. Simulated and measured phase noise for a carrier frequency of 1730MHz (coarse-tuning word is [0100], fine-tuning voltage is $\mathrm{V}_{dd}/2$).

The figure-of-merit (FoM) of the VCO is given by

$$FoM = \mathcal{L}(\Delta f) + 20\log\left(f_0/\Delta f\right) - 10\log(P) \qquad (2)$$

where $\mathcal{L}(\Delta f)$ is the phase noise at the offset frequency Δf, f_0 is the frequency of the carrier, and P is the power consumption in mW. Equation (2), calculated for Δf=1MHz, f_0=1730MHz, and P=0.9V$\times$250μA=225μW, yields a very high FoM of 188dBc/Hz, although the LC-tank was designed for maximum oscillation amplitude and not for maximum FoM. Further, it should be of interest remarking that, unlike most examples found in the literature, this FoM is relative to the complete VCO with biasing and AAC circuit, which usually contribute a non-negligible amount of phase noise, and this without the need of large off-chip filtering capacitors.

Conclusions

A fully monolithic RF VCO and a frequency divider, covering the unlicensed bands in the 750-900MHz spectrum, have been presented. The sub-mW power consumption, the very good phase noise performance, and the absence of external components make the design suitable for the most advanced hearing aid applications.

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