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Ultralow-Power GaAs MESFET MSI Circuits Using Two-Phase Dynamic FET Logic

Peter S. Lassen, Stephen I. Long, *Senior Member, IEEE*, and Kevin R. Nary, *Member, IEEE*

Abstract—Two-phase dynamic FET logic (TDFL) gates are used in GaAs MESFET MSI circuits to implement very low power 4-b ripple carry adders and a variable modulus (2 to 31) prescaler. Operation of the adders is demonstrated at 500 MHz with an associated power dissipation of less than 1.0 mW and at 750 MHz with $P_d = 1.7$ mW. The prescaler, which contains 166 TDFL gates and 79 static gates, is shown to operate up to 850 MHz with an associated power dissipation of 9.2 mW from its 1.0-V supply. The operation of the adders and prescalers demonstrates the use of three- and four-input TDFL gates and a completely dynamic TDFL XNOR gate. The TDFL gates in these circuits dissipate only from 14 to 20 nW/MHz.

I. INTRODUCTION

TWO-PHASE dynamic FET logic (TDFL) has been demonstrated to be a very low-power GaAs MESFET logic family for operation up to 1 GHz [1]–[3]. TDFL gates are capable of performing all the standard logic functions (NOT, NAND, NOR, AOI, XNOR). They are nonratioed, and have compact layouts. Furthermore, TDFL gates are compatible with static direct-coupled FET logic (DCFL) and super buffer FET logic (SBFL) gates. Because of its very low power dissipation and the compactness of its layout, TDFL is a suitable candidate for GaAs VLSI.

The primary purpose of this work is to demonstrate that TDFL can be used in circuits of moderate complexity. In particular, we report on the implementation of 4-b ripple carry adders, one of which is composed of 116 TDFL gates, and a variable modulus prescaler using 166 TDFL gates and 79 static gates (DCFL and SBFL). The operation of these circuits from a 1.0-V power supply at frequencies up to and above 800 MHz demonstrates the ability of TDFL to perform at very low power and high frequencies in a standard GaAs digital IC foundry process (Vitesse/MOSIS). Integral to the operation of the adders and the prescaler are a new TDFL XNOR gate, three-input NOR and NAND gates, and 22-AOI (AND-OR-INVERT) gates. We report the results of SSI test circuits of these gates.

Additionally, this work demonstrates the unique capabilities of TDFL. The unusual prescaler architecture, a tapped

AOI shift-register ring, was enabled by TDFL's self-latching characteristic and its compatibility with conventional static logic gates. The prescaler is capable of dividing by all integers from 2 to 31. Very high gate equivalence was obtained in the prescaler contributing to its low power dissipation as well as to its compact layout.

II. BACKGROUND

A detailed description of TDFL gate design, operation and test circuit performance can be found in [1] and [2]. TDFL gate operation can be understood with the aid of Fig. 1 which shows the schematic of two TDFL inverters and a timing diagram. All TDFL gates operate from a single 1.0-V (or greater) power supply and two nonoverlapping clocks that toggle (typically) from -1.2 to 0 V. When Φ_1 is high (the precharge phase of operation of inverter #1), the output of inverter #1 is charged to 1 V while the input value is passed to node A. Node A is charged to approximately 600 mV if the input is high, or it is discharged to ground if the input is low. During the evaluation phase of operation of inverter #1, Φ_2 is high, and the value at the output is passed to node C of inverter# 2.

Notice from Fig. 1(b) that TDFL gates are sequential: the output of an inverter is the inverse of its input one half clock cycle ($T/2$) later. While this property limits propagation delay to $T/2$, it also provides latched outputs at no extra cost in area or power—a distinct advantage for pipelined or sequential applications. Shift registers can easily be formed by cascades of any of the TDFL logic gates. Notice also from Fig. 1 that TDFL logic levels are compatible with DCFL and SBFL levels. The output of a TDFL gate can drive the input of either static gate type through a pass transistor, and the output of a static gate can be connected directly to a TDFL input.

TDFL uses nonoverlapping clocks to eliminate static power dissipation. By sequentially toggling transistors Q_3 and Q_4 in Fig. 1(a), a direct current path from V_{dd} to ground is prevented. When operated from a 1.0-V supply, TDFL gates dissipate only 24 μ W at 500 MHz (fan-out of 2; load capacitance of 100 fF). If the power overhead of the clock generator and driver circuitry is added to that dissipated from V_{dd} , the power dissipation figure is still an incredibly low 50 μ W per gate at 500 MHz. This corresponds to 100 nW/MHz and compares very favorably to both static, 5-V CMOS (5 μ W /MHz when loaded with 100 fF [4]), and to GaAs DCFL whose gates typically dissipate 200 μ W or more (depending on loading and desired speed).

The maximum frequency of operation of a TDFL gate is limited by the speed at which its output load capacitance can

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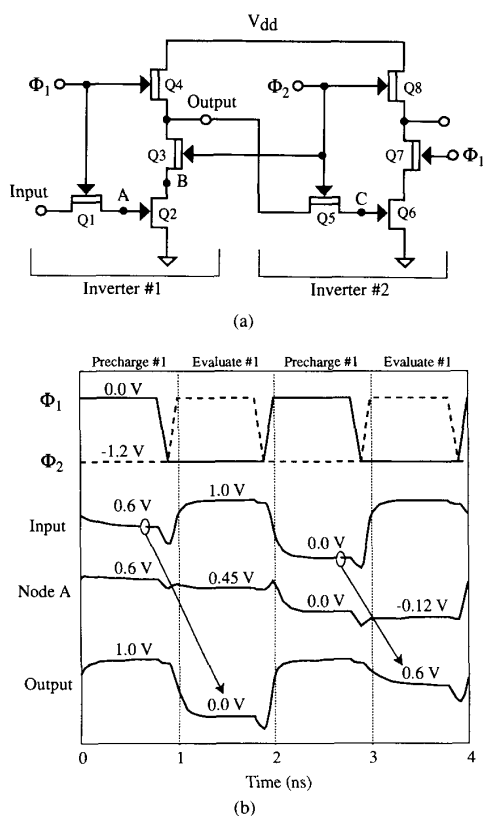


Fig. 1. (a) Schematic of two TDFL inverters in series. (b) Simulated operation of inverter with $V_{dd} = 1.0$ V.

be discharged. In circuits of moderate complexity like those reported here, the maximum frequency of operation is between 750 and 850 MHz. Because the operation of TDFL gates relies on the storage of charge on isolated circuit nodes, there is a minimum frequency of operation. The effect which determines this frequency is the leakage of charge from node A (Fig. 1(a)) through the gate to source Schottky diode of transistor Q2. Simulations indicate that the minimum frequency of operation is around 10 MHz although circuits have been demonstrated to operate down to 2 MHz.

III. CIRCUIT DESIGN

A. 4-b Ripple-Carry Adders

In [1], an XOR gate composed of three TDFL gates and a DCFL gate was described. This XOR gate topology and an XNOR gate topology in which the NAND gates are replaced by NOR gates were used with moderate success in four- and eight-stage linear feedback shift registers (LFSR's) and in a 4-b adder [3]. Subsequent to the design of these circuits, an XNOR gate topology which dissipates only dynamic power was found in the literature [5]. A schematic of this gate is shown in Fig. 2 and its layout in Fig. 3.

The key to the operation of the XNOR gate shown in Fig. 3 is the cross-coupled E-FET's Q7 and Q8. During the precharge phase of operation, Φ_1 is high and Φ_2 is low. Thus the output

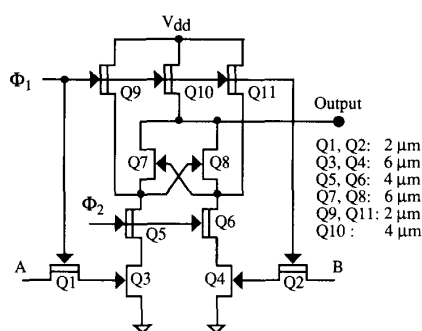


Fig. 2. Schematic of 11-transistor TDFL XNOR gate which dissipates only dynamic power.

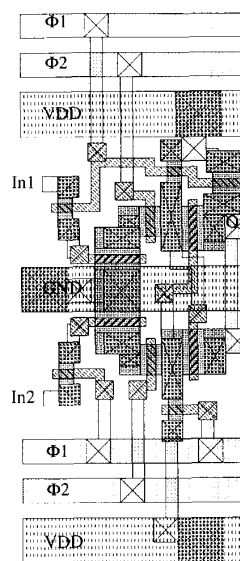


Fig. 3. Layout of XNOR gate. Dimensions are 38 μm \times 91 μm .

and the gates and sources of E-FET's Q7 and Q8 are charged high (to V_{DD}) through transistors Q9–Q11, and the input data values are passed to the gates of Q3 and Q4 through pass transistors Q1 and Q2. In the evaluate phase of operation, Φ_1 is low and Φ_2 is high. If the values on the gates of Q3 and Q4 are equal, then the gate-to-source potentials of Q7 and Q8 will remain zero, and the output will remain high. If the input values are not equal, then either Q7 or Q8 will conduct and the output will be discharged through one of the two pull-down paths. Simulations of the XNOR gate with transistor sizes as indicated in Fig. 2 predict that the gate will function correctly up to 800 MHz. The failure criterion used was a 20% degradation of the logic swing.

At first glance it would appear that transistor pairs Q3 and Q4, Q5 and Q6, and Q7 and Q8 should be reasonably well matched for the XNOR gate to function correctly. Otherwise, the gate-to-source potential of one of the cross-coupled E-FET's may exceed threshold long enough to partially discharge the output. Simulations of the XNOR gate at 500 MHz indicate that it will operate even if the device mismatch between all

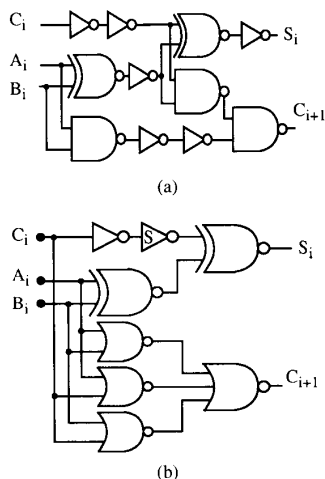


Fig. 4. Functional block diagrams of TDFL full adders which produce the sum and carry outputs in (a) two clock cycles and (b) one clock cycle.

three of these transistor pairs is 50% (i.e., one transistor of each of the above named transistor pairs twice as wide as the other).

Two full-adder designs based on the XNOR gate of Fig. 3 were implemented. Functional block diagrams of these are shown in Fig. 4. The adder of Fig. 4(a) uses two inverters on the C input and between two of the NAND gates to ensure proper timing (recall that TDFL gates are sequential). Since signals must propagate through four TDFL gates in the adder of Fig. 4(a), its latency is two clock cycles (half a clock cycle per gate). The adder design of Fig. 4(b) reduces the latency to one clock cycle by using a TDFL inverter in series with a static SBFL inverter (labeled with an S). These two inverters are used so that the carry input is presented to the input of the sum generating XNOR gate coincidentally with the XNOR of inputs A and B .

Fig. 5 depicts a block diagram of the 4-b ripple-carry adders. Shift registers are used on the inputs and outputs so that all 5 b of a sum are shifted out on the same clock cycle. These shift registers are implemented simply by cascading TDFL inverters. In the 4-b adder using the full adder of Fig. 4(a), the outputs appear eight clock cycles after the inputs are present. The 4-b adder using the full adder of Fig. 4(b) produces outputs in four clock cycles. Though the latency of these adders may be undesirable in some applications, (i.e., in applications requiring a very fast adder which is used infrequently), they are well suited for highly pipelined, serial applications in which they are used constantly. For example, they are well suited to high-speed digital signal processing applications. When addends are fed to these adders at the clock rate, sums are produced every clock cycle.

The adders (and the prescaler described below) were designed for fabrication in the Vitesse enhancement/depletion $0.8\text{-}\mu\text{m}$ process and were fabricated through the MOSIS/ISI foundry service.¹The 4-b adder which uses the full adder of Fig. 4(a) is composed of 116 TDFL gates and occupies 0.25

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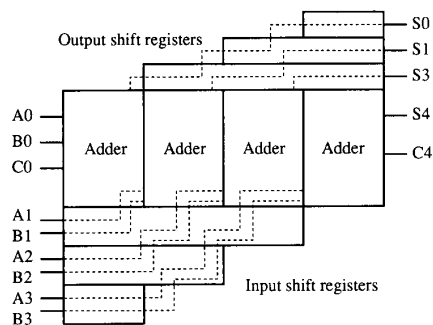


Fig. 5. Block diagram of TDFL 4-b ripple carry adder. Shift registers synchronize data into and out of adder.

mm^2 . Its predicted power dissipation at 500 MHz is only 1.3 mW. The 4-b adder utilizing the full-adder design of Fig. 4(b) uses 64 TDFL gates and 4 SBFL gates, occupies only 0.16 mm^2 , and has a predicted power dissipation of only $800\text{ }\mu\text{W}$ at 500 MHz despite the fact that it uses 4 static gates. The static gates can be designed to be very low power since their propagation delay need only be a little less than half of the intended maximum clock period (i.e., less than 500 ps). The outputs of the adders are fed into output buffers through pass transistors that eliminate the precharge phase from the output signals. The output buffers are composed of DCFL and SBFL gates.

B. TDFL Variable Modulus Prescaler

Variable modulus prescalers are important components in phase-locked loops used for frequency synthesis. While power dissipation is not critical for some applications, the increasing emphasis on portable operation of computers and communications systems has placed a priority on low-power circuit implementations. For applications from 100 MHz to 1 GHz, silicon bipolar emitter-coupled logic (ECL) and GaAs DCFL are appropriate technology choices. Prescalers made in these technologies typically use cascades of modulus two dividers realized by type D or JK flip-flops. Taking advantage of the self-latching nature of TDFL gates, the TDFL prescaler described in this work uses an architecture based upon a tapped shift-register ring—a technique used in charge-coupled device circuit design [6]. This prescaler is capable of dividing by all integers from 2 to 31.

To understand the principle behind the prescaler's operation, consider the schematic shown in Fig. 6(a) and the timing diagram in Fig. 6(b). Each gate is marked with the clock which controls its precharge phase of operation. Hence, the outputs of all gates controlled by Φ_1 are high when Φ_1 is high, and these gates are in their evaluation phase when Φ_1 is low. To initialize the ring, the *init* input is held high. After three clock periods, it can be seen that the outputs of all Φ_1 gates will be low and the outputs of all Φ_2 gates will be high. Once initialized, the *init* input is set low. This causes a logic low to propagate around the ring from *init* to nodes A , C , and then D in three clock periods. The output at node D is then inverted by a static inverter so that three clock periods after the *init* input is set low, a logic high begins to propagate around the

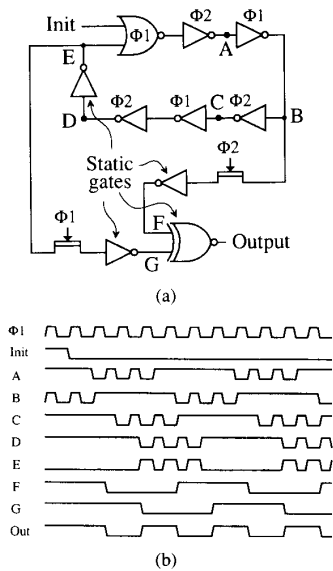


Fig. 6. (a) TDFL shift-register ring and (b) associated timing diagram.

ring. Notice that the output at any node in the ring will change state every three clock cycles. By feeding the waveform from any node in the ring through a pass transistor and a static inverter, the TDFL precharge cycle can be filtered from the waveform. This produces a waveform that has one sixth of the clock frequency (at nodes *F* and *G* of Fig. 6). By adding more TDFL inverter pairs to the ring, signals whose frequency are even fractions of the clock frequency can be made.

By filtering the precharge phase from outputs at opposite sides of the shift register ring (e.g., nodes *B* and *E* in Fig. 6(a)) and then taking the logical EXCLUSIVE OR (or the logical EXCLUSIVE NOR) of the resulting quadrature waveforms, a signal with an odd modulus, in this case one third of the clock frequency, is produced. It is necessary to use static gates to perform this XOR (or XNOR) since the inputs to it are derived from TDFL gates driven by opposite clocks and since the desired output will be an odd fraction of the clock frequency (this could not be achieved with a TDFL XNOR gate).

A simplified schematic of the prescaler ring is shown in Fig. 7. Each of the 22-AOI gates are realized with just 10 transistors, and, combined with the inverters whose inputs are the $mod(i)$ ($i = \text{even integer}$), they function as 2:1 multiplexers with latched outputs. (To illustrate the high gate equivalence that can be achieved with TDFL, a 2:1 MUX with output latch would require nine DCFL gates.) When the $mod(i)$ input to a 22-AOI gate is high, it inverts the output of the 22-AOI gate preceding it. When the $mod(i)$ input is low, the 22-AOI gate inverts the output of the inverter or NOR gate immediately above it in Fig. 7. Consequently, by setting all but one of the $mod(i)$ high, rings of different length can be made. Initialization of the prescaler ring is achieved by setting the *init* input high and by setting all $mod(i)$ inputs low.

To produce even modulus signals, the output at node *A* of Fig. 7 is selected. To produce odd modulus signals, the shift-register ring is tapped in 15 places and the desired tap is

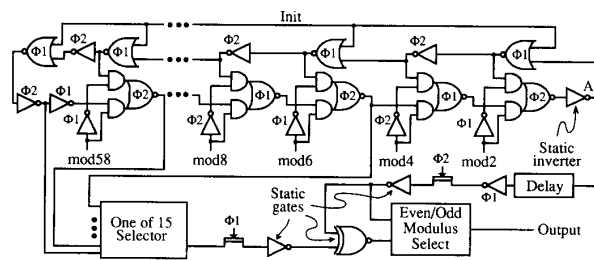


Fig. 7. Simplified schematic of TDFL variable modulus prescaler ring.

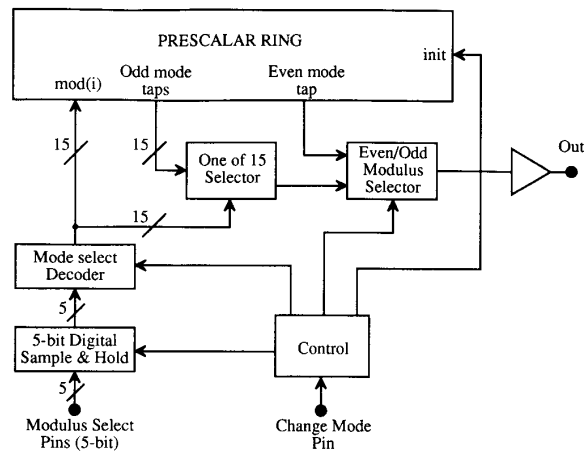


Fig. 8. Block diagram of TDFL variable modulus (divide by 2 to 31) prescaler ring.

selected with a TDFL 1-of-15 select circuit. The signal at *A* is delayed by several TDFL inverters so that the signal derived from *A* and the signal from the output of the tap select circuitry are 90° out of phase as shown previously in Fig. 6. Finally, a DCFL circuit selects the even or odd modulus signal.

A block diagram of the entire prescaler is shown in Fig. 8. Asynchronous modulus select inputs are fed into digital sample-and-hold circuits which incorporate TDFL 22-AOI gates. The outputs from the digital sample and holds are converted to the modulus select signals required by the prescaler ring by a DCFL 5-to-31 decoder. Control circuitry composed predominantly with TDFL gates is used to control the flow of data into and out of the input sample and holds, to generate the ring initialization signal, and to enable and disable the prescaler output. A static output buffer is used to drive the prescaler output off-chip. The prescaler is composed of 166 TDFL, 44 DCFL and 35 SBFL gates. The chip dimensions are approximately 1.0 mm by 1.5 mm.

IV. EXPERIMENTAL RESULTS

A. 4-b Ripple-Carry Adders

Testing of the adders was performed on packaged parts with from 1.0- to 1.5-V (peak-to-peak) clock signals which overlapped at or near 50% of their excursions. V_{dd} was nominally 1.0 V. The input signal frequencies were integer fractions of the clock frequency. Output buffers made from

DCFL and SBFL gates were used to drive the outputs off-chip. For the sake of brevity, the adder which incorporates the full adder of Fig. 4(a) shall from this point be referred to as a "type I" adder; the adder using the full adder of Fig. 4(b) is referred to as a "type II" adder.

Several SSI test circuits were included on the chip containing the type II adder. The purpose of these circuits was to verify the operation of TDFL three-input NOR and three-input NAND gates, 21 AOI gates, and 22 AOI gates. The test circuits consisted of these gates with two TDFL inverters buffering each input and a single TDFL inverter on each output. The three-input NOR and NAND test circuits operated up to 1.1 GHz typically, and to 1.3 GHz best case. The 21-AOI test circuit operated to 960 MHz typical with a best-case operation of 1.1 GHz. The maximum frequency of operation of all of the 22-AOI test circuits was 960 MHz. At 900 MHz, the power dissipated from V_{dd} by all four test circuits (34 TDFL gates) was $440 \mu\text{W}$ (average of five chips) corresponding to 14 nW/MHz/gate.

Of the ten type I adders characterized, eight were fully functional up to 450 MHz, seven were fully functional at 500 MHz, and four at 550 MHz. (When simulated with models representative of transistors which were one standard deviation toward the "slow" end of the process distribution, the maximum frequency of operation of the adder was approximately 500 MHz.) Two devices operated at 740 MHz, though they required a 1.3-V supply. The performance of the five type II adders tested was significantly better. All five operated at 600 MHz, one operated to 750 MHz, and one operated to 770 MHz. As with the type I adder, a slightly higher V_{dd} potential was required for the highest frequencies of operation. Fig. 9(b) depicts the operation of the type II adder at 770 MHz. A timing diagram of the inputs used to produce the outputs in Fig. 9(b) is provided in Fig. 9(a). In the oscilloscope photo, the signals are attenuated by 20 dB.

The average power dissipation versus frequency for the two adder types with V_{dd} equal to 1.0 V is shown in Fig. 10(a). At 500 MHz, the average power dissipated from V_{dd} (excluding output buffers) was 1.08 mW and $852 \mu\text{W}$ for the type I and type II adders, respectively. The type I adder, which operated at 740 MHz, dissipated 2.4 mW, while the two type II adders, which operated at 750 MHz, dissipated 1.7 mW. As expected, the power dissipation is linear in frequency and extrapolates to a dc power dissipation near zero. The line fitted to the type I data has a slope of $2.2 \mu\text{W}/\text{MHz}$ and has an extrapolated zero frequency power dissipation near 0 mW ($-29 \mu\text{W}$). The fit to the type II data has a slope of $1.3 \mu\text{W}/\text{MHz}$ and a zero frequency power dissipation of $170 \mu\text{W}$ (the static power consumed by the four SBFL gates used in this design). The power dissipated per megahertz per gate is 19 and 20 nW/MHz/gate for the type I and II adders, respectively. Fig. 10(b) is a scatter plot of the power dissipation versus frequency for the type II adder. Included are data points for which V_{dd} was other than 1.0 V.

The performance of the type I adder was characterized as a function of V_{dd} and of the clock levels. At 450 MHz, the mean minimum V_{dd} was 840 mV. Increasing V_{dd} to 1.3 V enhanced the maximum frequency of operation by as much as 200 MHz,

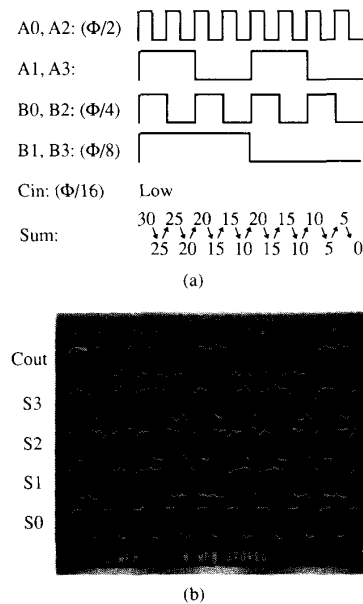


Fig. 9. (a) Timing diagram of inputs and expected sum and (b) oscilloscope photo showing outputs from type II TDFL 4-bit adder operating at 770 MHz.

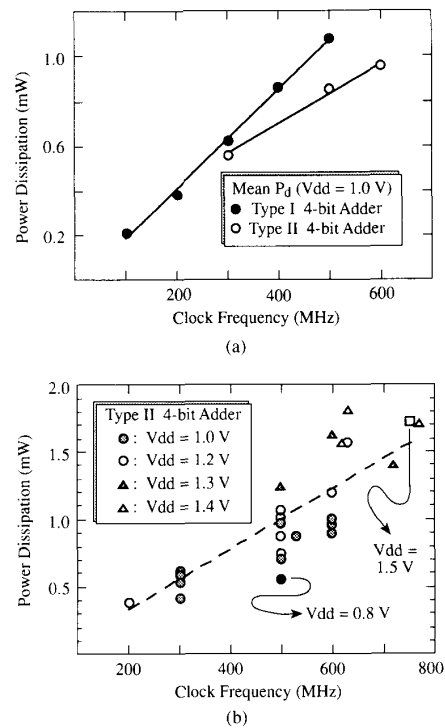


Fig. 10. (a) Mean power dissipation versus frequency for type I and type II TDFL adders with V_{dd} of 1.0 V, and (b) scatter plot of power dissipation versus frequency of type II adder.

though further quantification of this was difficult because of the difficulty of synchronizing all chip inputs. Increasing V_{dd} above 1.3 V gave no further improvement in performance. With a clock amplitude of 1.5 V, the adder operated over a

TABLE I
COMPARISON OF GaAs 4-b ADDRESS

Logic Family	Area (mm ²)	Gate Count	P _D (mW)	Max Clock Frequency (MHz)
TDFL				
Type I	0.25	116	2.4	740
Type II	0.16	68	1.7	770
DCFL[7]	0.32	62	47	714
BFL[7]	0.75	62	190	500
CCDL[7]	0.70	28	96	900
TTDL[8]	0.55	15	130	1250

CCDL - Capacitively Coupled Domino Logic.

TTDL - Trickle Transistor Dynamic Logic.

dc clock offset range of -466 to -663 mV on average. As expected, the power dissipation and the maximum frequency of operation increased as the dc level of the clock was made less negative. The reason for these trends can be understood by considering Fig. 1. During the precharge phase of a TDFL gate's operation, increased clock high potentials enable faster charging of a gate's output (through $Q4$ and $Q8$) and faster charge transfer through the gate's input pass transistors ($Q1$ and $Q5$). In the evaluate phase, a greater clock high potential decreases the series resistance in the pull-down path ($Q3$ and $Q7$). At 400 MHz the mean power dissipation was $790 \mu\text{W}$ when the clock dc level was -700 mV and was $976 \mu\text{W}$ for a dc level of -550 mV.

The data in Table I compare the results of this work to 4-b adders designed in other GaAs logic families. In comparing the TDFL adder results to the others listed in Table I, recall that the TDFL adders are fully pipelined, whereas the other adders listed have at most one stage of pipelining. If adders made with the other logic families had more stages of pipelining, they would likely have higher maximum frequencies of operation. They would also dissipate more power, however, and would be correspondingly larger. The maximum frequencies of operation of the non-TDFL adders listed in Table I were obtained from their measured or predicted critical path delay. Capacitively coupled domino logic [7] (CCDL) and trickle transistor dynamic logic [8] (TTDL) are also dynamic logic families. Both, however, incorporate static inverters and, in the case of TTDL, static level shifters, so they dissipate static power. For two other points of comparison, a 1-b DCFL full adder in the Vitesse Semiconductor cell library dissipates 4.8 mW and has a critical delay (A/B to sum) of 836 ps [9] while a 1-b full adder in the VTI 1.0- μm CMOS process dissipates $58 \mu\text{W}/\text{MHz}$ and has a critical delay (carry to sum) of 1.59 ns [10].

To make a fair comparison of the power dissipation of TDFL to other logic families, the power dissipated by the clock drivers needed to operate the adder should be included. The capacitive load presented by the adder to each clock is approximately 600 fF. A two-phase clock generator and driver circuit has been designed which dissipates 52 mW when driving 10 pF (on each clock line) at 500 MHz. Using a scaled-down version of this generator/driver circuit, an additional 3.1 mW would be added to the 1.1 mW dissipated from V_{dd} . In

terms of power/megahertz/gate, this works out to be only 72 nW/MHz/gate. For comparison with a representative silicon VLSI technology of the same gate length and under similar loading, static, 5-V CMOS gates dissipate approximately $1 \mu\text{W}/\text{MHz}$ (assuming 20 fF of load on each gate) [4].

B. Variable Modulus Prescaler

The variable modulus prescaler was tested using Cascade probes. The two clock signals and the initialization signal were provided from a 10-Gb/s pattern generator. Differential 50% duty cycle clock signals were used rather than nonoverlapping clock signals. By periodically initializing the prescaler, the initialization signal could be used for triggering the oscilloscope. In this way, the phase during which the prescaler samples the mode select pins, resets and initializes the ring for a new modulus, and enables the output, could be monitored.

Testing was performed using $V_{dd} = 1.0$ V. The clock dc level and amplitude were varied by using a fixed clock low level of -1.2 V and varying the high level from 0 to $+0.5$ V. As expected, the maximum speed of operation of the prescaler increased with increasing clock high level. With a clock high level of 0.0 V, the maximum speed of operation of the prescaler was 400 MHz, while 850-MHz operation was obtained when the clock high level was 0.5 V.

Fig. 11 shows prescaler operation at 850 MHz for three different moduli (divide by 3, 9, and 31). Notice the initialization phase in the top two plots of Fig. 11. During initialization, the output is disabled (forced low), and 13 clock periods later, the new modulus is observed on the output. This latency (from when the initialization is activated until the output is present) and the associated phase noise might be unacceptable in some applications. However, a prescaler design that uses the same architecture with roughly double the circuit complexity could switch between moduli in one to two clock cycles.

The power dissipation versus frequency was measured for three different clock high levels (0, $+0.2$, $+0.3$ V). These data are plotted in Fig. 12. The power dissipation exhibits a linear dependence on frequency as seen from the least square linear fits. As expected, the dynamic power dissipation (slope) increases with the clock high level from 1.7 mW/MHz at 0 V to 2.3 mW/MHz at $+0.3$ V. With 166 TDFL gates on the chip, this corresponds to less than 14 nW/MHz/gate. The average dc intercept representing the static power dissipated in the DCFL and SBFL gates is 6.2 mW, which corresponds to less than $80 \mu\text{W}/\text{gate}$. As with the 4-b adder, this demonstrates that very low-power static gates can be used in conjunction with TDFL for high-speed circuits. When operating at 850 MHz, the prescaler dissipated 9.2 mW. The output buffer dissipates 7 mW (unloaded), and 32 mW when driving a 50- Ω load, and produces ECL levels. The operation of the prescaler compares favorably with a divide-by-1 to -16 prescaler implemented with GaAs enhancement/depletion-mode differential pass-transistor logic, which dissipated 15.7 mW and operated up to 1 GHz [11]. The power dissipation of the prescaler also compares favorably with silicon bipolar prescalers designed to operate in the same frequency range (significantly more than 100 mW [12] for 1-GHz operation—four moduli) and

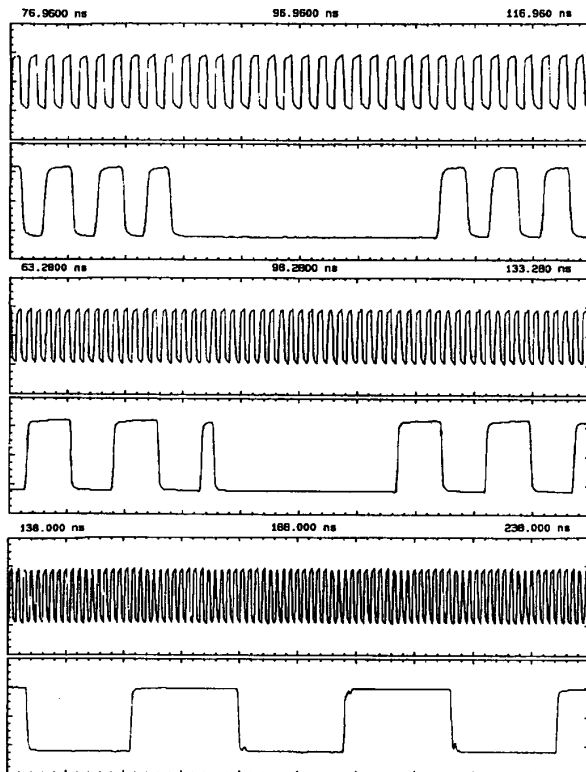


Fig. 11. Prescaler operation at 850 MHz. Associated input and output waveforms are shown for three different division moduli. Top to bottom: divide by 3, 9, and 31. Initialization sequence disable output in divide-by-3 and -9 plots. Vertical scale in each: 1.0 V/div for clock trace, 400 mV/div for output trace.

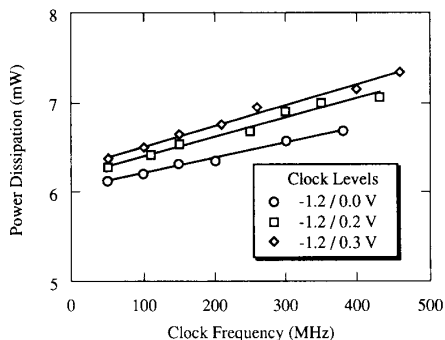


Fig. 12. Prescaler power dissipation versus frequency with clock high level as parameter.

with GaAs MESFET prescalers composed entirely of static logic gates (about 500 mW [13] for 2-GHz operation—eight moduli; see also [10]).

The prescaler operated at V_{dd} supply levels ranging from 850 mV to 2 V. The fastest operation was obtained for $V_{dd} = 1.3$ V.

V. CONCLUSION

In summary, this work demonstrates the operation of TDFL circuits of MSI complexity at clock frequencies close to a

gigahertz. A variable modulus prescaler which divides by all integers from 2 to 31 was shown to operate at 850 MHz and dissipate only 9.2 mW. Operation of 4-b TDFL adders at 500 MHz with less than 1 mW of power dissipation and at 750 MHz with 1.7 mW was demonstrated. The TDFL gates in these circuits were shown to dissipate only 14 to 20 nW/MHz/gate (approximately 50 times less than static 5-V CMOS). This work confirms that low-power static gates can be used in conjunction with TDFL gates to obtain high-frequency performance. Additionally, this work verifies the operation of three- and four-input TDFL gates and a TDFL 11-transistor EXCLUSIVE NOR gate in MSI circuits.

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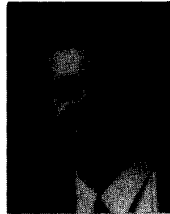
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