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Nielsen, Jannik Hammel; Bruun, Erik

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A LOW-POWER 10-BIT CONTINUOUS-TIME CMOS ΣΔ A/D CONVERTER

Jannik Hammel Nielsen and Erik Bruun

Ørsted•DTU, Technical University of Denmark
DK-2800 Kgs. Lyngby, Denmark
jhn@oersted.dtu.dk

ABSTRACT

This paper presents the design of a third order low-pass ΣΔ analog-to-digital converter (ADC) employing a continuous-time (CT) loop filter. The loop filter is implemented using $G_{\mathrm{m}} - C$ integrators, where the transconductors are implemented using CMOS transistors only. System level as well as transistor level design issues for power efficiency is discussed. A prototype ΣΔ ADC intended for weak biological signals restricted to bandwidths below $4\,\mathrm{kHz}$ has been manufactured in a standard $0.35\,\mu\mathrm{m}$ CMOS technology. The ADC has a measured resolution of 10 bits and a dynamic range (DR) of 67 dB at a sampling rate of $f_{\mathrm{s}} = 1.4\,\mathrm{MHz}$, while drawing a bias current of $60\,\mu\mathrm{A}$ from a modest supply voltage of $1.8\,\mathrm{V}$, thus consuming $108\,\mu\mathrm{W}$ of power.

1. INTRODUCTION

The last few decades has seen a rapidly growing interest in the implementation of systems-on-chip for sensing, recording and processing of various physical signals, ranging from micromachined silicon sensor readouts to biological signals. A typical configuration for these systems consists of an analog frontend for preprocessing the often weak signal input followed by an A/D converter leaving the signal for further digital processing. As many of these systems are designed for portability, low power consumption of the system components is crucial.

In this paper we propose a continuous-time ΣΔ A/D converter suitable for quantizing preamplified nerve signals recorded by cuff-electrodes. The main energy of human nerve signals lie in the frequency band $400\,\mathrm{Hz} < f_{\mathrm{sig}} < 4\,\mathrm{kHz}$ and has a typical maximum amplitude of $\pm 10\,\mu\mathrm{V}$ [1]. A preamplifier which brings the nerve signal to $\pm 100\,\mathrm{mV}$ has previously been implemented and is reported in [2].

CT loop filters hold several advantages over their discrete-time counterparts. As the sampler is located deep inside the modulator loop, implicit anti-aliasing is provided by the CT loop filter. Furthermore, the gain-bandwidth-product (GBW) of the active element in the CT loop filter can be significantly lowered compared to traditional switch-capacitor implementations for a given sampling frequency implying power savings [3]. The drawbacks of using a CT loop filter is increased sensitivity to clock jitter and loop delay.

For low power implementation of ΣΔ-modulators, the single-loop architecture as shown in fig.1 is preferred, as only the first integrator in the loop has strict requirements imposed on it. The requirements for the remaining integrators can be relaxed as all internal nodes are filtered to the output.

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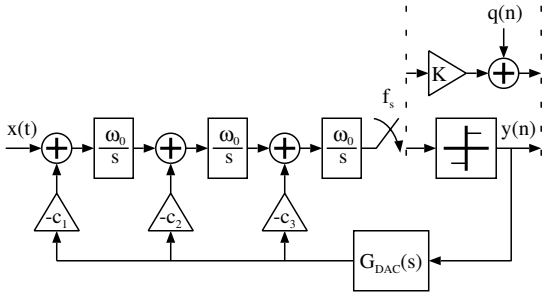


Fig. 1. Continuous-time 3^{rd}order ΣΔ- modulator block diagram.

2. CT ΣΔ-MODULATOR SYSTEM DESIGN

As shown in fig. 1, the quantizer is modelled by a gain factor K and an additive white noise source $q(n)$. The feedback DAC is a NRZ zero-order hold waveform and the s-domain transfer function of the DAC is given by: $G_{\mathrm{DAC}}(s) = [1 - \exp(-sT)]/s$. The overall loop filter function can be written:

$$H(s) = \sum_{n=1}^{3} c_{\mathrm{n}} \left(\frac{\omega_0}{s}\right)^n G_{\mathrm{DAC}}(s) \tag{1}$$

The signal transfer function (STF) and noise transfer function (NTF) from a loop-filter perspective are respectively:

$$\mathrm{STF}(s) = \frac{KH(s)}{1 + KH(s)} \approx 1, \quad \mathrm{NTF}(s) = \frac{1}{1 + KH(s)} \tag{2}$$

By choosing an appropriate NTF, e.g. a butterworth highpass filter, the feedback coefficients can be derived [3].

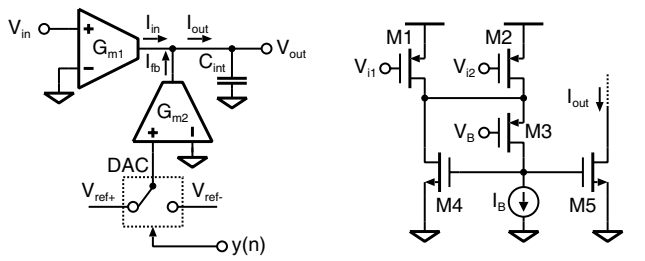
ΣΔ-modulators are characterized by having a maximum stable input amplitude (MSA), which will cause the modulator to become unstable when exceeded. The MSA is inversely proportional to the loop filter order and cutoff frequency ω_0, i.e. the more aggressively we high-pass filter the quantization noise, the less signal power can be applied while maintaining stable operation [3].

For a given quantization noise power σ_{q}^2, the inband quantization noise power for a channel $[f_{\mathrm{low}};\ f_{\mathrm{high}}]$ can be found:

$$P_{\mathrm{Q}} = \frac{\sigma_{\mathrm{q}}^2}{f_{\mathrm{s}}} \int_{f_{\mathrm{low}}}^{f_{\mathrm{high}}} \left| \frac{1}{1 + KH\left(e^{j2\pi f}\right)} \right|^2 df \tag{3}$$

The resulting maximum signal-to-quantization-noise-ratio (SQNR) at the MSA is then:

$$\mathrm{SQNR} = 10 \log \left(\frac{\mathrm{MSA}^2}{P_{\mathrm{Q}}} \right) \tag{4}$$



(a) Integrator block diagram (b) Transconductor schematic

Fig. 2. Continuous-time integrator with feedback and corresponding single-ended dual input transconductor MOST schematic.

The optimum loop filter order, sampling frequency and loop filter cut-off frequency ω_0, with regards to minimizing the power consumption for a required SQNR can be found by using the design methodology described in [3]. For 10 bits performance for our given bandwidth, a third order loop filter with a cut-off frequency of $80\,\mathrm{kHz}$ and a sampling frequency of $1.4\,\mathrm{MHz}$ was found to be optimal as a second order filter would require a high sampling frequency, whereas a fourth order filter would degrade stability.

3. IMPLEMENTATION

3.1. Transconductor Core

The integrators were implemented as $G_\mathrm{m} - C$ structures. A principle block diagram of an integrator is shown in fig. 2(a), where the integrator is shown in a single-ended version for simplicity. The integrator unity-gain frequency is given by $\omega_0 = G_{\mathrm{m}1}/C_{\mathrm{int}}$. The integrator employs two transconductors for the signal input and the modulator DAC feedback respectively. The feedback DAC function is implemented by letting the ADC output $y(n)$, control a switch selecting either a positive or negative voltage reference $V_{\mathrm{ref+/-}}$. The feedback factor is determined by $c = G_{\mathrm{m}2}/G_{\mathrm{m}1}$.

The two transconductors employed in an integrator were implemented in a single MOST-only structure by using an extended version of the transconductor introduced in [4], shown in a single-ended version in fig. 2(b). The transconductors $G_{\mathrm{m}1}$ and $G_{\mathrm{m}2}$ of fig. 2(a) are realized by biasing M1 and M2 in the triode region thus realizing a two-input transconductor. The drain voltage of M1 and M2 is set by the bias voltage V_B and held constant through the negative feedback loop comprising M3 and M4. Hence, the source node of M3 constitutes a virtual ground node well suited for current summing. M3 is biased in weak inversion to maximize the $g_\mathrm{m}/I_\mathrm{D}$-ratio whereas all other MOSTs are biased in strong inversion for good matching. The signal currents produced by M1 and M2 are thus sensed by M3 resulting in a voltage change at the gate of M4 modulating the M4 current i_DS. The summed signal current is accessed through M5 which mirrors the M4 i_DS.

Using the EKV-model, the drain current for a PMOST biased in the triode region is given by [5]:

$$I_\mathrm{D} = K_\mathrm{P}^{'}\,(W/L)\Big[V_\mathrm{G} - V_{\mathrm{th,p}} + \frac{n}{2}\,(V_\mathrm{D} - V_\mathrm{S})\Big](V_\mathrm{D} - V_\mathrm{S}) \quad (5)$$

where $V_{\mathrm{th,p}}$ is the threshold voltage, n is the slope factor and all terminal voltages are referred to the bulk. Eq. (5) is valid for $V_\mathrm{G} - V_{\mathrm{th,p}} \leq n\,(V_\mathrm{D} - V_\mathrm{S})$. From eq. (5) it is seen that the drain current varies linearly with the gate voltage if the drain-source voltage is held constant. The transconductance of M1 and M2 constituting $G_{\mathrm{m}1}$ and $G_{\mathrm{m}2}$ in the overall dual input transconductor is equal to the triode region small-signal transconductance:

$$G_{\mathrm{m,single}} = g_\mathrm{m} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}} = K_\mathrm{P}^{'}\,(W/L)\,(V_\mathrm{D} - V_\mathrm{S}) \quad (6)$$

From eq. (6) we see that the transconductance is tunable by regulating the drain-source voltage enabling us to tune the loop filter cut-off frequency ω_0 to the desired frequency.

The necessary bias current of the transconductor core is determined by the speed requirements of the negative feedback loop. An approximate expression for the loop GBW is given by: $\mathrm{GBW} = g_{\mathrm{m}4}/(2c_{\mathrm{gs}4} + c_{\mathrm{gd}3} + c_{\mathrm{IB}})$. Voltage excursions on the drain of M1 and M2 will result in modulation of the transconductor output current given by: $\Delta i_{\mathrm{ds}1,2} = \Delta v_{\mathrm{ds}1,2}\,(g_{\mathrm{ds}1} + g_{\mathrm{ds}2})$. The amplitude of the voltage excursions is given by regulated impedance seen at the source node of M3 Z_x. An approximate expression for this impedance for frequencies greater than the loop 3dB frequency is:

$$Z_\mathrm{x}(\omega) \approx \frac{\omega}{g_{\mathrm{m}3}\mathrm{GBW}} \quad (7)$$

From eq. (7), we see that the impedance can be lowered by increasing the loop GBW and $g_{\mathrm{m}3}$, hence giving us the required bias current necessary for a given input frequency.

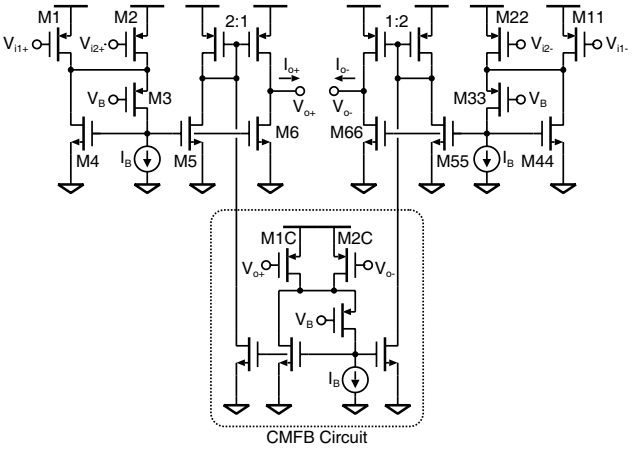


Fig. 3. Fully differential dual-input transconductor including CMFB circuit.

3.2. Differential Transconductor

A fully differential version of the dual-input transconductor can be easily realized by duplicating the circuit of fig. 2 as shown in fig. 3. Common mode stabilization is achieved by including a common-mode-feedback (CMFB) circuit which is constructed by replicating the transconductor core as seen in fig. 3. Output common-mode voltage deviation is sensed by M1C and M2C which injects current through the 2:1 mirrors to correct the output voltage. The aspect ratio of M1C and M2C are set equal to half the aspect ratio sum of M1 and M2. So we have $W_{1\mathrm{C}} = W_{2\mathrm{C}} = (W_1 + W_2)/2$, hereby ensuring that the correct common-mode level is set for the succeeding integrator.

The 2:1 mirrors employed by the CMFB circuit will also half the small signal current, hence the differential transconductor has

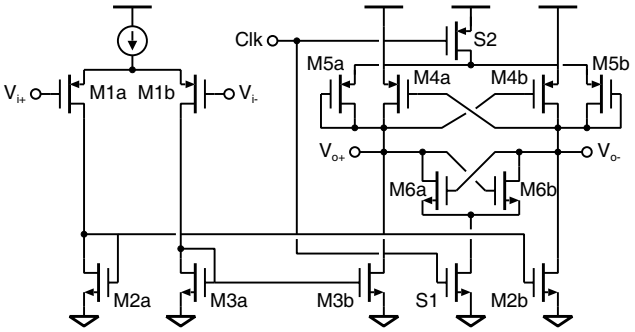


Fig. 4. Comparator schematic.

transconductance equal to half the single-ended version:

$$G_{\mathrm{m,diff}} = 1/2 G_{\mathrm{m,single}} = 1/2 g_{\mathrm{m1}} \tag{8}$$

Due to the filtering of the internal nodes in the loop filter, the requirements for the 2nd and 3rd transconductors can be relaxed. A summary of the transconductor performances is given below:

	$I_{\mathrm{B}}\,[\mu\mathrm{A}]$	Reg. GBW [MHz]	DC-gain A_0[dB]
G_1	3	10	61
G_2	1.25	4.5	61
G_3	0.75	2.7	48

3.3. Comparator

As the quantizer in the ADC modulator consists of a single bit, a comparator suffices. A schematic of the realized comparator is shown in fig. 4. It consists of a preamplifier stage and a track and latch output stage. During the low state of the clock, the M6 positive feedback pair is switched off and the M5 pair is switched on. The loop gain around the M4 and M5 pairs is in this case <1 and the comparator operates in track mode with a gain given by:

$$A_{\mathrm{V}} = \frac{v_{\mathrm{o}}}{v_{\mathrm{i}}} = g_{\mathrm{m1}} \frac{g_{\mathrm{m4}} + g_{\mathrm{m5}}}{g_{\mathrm{m5}}^2 - g_{\mathrm{m4}}^2} \approx \frac{g_{\mathrm{m1}}}{g_{\mathrm{m5}}} \tag{9}$$

As the clock goes high, switch S2 turns off and the loop gain around the M4 pair is now >1. Switch S1 turns on enabling the M6 positive feedback pair and the comparator output is latched. A digital set-reset latch succeeds each of the comparator outputs in order to restore the output to full digital levels.

3.4. Capacitor dimensioning

A figure of merit for transconductors is the noise-excess-factor (NEF) which is defined as the ratio of transconductor output thermal noise conductance to the transconductance:

$$\mathrm{NEF} = \frac{\mathrm{G_{N,out}}}{G_{\mathrm{m}}} \tag{10}$$

For the employed transconductor, the NEF can be shown to be [4]:

$$\mathrm{NEF} = \frac{g_{\mathrm{ds1}}}{g_{\mathrm{m1}}} \left(1 + \frac{g_{\mathrm{ds1}}}{g_{\mathrm{m3}}} \right) + 2\frac{g_{\mathrm{m4}}}{g_{\mathrm{m1}}} + \frac{g_{\mathrm{m,IB}}}{g_{\mathrm{m1}}} \tag{11}$$

The thermal noise accumulated on the integrating capacitor is:

$$P_{\mathrm{Th}} = \frac{\mathrm{NEF} \cdot kT}{C_{\mathrm{int}}} \tag{12}$$

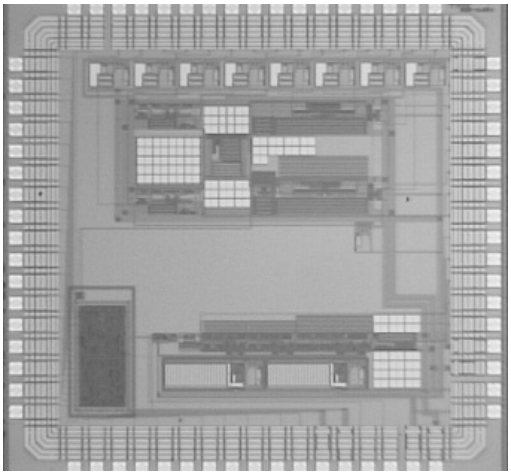


Fig. 5. Chip die microphotograph.

Referred to a given reference voltage V_{ref}, the total amount of noise allowable for a resolution of b bits is given by:

$$P_{\mathrm{N}} = \frac{(\mathrm{MSA} \cdot V_{\mathrm{ref}})^2}{2 \cdot 10^{(6.02b+1.76)/10}} \tag{13}$$

We have previously derived an expression for the inband quantization noise eq. (3). Combining equations (12-13) and eq. (3), we can solve for the minimum allowable capacitor size:

$$C_{\mathrm{int}} = \mathrm{NEF} \cdot kT \left[\frac{(\mathrm{MSA} \cdot V_{\mathrm{ref}})^2}{2 \cdot 10^{(6.02b+1.76)/10}} - P_{\mathrm{Q}} \right]^{-1} \tag{14}$$

The noise filtering of the intenal nodes allows for smaller capacitors in the 2nd and 3rd integrators. The implemented capacitor sizes are given below:

	C_1	C_2	C_3
Cap. size [pF]	7.5	1.75	1.25

4. MEASUREMENTS

The circuit was implemented in a standard $0.35\,\mu\mathrm{m}$ CMOS process. A chip microphotograph is shown in fig. 5, where the $\Sigma\Delta$-modulator is contained in the lower half of the chip.

An example output spectrum is shown in fig. 6, for an input tone at $1.3\,\mathrm{kHz}$ with an amplitude of $0.8 V_{\mathrm{ref}}$. The second harmonic is seen to dominate the spurious performance, which is most likely caused by mismatches between the positive and negative signal paths.

Fig. 7 shows the measured signal-to-noise-plus-distortion ratio (SNDR) for two different tone frequencies versus the normalized input signal $V_{\mathrm{in}}/V_{\mathrm{ref}}$ for one of the test chips. Though the harmonic performance is unexpectedly dominated by the second harmonic we still achieve a max. SNDR of approx. $62\,\mathrm{dB}$ at the low tone frequency at $340\,\mathrm{Hz}$, which deteriorates to approx. $56\,\mathrm{dB}$ for the higher tone frequency at $1300\,\mathrm{Hz}$. The average max. SNDR over the ten test chips for an input tone of $1864\,\mathrm{Hz}$ was measured at $58.4\,\mathrm{dB}$.

The measured average current drawn in the ten test chips is $60\,\mu\mathrm{A}$ from a $1.8\,\mathrm{V}$supply giving an average power consumption of $P = 108\,\mu\mathrm{W}$, excluding bias circuitry and input buffers.

	This work	[6]	[7]	[8]	[9]
Power Dissipation [μW]	108	135	950	340	40
Signal Bandwidth [kHz]	3.6	25	25	8	16
Sampling Frequency [MHz]	1.4	2.4	5	1.024	1.538
Peak SNDR [dB]	62	70	85	69	62
$V_{\rm DD} - V_{\rm SS}$ [V]	1.8	1.5	1	1.95	0.9
Dynamic Range [dB]	67	80	88	73	77
Technology	$0.35\,\mu$m CMOS	$0.5\,\mu$m CMOS	$0.35\,\mu$m CMOS	$1.2\,\mu$m CMOS	$0.5\,\mu$m CMOS

Table 1. Measured performance summary of the third order $\Sigma\Delta$-modulator and comparison with prior work.

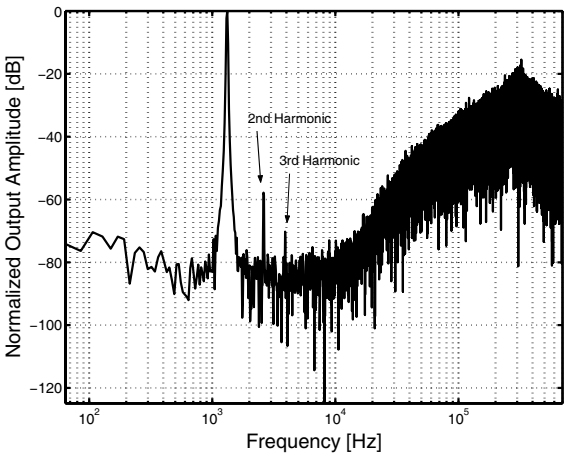


Fig. 6. Measured output spectrum.

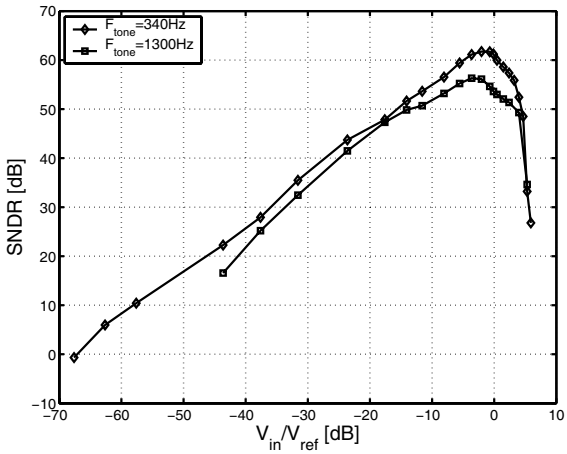


Fig. 7. SNDR for two different input tone frequencies.

The measured performance of the circuit is summarized in table 1 together with results of recent similar work.

5. CONCLUSION

A low-power CT ADC has been implemented using $G_{\rm m} - C$ integrators. The transconductors were implemented using MOST only, whereas the integrating capacitors were implemented as poly-poly capacitors. However as all capacitors are grounded, poly-well capacitors are feasible for a MOST only implementation of the ADC thus making it suitable for implementation in pure digital CMOS standard processes. Comparison with prior work shows that CT loop-filters are a good alternative to switch-capacitor DT loop-filters for low-power $\Sigma\Delta$ ADCs. The transconductor employed is reported operational at a supply of 1.2 V in a $0.18\,\mu$m technology [4], implying that sub $75\,\mu$W operation of the ADC could be achieved.

6. REFERENCES

[1] J. Struijk et al., "Cuff electrodes for long-term recording of natural sensory information," *IEEE Eng. in Medicine and Biology*, vol. 18, pp. 91–98, 1999.

[2] J. H. Nielsen and T. Lehmann, "An implantable CMOS amplifier for nerve signals," *Analog Int. Circuits and Signal Proc.*, vol. 36, pp. 153–164, 2003.

[3] J. H. Nielsen and E. Bruun, "A design methodology for power-efficient continuous-time sigma-delta a/d converters," in *Proc. Int. Symp. on Circuits and Systems*. IEEE, 2003, vol. 1, pp. 1069–1072, IEEE.

[4] U. Yodprasit and C. Enz, "A 1.5V 75-dB dynamic range third-order Gm-C filter integrated in a standard 0.18-μm standard digital CMOS process," in *Proc. European Solid-State Circuits Conference*, 2002, pp. 647–650.

[5] C. Enz et al., "An analytical CMOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Int. Circuits and Signal Proc.*, vol. 8, pp. 83–114, 1995.

[6] F. Gerfers et al., "A 1.5V 12-bit power-efficient continuous-time third-order $\Sigma\Delta$ modulator," *IEEE Journal of Solid-State Circ.*, vol. 38, pp. 1343–1352, 2003.

[7] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Sigma\Delta$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE Journal of Solid-State Circ.*, vol. 36, pp. 349–355, 2001.

[8] S. Au and B. H. Leung, "A 1.95-V, 0.34-mW, 12-b sigma-delta modulator stabilized by local feedback loops," *IEEE Journal of Solid-State Circ.*, vol. 32, pp. 321–328, 1997.

[9] V. Peluso et al., "A 900-mV low power $\Sigma\Delta$ A/D converter with 77-dB dynamic range," *IEEE Journal of Solid-State Circ.*, vol. 33, pp. 1887–1897, 1998.