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A DESIGN METHODOLOGY FOR POWER-EFFICIENT CONTINUOUS-TIME ΣΔ A/D CONVERTERS

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ABSTRACT

In this paper we present a design methodology for optimizing the power consumption of continuous-time (CT) ΣΔ A/D converters. A method for performance prediction for ΣΔ A/D converters is presented. Estimation of analog and digital power consumption is derived and employed to predict the most power efficient configuration of a CT single-loop ΣΔ ADC. Finally, a 10 bit prototype converter is optimized and simulated using a 0.35 μm CMOS technology. The simulation results of the prototype 1.8 V converter show a SNR better than 65 dB and a spurious-free dynamic range of more than 63 dB, consistent with 10 bits performance. Expected power consumption for the prototype is approx. 170 μW.

1. INTRODUCTION

Todays trend toward high portability of everyday electronic devices ranging from telecommunication to biomedical devices, constitutes a major design challenge. The need for high durability of battery-powered devices coupled with ever-increasing performance requirements only enhances the need for low-power solutions. Another factor is the decreasing voltage supply driven by technology scaling. This is due to the fact that low-voltage operation of analog circuits requires high power consumption in order to retain sufficient dynamic range.

An important building block in many devices is the A/D converter (ADC). Of the many possible variations of ADC topologies, the ΣΔ-modulator type remains highly interesting. This topology offers an elegant way to obtain high resolution for low- to moderate input frequencies and yet still maintain modest requirements for the analog building blocks. In the past decade, this ADC topology has shown it's robustness through many implementations using the discrete-time (DT) switched-capacitor (SC) technique. However as supply voltages decrease with technology scaling, the SC technique is becoming less viable.

CT implementations holds promise of lower power consumption and are less dependent on supply scaling than their DT counterparts. The price paid is increased sensitivity towards e.g. clock jitter and other non-idealities.

2. CT ΣΔ-MODULATORS

Employing a CT loop-filter for the ΣΔ ADC realisation holds several advantages. As the sampler is located deep in the loop, implicit anti-aliasing (AA) is native to the CT ΣΔ ADC, often making an explicit AA-prefilter redundant. The necessary gain-bandwidth (GBW) of the integrators is typically a factor of 3 lower than their DT counterparts [2] for a given sampling frequency f_s.

These properties imply that a significantly lower power consumption can be achieved by using a CT loop-filter over the DT counterpart.

A single-loop CT ΣΔ ADC of order N is shown in fig. 1. This configuration is well suited for low-power as only the first integrator has stringent requirements imposed on it. This is due to the filtering from all other internal nodes to the output. The quantizer is sampled at f_s from which we can define the oversampling ratio: OSR $= f_s/2f_b$, where f_b is the baseband frequency.

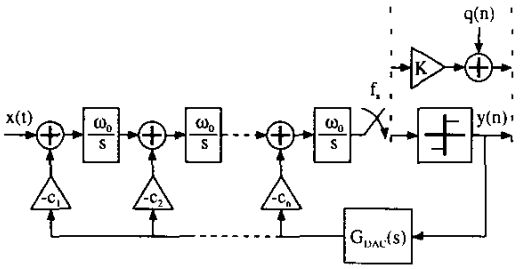
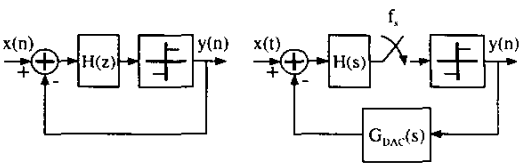


Figure 1: Continuous-Time ΣΔ-modulator.



(a) DT Feedback Filter (b) CT Feedback Filter

Figure 2: Feedback filters in DT and CT modulators.

2.1. DT to CT Mapping

In order to be able to obtain fast and yet precise simulation of the CT ADC performance, a DT/CT equivalence can be established. This also allows us to use the design methods usually employed for DT ΣΔ ADCs. In fig. 2, a linear model of the ADC is shown from a loopfilter perspective in both a DT and CT version. The

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N	
2	$\left(\frac{\omega_0}{f_s}\right)^2 \left\{c_1 = \frac{d_1+d_2}{2},\ c_2 = d_1 + d_2\right\}$
3	$\left(\frac{\omega_0}{f_s}\right)^3 \left\{c_1 = \frac{2d_1-d_2+2d_3}{6},\ c_2 = d_3 - d_1,\ c_3 = d_1 + d_2 + d_3\right\}$
4	$\left(\frac{\omega_0}{f_s}\right)^4 \left\{c_1 = \frac{3(d_4-d_1)+d_2-d_3}{12},\ c_2 = \frac{11(d_1+d_4)-d_2+d_3}{12},\ c_3 = \frac{3(d_4-d_1)+d_3-d_2}{2},\ c_4 = \sum_{n=1}^{4} d_n\right\}$

Table 1: Mapping of DT to CT filter coefficients.

signal transfer function (STF) and noise transfer function (NTF) for fig. 2(a) are respectively:

$$\mathrm{STF}(z) = \frac{KH(z)}{1+KH(z)} \approx 1, \quad \mathrm{NTF}(z) = \frac{1}{1+KH(z)} \quad (1)$$

An often used approach for the design of $\Sigma\Delta$-modulators is to choose a desired NTF (e.g. butterworth etc.) [1]. From the NTF, the feedback filter $H(z)$ can be derived, determining the feedback coefficients. Since the CT modulator in fact constitutes a sampled system, a CT feedback filter equivalent to the DT filter can be obtained by requiring that the outputs are equal at the sampling instant. Referring to fig. 2, we thus have that:

$$H(z) = \mathcal{Z}\left\{H(s)G_{\mathrm{DAC}}(s)\right\} = \widehat{H(z)} \quad (2)$$

where $H(s)G_{\mathrm{DAC}}(s) = \widehat{H(s)}$, constitutes the combined feedback filter. Assuming a zero-order-hold feedback DAC with a NRZ feedback waveform, the s-domain transfer function of the DAC is: $G_{\mathrm{DAC}}(s) = [1 - \exp(-sT)]/s$. For a single-loop modulator of order N, the CT and DT feedback filters can be written respectively:

$$H(s) = \sum_{n=1}^{N} c_n \left(\frac{\omega_0}{s}\right)^n, \quad H(z) = \sum_{n=1}^{N} d_n z^{-1} \left(\frac{z}{z-1}\right)^n \quad (3)$$

Taking the z-transform of each order of $H(s)$ can be shown to be:

$$\mathcal{Z}\left\{H(s)\right\} = \sum_{n=1}^{N} \frac{c_n (\omega_0 T)^n}{n!} \frac{B_n(z)}{(1-z^{-1})^n} \quad (4)$$

where $B_n(z)$ is a polynomial in z of order n. By comparing the coefficients of z in $\widehat{H(z)}$ and $H(z)$, a set of linear equations result from which the mapping between the DT d-coefficients and the CT c-coefficients can be established. In table 1, the mapping for modulators of orders 2 through 4 is given.

2.2. Performance Prediction

The quantizer in the $\Sigma\Delta$ constitutes a highly nonlinear element. As shown in fig. 1, the quantizer can be modelled as a gain factor K, and an additive noise source $q(n)$.

In [1] a quasilinear model of the 1-bit quantizer is proposed. If a signal with a sufficiently high amplitude is applied at the modulator input, the modulator will become unstable. The maximum stable amplitude (MSA) can be shown to be a function of the feedback filter cut-off frequency f_c. Assuming a heavily oversampled input signal, the output power: $\sigma_y^2 = 1 - m_y$, can be attributed

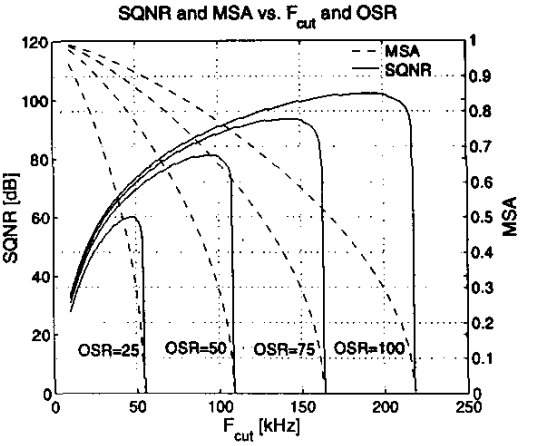

Figure 3: SQNR and MSA in a a 3rd order $\Sigma\Delta$ ADC vs. f_c for increasing OSR.

solely to the quantization noise σ_q^2. Hence we can define a noise amplification factor, $A(K)$ [1]:

$$A(K) = \frac{1-m_y^2}{\sigma_q^2} = \int_0^{\pi} \left|\mathrm{NTF_K}\left(e^{j\omega}\right)\right| d\omega = \sum_{n=1}^{\infty} \left|\mathrm{ntf_K}(n)\right|^2 \quad (5)$$

where Parseval's theorem has been used to obtain the time-domain representation. m_y is the mean of the modulator output. Due to the high feedback filter gain, we have that $m_x \approx m_y$.

As the quantization noise is in fact not an independent signal source, but generated by the input signal itself, we can estimate σ_q^2 from m_x and the quantizer input probability density function (PDF) [1]. For higher order modulators (N>2), the quantizer input is well approximated by a gaussian PDF. For a gaussian PDF, we have [4]:

$$\sigma_q^2 = 1 - m_y^2 - \frac{2}{\pi} \exp\left[-2\left(\mathrm{erf}^{-1}(m_y)\right)^2\right] \quad (6)$$

where erf^{-1}, is the inverse error function.

As the lowest amount of quantization noise is attained at the MSA, the minimum value of $A(K)$ yields the MSA. Hence by combining eq. (5-6) we can obtain an estimate of the MSA .

However, as $A(K)$ is an increasing function of the NTF cut-off frequency [1], the MSA is inverserly proportional to f_c and hence a trade-off exists between a high f_c, i.e. high quantization noise supression, and a high MSA, i.e. high signal power.

Due to the intrinsic minimization of the quantization noise, an equilibrium quantizer gain K_{eq}, can be estimated by the K which minimizes $\|\mathrm{ntf_K}\|_2^2/K^2$. The obtained K_{eq} determines both $\mathrm{NTF_K}(z)$ and $A(K)$. From eq. (5), the quantization noise for zero input can be found: $\sigma_q^2 = 1/A(K_{eq})$. For a base-band frequency of f_b, the signal to quantization-noise ratio (SQNR) for a sinusoid at MSA can be estimated:

$$\mathrm{SQNR} = \frac{\mathrm{MSA}^2}{2A(K_{eq})f_s} \int_0^{f_b} \left|\frac{1}{1+K_{eq}H(e^{j\omega})}\right|^2 df \quad (7)$$

In fig. 3 the predicted MSA and SQNR for a third order $\Sigma\Delta$ is shown vs. f_c for different OSRs. The abrupt drop-off of the SQNR

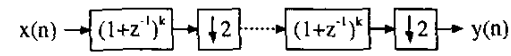

Figure 4: FIR2 combfilter structure.

curves occur as the MSA approaches zero. From fig. 3, it is seen that the maximum SQNR is obtained at a MSA of approx. 0.3. This low value is due to the fact that the noise suppression grows "faster" for increasing f_c than the MSA decreases.

2.3. Decimation filter

A popular choice for decimation filters is the combfilter which can be implemented without using computationally expensive multipliers. The combfilter transfer function is given by [3]:

$$H_{\mathrm{com\,b}}(z) = \left(\frac{1-z^{-D}}{1-z^{-1}}\right)^k = \prod_{n=0}^{\log_2 D-1}\left(1+z^{-2^n}\right)^k \qquad (8)$$

where D is the decimation factor and k is the order of the filter. The second form of eq. (8) can be implemented by a series of FIR filters each decimating by a factor of two as shown in fig. 4.

The wordlength of the registers at the ouput of each FIR stage is equal to $(W_0 + ki)$ bits, where W_0 is the number bits at the filter input. Hence we have a filter configuration where the full sampling frequency is only applied to the first stage, which only has a wordlength of a few bits. Whereas the other stages, with increasing wordlength, are clocked at decimated frequencies giving a power-efficient decimation filter [3]. For a $\Sigma\Delta$-modulator of order N, a decimation filter of order N+1 suffices for out-of-band quantization noise suppression.

3. CT $\Sigma\Delta$-MODULATOR OPTIMIZATION

As was previously seen, the MSA is inversely proportional to the feedback filter cut-off frequency. However the SQNR curves suggests that the maximum SQNR is achieved for low values of the MSA. A very low MSA points towards a very high power consumption in the analog implementation, since in order to obtain the desired dynamic range, very low noise analog blocks must be developed, indicating high biasing currents.

Clearly, a trade-off exists between the analog power consumption, the MSA and the SQNR.

3.1. Power estimation

The core elements of an analog integrator consists of an integrating capacitor and a regulating active element, e.g. an op-amp. The power consumption of the active element is then determined by the GBW necessitated by the integrator specifications, e.g. max. input frequency. Whereas the size of the capacitor is determined by noise limitations hereby setting dynamic power consumption.

We have previously derived an expression for the quantization noise σ_q^2. Referring the quantization noise to a reference voltage V_{ref} and taking the combined filtering of $\mathrm{NTF}(z)$ and $H_{\mathrm{com\,b}}(z)$ into account, we have the resulting quantization noise power:

$$P_{\mathrm{Q}} = \frac{V_{\mathrm{ref}}^2}{A(K_{\mathrm{eq}})f_s}\int_0^{\pi}\left|\frac{H_{\mathrm{com\,b}}\left(e^{j\omega}\right)}{1+K_{\mathrm{eq}}H\left(e^{j\omega}\right)}\right|^2 d\omega \qquad (9)$$

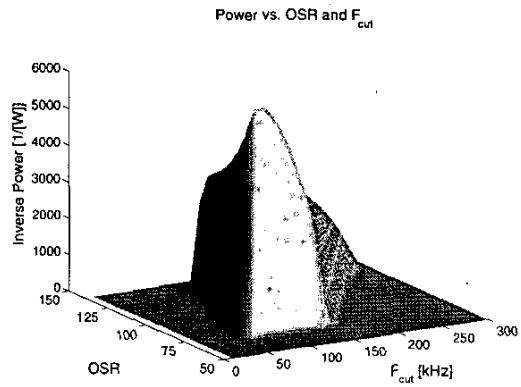

Figure 5: Inverse power consumption of a 3rd order $\Sigma\Delta$ ADC.

The thermal noise accumulated on the integrating capacitor is:

$$P_{\mathrm{Th}} = \frac{\mathrm{NEF}\cdot kT}{C_{\mathrm{int}}} \qquad (10)$$

where NEF is the Noise Excess Factor taking the added circuitry noise into account.

The total amount of noise allowable for a resolution of b bits is given by:

$$P_{\mathrm{N}} = \frac{(\mathrm{MSA}\cdot V_{\mathrm{ref}})^2}{2\cdot 10^{(6.02b+1.76)/10}} \qquad (11)$$

Combining equations (9-11), we can solve for the minimum allowable capacitor size:

$$C_{\mathrm{int}} = \mathrm{NEF}\cdot kT\left[\frac{(\mathrm{MSA}\cdot V_{\mathrm{ref}})^2}{2\cdot 10^{(6.02b+1.76)/10}} - P_{\mathrm{Q}}\right]^{-1} \qquad (12)$$

The static power consumption is determined by the required GBW of the regulating cell. A first order approximation of the necessary bias current I_{B}, can be found:

$$I_{\mathrm{B}} = \frac{\mathrm{GBW}^2 C_{\mathrm{l}}^2}{2\beta} \qquad (13)$$

C_{l} is the loading capacitance and β is the beta of the driving MOS transistor.

As the output of the first integrator goes unattenuated to the ADC output, the requirements of this block are as strict as for the overall system. The outputs of the other blocks however, are filtered and the requirements for these can hence be significantly loosened. The GBW of the integrators can be lessened, implying a lower I_{B} and more noise can be tolerated on the integrating capacitors, allowing for a smaller capacitors C_{int}.

Let P_c denote the quantizer power per frequency, the analog power is then approximated by:

$$P_{\mathrm{an}} \approx 4V_{\mathrm{ref}}f_s\sum_{i=1}^{N}C_{\mathrm{int,i}} + mV_{\mathrm{DD}}\sum_{i=1}^{N}I_{\mathrm{B,i}} + P_c f_s \qquad (14)$$

m is the number of current branches in the regulating element and the summations indicate the scaling of bias currents and capacitors for the cascade of integrators.

Power Consumption	171 μW
Supply Voltage	1.8 V
Sampling Frequency	1.5 MHz, (OSR=75)
Feedback filter cut-off frequency, f_c	100 kHz
SNR	> 65 dB
SFDR	> 63 dB
Technology	0.35 μm CMOS

Table 2: Test design performance summary.

The digital circuitry when using the FIR2 decimation filter structure is confined to D-flip flops, half- and fulladders. For a given clock frequency we have:

$$P_{\text{dig}} = \alpha \sum_{i=1}^{\log_2 D-1} \frac{f_{\text{clk}}}{2^{i-1}} \left(P_{\text{fa}} + P_{\text{ha}} + P_{\text{dff}}\right) \qquad (15)$$

The frequency dependent power consumption of the digital blocks can be found in the datasheets of the employed technology. α denotes the activity factor. The total power of the modulator is thus given by: $P_{\text{tot}} = P_{\text{an}} + P_{\text{dig}}$. The inverse power is plotted for a third order modulator in fig. 5, where 10 bits of accuracy is required and $V_{\text{ref}} = 200\,\text{mV}$. A clear peak is observed, indicating that a global optimum with regards to power efficiency exists. Hence an optimum f_{clk} and f_c can be extracted for a modulator of order N.

4. TEST CASE

In order to verify the developed design method, a prototype ADC requiring 10 bits performance was simulated. In the table below, the projected power consumption of $\Sigma\Delta$ ADCs of order 2-5 are shown, indicating that a third order $\Sigma\Delta$ is suitable for the specifications.

N	2	3	4	5
P [μW]	308	164	195	257

The prototype $\Sigma\Delta$ ADC was simulated at transistor level using a 0.35 μm CMOS process. The integrators were implemented as $G_m - C$ cells, where the G_m was obtained by placing a MOST in the linear region and the necessary GBW given by the speed requirements for the regulating loop. An example output spectrum with a tone at the MSA of the prototype modulator is shown in fig. 6. The third harmonic is below $-63\,\text{dB}$, indicating 10 bits spurious-free performance is obtained. The fifth harmonic is not visible as it is buried beneath the noise floor. The even order harmonics are suppressed due to the fully differential structure. Overlaid the spectrum, the employed decimating comb-filter transfer function is shown. A summary of the prototype $\Sigma\Delta$-modulator performance is given in table 2.

A comparison with an equivalent SC $\Sigma\Delta$ ADC is in it's place. The number of time constants n, necessary for first order settling behaviour to b bits can be found from: $n > (b+1)\ln(2)$, which resolves to $n \approx 8$ for 10 bits performance. Using a first order model of an op-amp, we have that: $GBW = g_m/C_{\text{int}} = 1/\tau$, where the transconductance is: $g_m = \sqrt{2\beta I_B}$. Requiring the output to settle within half a clock-period, we have that: $1/\tau = 16 f_s$. Hence we can approximate the necessary bias current:

$$I_B \approx \frac{(16 f_s C_{\text{int}})^2}{2\beta} \qquad (16)$$

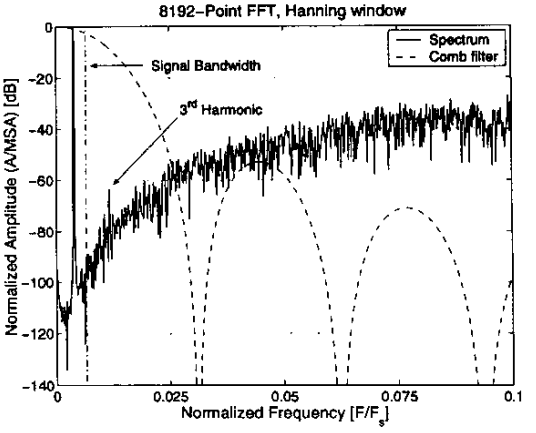

Figure 6: Output spectrum of the test design $\Sigma\Delta$ ADC.

Using the same capacitor sizes and parameters as in the prototype ADC and employing a folded cascode op-amp, the static power consumption of the integrators can be found to be: $P_{\text{stat,DT}} \approx 335\,\mu\text{W}$. Whereas the corresponding CT consumption in the prototype ADC is: $P_{\text{stat,CT}} \approx 111\,\mu\text{W}$. Hence an estimated 2/3 of the static integrator power consumption has been saved by employing a CT structure.

5. CONCLUSION

A design methodology for CT single-loop $\Sigma\Delta$ ADCs has been presented in this paper. The theory necessary for performance prediction was shown and a method for estimation of power consumption. For a given set of specificatons, the theory allows an optimum $\Sigma\Delta$ order, feedback filter cut-off frequency and sampling frequency to be extracted. Finally, a test case was specified and optimized in order to verify the theory. The prototype has performance in good correspondance with the expected results from the optimization routine, verifying the validity of the proposed methodology. An estimate of the power consumption of an equivalent DT cascade of integrators showed that power savings of approx. 2/3 had been obtained by using the CT configuration.

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