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Rasmussen, Frank Engel; Frech, J.; Heschel, M.; Hansen, Ole

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FABRICATION OF HIGH ASPECT RATIO THROUGH-WAFER VIAS IN CMOS WAFERS FOR 3-D PACKAGING APPLICATIONS

F. E. Rasmussen[1,*], J. Frech[2], M. Heschel[3] and O. Hansen[1]
[1]*MIC*, Technical University of Denmark, Bldg. 345 East, DK-2800 Kgs. Lyngby, Denmark
[2]*HSG-IMIT*, Wilhelm-Schickard-Strasse 10, D-78052 Villingen-Schwenningen, Germany
[3]*Hymite A/S*, Technical University of Denmark, Bldg. 325, 1st floor, DK-2800 Kgs. Lyngby, Denmark
*E-mail: fra@mic.dtu.dk http://www.mic.dtu.dk
Phone: +45 2682 3493 Fax: +45 3927 7900

ABSTRACT

A process for fabrication of through-wafer vias in CMOS wafers is presented. The process presented offers simple and well controlled fabrication of through-wafer vias using DRIE formation of wafer through-holes, low temperature deposition of through-hole insulation, doubled sided sputtering of Cr/Au, and electroless deposition of Cu. A novel characteristic of the process is the use of a metal etch stop layer providing perfect control of the etch profile of the wafer through-holes in combination with a remarkably improved etch uniformity across the wafer.

Excellent through-hole insulation is provided through the use of a CVD deposited polymer, Parylene C, whereas electroless deposition of Cu ensures even distribution of the via metallization.

INTRODUCTION

The use of 3-D interconnects, in the form of through-wafer vias, has previously been proposed to achieve denser microsystems packages [1,2,3,4]. Application of through-wafer via technology offers the possibility of advanced microelectronic chip stacking or stacking of various types of microcomponents directly on for example a CMOS chip. The latter implies the possibility of stacking e.g. MEMS-devices on CMOS chips in order to provide the often needed direct conditioning of the MEMS device output signal. If through-wafer vias is applied in combination with wafer level packaging, fabrication of ultra small 3-D packages containing several active devices is possible. Ultimately this 3-D package could represent a complete microsystem that could be surface mounted as a ball grid array (BGA) using solder bumps.

This paper presents a relatively simple process for post processing of high aspect ratio through-wafer vias in CMOS wafers. The overall objective of this work has been to develop a process for through-wafer via fabrication that has a realistic chance of being successfully implemented in a high-end portable product. The leading thoughts behind the process design have therefore been to create a process sequence containing as few critical process steps as possible, and to create a process sequence that is relatively insensitive to process variations and non-uniformities. The resulting process design allows great latitude in the choice of parameters for the individual process steps, thus lightening the task of transferring the final process from development to production facility.

The through-wafer via process presented is designed to be applicable as a post process to any kind of CMOS wafer regardless of the type of passivation provided by the CMOS foundry (usually silicon oxide, silicon nitride or polyimide). The thermal budget of a CMOS compatible process is rather limited, i.e. normally below ~450°C (above this approximate temperature the CMOS Al metallization will start diffusing into the silicon, thus causing non-functional circuits). For post processing on CMOS wafers having polyimide passivation the thermal budget is reduced even further. Thus, in present case the highest process temperature has been kept at 300°C.

The process developed offers simple but well controlled through-wafer via formation eliminating common problems like notching [2,5,6,7] and poor distribution of via metallization and insulation material [2,6]. The process is based on fast Si-DRIE of wafer through-holes, low temperature deposition of through-hole insulation, double sided sputtering of Cr/Au, and electroless deposition of Cu. The fast Si-DRIE process offers high etch rates in the range of 6 μm/min. depending on actual loading, feature sizes and etch depth.

A 3-D illustration of a final through-wafer via is shown in Figure 1.

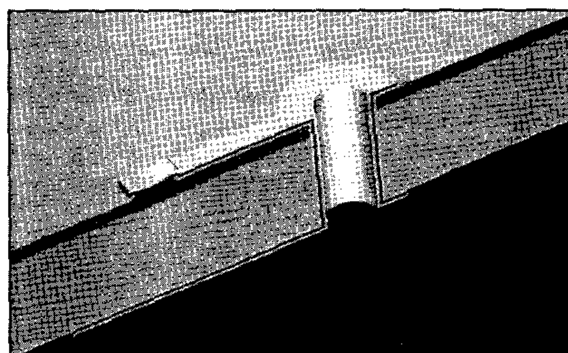

Figure 1: *3-D illustration of final through-wafer via providing electrical contact from a CMOS pad on the front side of the chip to a redistribution network on the backside.*

FABRICATION

A simplified version of the process sequence is shown in Figure 2.

The process sequence is applied directly on the CMOS wafers as provided by the CMOS foundry (backlapped). Initially a protective PECVD silicon nitride layer is

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deposited on the front side of the wafer (Figure 2-a). The CMOS wafer is then chemical mechanical polished (CMP) in order to obtain a smooth and defect free surface suitable for further processing. The protective PECVD nitride covering the entire front surface has to be opened above the CMOS contact pads in order to allow subsequent deposited metal layers to make electrical contact to the pads. The PECVD nitride is patterned in a reactive ion etching (RIE) process using a suitable photoresist mask.

A sacrificial Al layer is sputter deposited on the backside of the wafer (Figure 2-b) in order to provide an etch stop for the DRIE formation of the wafer through-holes (Figure 2-d). Additionally, the Al etch stop functions as a membrane preventing He leaking into the process chamber once the wafer through-holes are formed (He is used for wafer cooling during Si-DRIE). In present case an Al thickness of 2 μm has been chosen in order to provide a sufficient mechanically stable etch stop layer.

A thick photoresist layer (9.5 μm, AZ4562) is deposited on the front side of the wafer. The photoresist is patterned to define circular openings with a diameter of 100 μm. The PECVD silicon nitride is then patterned correspondingly using RIE with the photoresist acting as a mask (Figure 2-c). The wafer through-holes are formed in a room temperature Si-DRIE process (Figure 2-d) using alternating gas chemistry; SF_6 for Si etching and C_4F_8 for intermediate passivation (BOSCH process). In present case an average Si etch rate of 4.5 μm/min was obtained for circular 100 μm wide and 350 μm deep wafer through-holes (< 1% loading). The Si-DRIE process terminates on the Al layer on the backside of the wafer without deteriorating the profile of the wafer through-hole, i.e. without notching effects.

After through-hole formation the Al etch stop layer is etched using a mixture of phosphoric, acetic and nitric acid. The resulting etch rate is approximately 0.2 μm/min.

The wafer through-holes are insulated by room temperature CVD of 3 μm Parylene C (poly-monochloro-para-xylylene) (Figure 2-e). Parylene C is a high quality dielectric material ideally suited for through-hole insulation as it offers perfect step coverage, low dielectric constant (3.1 @ 1 kHz), chemical inertness and low water absorption. The Parylene C CVD process is characterized by the ability to coat the entire wafer conformably in one process step. The simultaneous coating of wafer front, backside and inside of wafer through-holes provides an efficient insulation of the final via.

The Parylene deposited on the CMOS contact pads on the wafer front side is removed in a RIE process using a standard photoresist layer as a mask (Figure 2-e). The small lateral dimension of the via holes combined with the mild resolution requirement (only definition of large feature sizes is needed) allows for spinning of photoresist in a standard photoresist spinner. In present case a Suss RC8 spinner was used with a dedicated non-vacuum chuck, which eliminates potential problems with photoresist penetrating through the holes to the backside of the wafer. The spinner was mounted with the Suss Gyrset system which reduces spinning defects such as striations and comets, which otherwise could be expected when spinning on a surface with holes.

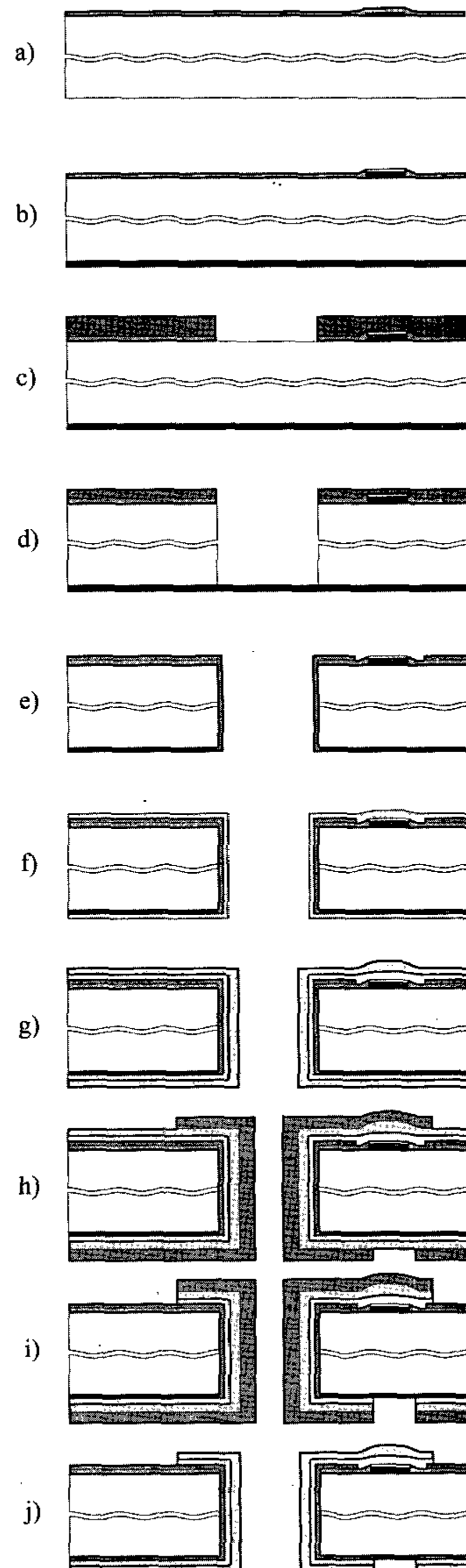

Figure 2: *Simplified process sequence for post processing of through-wafer vias in CMOS wafers.*

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Prior to deposition of the through-hole metallization the Parylene surface is treated in a mild oxygen plasma in order to improve the conditions for obtaining good metal adhesion. The wafers were treated in a plasma etcher (barrel type) with the process parameters: O_2: 120 ml/min., N2: 20 ml/min., RF: 150 W, T: 3-5 min.

The through-hole metallization is deposited immediately after the plasma treatment. A plating base consisting of 500 nm Cr and 500 nm Au is sputter deposited on both sides of the wafer (Figure 2-f).

In order to obtain sufficiently low resistance of the final through-wafer vias a thick Cu-layer is deposited (3-5 µm). The Cu is deposited in an electroless process using the sputter deposited Cr/Au as a seed layer (Figure 2-g), i.e. simultaneous deposition on both sides of the wafer and inside the wafer through-holes. The electroless Cu deposition process is based on a commercially available electrolyte (CIRCUPOSIT 3350, Shipley) giving a deposition rate around 5 µm/hour.

In order to define the final structure of the via metallization on front and backside of the wafer an electrodeposited, negatively working photoresist is applied (Eagle 2100 ED, Shipley). By applying a DC voltage across the Cr/Au/Cu metallization the resist is uniformly deposited all over the wafer (including inside of wafer through-holes) in a cataphoretic electrodeposition process taking place at 35°C (Figure 2-h). This type of resist is not widely used within the field of MEMS, though it is well known in the printed circuit board (PCB) industry as it is originally developed for patterning of Cu wires on PCB [8]. Using a standard mask aligner the front and backside of the photoresist coated wafer is exposed, and the electrodeposited resist is subsequently developed in a dedicated developer. Finally, the through-wafer via metallization is structured by wet chemical etching using the electrodeposited photoresist as an etch mask (Figure 2-i). The Cu metal is etched using a sodium persulfate ($Na_2S_2O_8$) solution, whereas the underlying Cr/Au base layer is sequentially etched using commercial Au and Cr etchants, which are both Cu compatible.

The electrodeposited photoresist mould is stripped using a dedicated remover (Figure 2-j).

RESULTS & DISCUSSION

A novel characteristic of the process presented above is the use of a metal etch stop layer. As shown in Figure 3 the Si-DRIE process itself results in nearly vertical sidewall profiles, but it is the Al etch stop that actually provides means for perfect control of the etch profile (Figure 4) as it eliminates the problem of notching, which is commonly observed when insulating etch stop materials like silicon oxide are used [2,5,6,7]. Thus, using the Al etch stop allows for prolonged over-etching without deterioration of the etch profile, which is often necessary to ensure proper breakthrough of all through-holes across the wafer. This feature is especially important when working on CMOS wafers, where process uniformity across the wafer can be an issue because of the large wafer size (typically 6 or 8 inch).

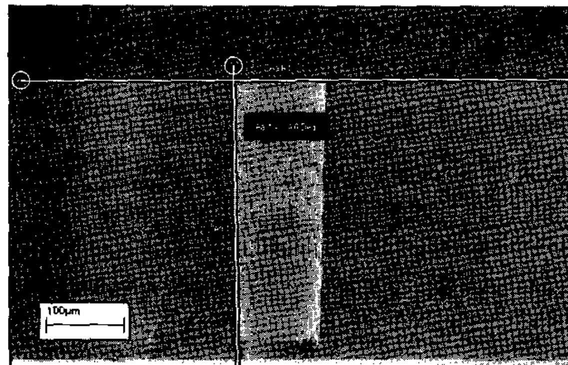

Figure 3: *SEM micrograph of the etch profile of a through-hole fabricated using fast Si-DRIE (average etch rate of 4.5 µm/min.). The defects at the entrance of the hole (in the bottom of the picture) are caused by the wafer cleavage.*

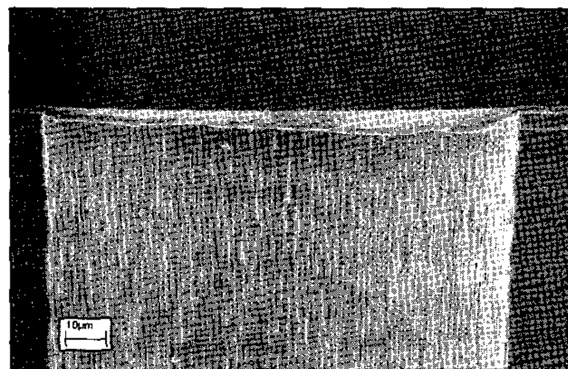

Figure 4: *SEM micrograph showing close-up on Al etch stop eliminating the problem of notching. The 2 µm thick Al membrane spans across a 100 µm wide wafer through-hole.*

Adhesion of metal on Parylene C

The use of Parylene C ensures high quality insulation of the through-wafer vias. However, an inherent disadvantage is related to the chemically passive surface of the Parylene, which makes it difficult to obtain sufficient adhesion of metals deposited on top thereof. In order to improve metal adhesion the Parylene surface was pre-treated in a mild oxygen plasma, as previously described. The structure of the Parylene surface is chemically modified by the oxygen plasma. A clear indication of this is the shift from the very hydrophobic, as-deposited Parylene surface to a hydrophilic surface after plasma treatment. The modification of the chemical structure of the surface allows for formation of metal-oxygen-carbon and metal-carbon bonds, which is assumed to be the main contributing factor for improved metal adhesion [9]. In addition to the plasma treatment experiments with different adhesion metals were performed. In summary, the best results were obtained using Cr.

Sputter deposition of Cr/Au

The use of sputtering for deposition of Cr/Au is a very important aspect of the presented process in order to ensure CMOS compatibility. Compared to e-beam evaporation, which is another commonly used deposition technique

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within microfabrication, sputtering is not associated with generation of X-rays and the risk of radiation damaging the sensitive CMOS circuitry is therefore significantly reduced (X-rays are known to cause threshold voltage shifts, etc.).

The thickness of the sputtered layers (on the wafer surface) has to be sufficiently large in order to guarantee deposition of even a very thin layer on the sidewalls deep inside the wafer through-holes. As an example double sided sputtering of a 500 nm thick metal layer will according to theory result in a deposit thickness in the middle of the wafer through-hole of around 10-20 nm (for a hole with a depth to diameter ratio of 4) [10]. On this basis double sided sputtering of 500 nm Cr and 500 nm Au has been chosen in order to obtain a sufficiently thick and continuous film inside the through-hole.

Electroless Cu deposition

The electroless process ensures almost perfect metal distribution as the reduction of metal ions in the deposition process is entirely chemically driven. Thus, the material distribution depends only on the availability of reducing agents, metal ions and a catalytic surface, i.e. a surface acting as catalyst in the reduction process of the given metal ions (in this case the sputtered Au surface).

The presence of a clean and wettable surface is crucial to obtain successful, chemical deposition of Cu. The as-deposited Au surface showed only limited ability to initiate the deposition process (sporadic Cu deposition was obtained). This was mainly attributed to the fact that the Au surface exhibited poor wettability. Various combinations of different cleaning steps were attempted in order to improve wettability and facilitate optimum conditions for the chemical Cu deposition process. The most successful pre-treatment was found to be sequential cleaning of the wafer using an oxygen plasma (O_2: 220 ml/min., N2: 100 ml/min., RF: 500 W, T: 5 min.) followed by electrochemical cleaning in a cyanide containing degreaser for 60 sec., and finally a short dip (30 sec.) in a pickling solution (HF containing, dry acid solution). Electrochemical cleaning and pickling solution dip are parts of the standard cleaning procedure performed prior to plating of metals. When these cleaning steps are included and performed immediately before immersion of the wafer in the Cu electrolyte excellent uniformity is obtained.

Figure 5 shows a SEM micrograph of a final through-wafer via. As shown in Figure 5 the chosen metallization scheme yields a very smooth and uniform coating (even around the critical corners at the entrance of the wafer through-hole).

CONCLUSION

The through-wafer vias are an ideal tool for achieving denser packages as they allow for integration of microcomponents with integrated circuitry through monolithic as well as hybrid integration approaches.

The presented process allows for fabrication of through-wafer vias in wafers containing sensitive CMOS circuitry.

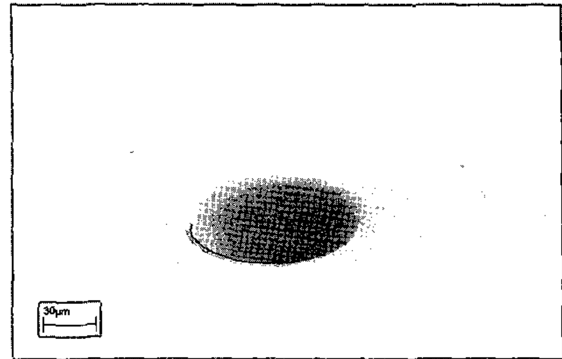

Figure 5: *SEM of final through-wafer via.*

The through-wafer vias are fabricated using a relatively simple process flow containing a minimum of critical process steps. Metallization of Parylene C showed to be the main challenge of the presented process. The chosen metallization scheme using a combination of sputter deposited Cr/Au and chemically deposited Cu showed good results.

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