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Improvement of input power dynamic range for 20 Gbit/s optical WDM switch nodes using an integrated Michelson wavelength converter

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11

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ThD

8:30–10:00am

Room C241

All-Optical Switching

Jay Wiesenfeld, *AT&T Laboratories, Presider*

ThD1 (Invited)   8:30am

High-speed optical logic

K.L. Hall, K.A. Rauschenbach, N.S. Patel, *MIT Lincoln Laboratory, C-237, 244 Wood Street, Lexington, Massachusetts 02173-9108; E-mail: khall@ll.mit.edu*

All-optical switches and logic gates have been studied for many years, primarily because of their potential for high-speed operation. High-speed operation has been demonstrated in optical AND (demultiplexing) gates. For example, researchers at NTT have demonstrated all-optical demultiplexing of 100 Gbit/s data streams using a variety of optical switching elements.[1–4] Still, all-optical bit-wise logic has not been demonstrated above 40 Gbit/s.[5,6] However, rapid advances in the demonstrated switching speeds of optical logic gates are expected in the near future.

All-optical logic gates take advantage of the intensity-dependent transmission or the intensity-dependent refractive index (or both) of optical waveguides. Typically, short optical pulses are used to induce these nonlinearities because they have high peak powers and dissipate relatively small amounts of heat. Therefore soliton or short pulse communication systems, (with RZ signaling formats) will benefit most from the availability of all-optical logic gates. However, the simplest (utilizing a single waveguide) optical logic gates, NOT gates based on cross-gain saturation in active semiconductor waveguides, are compatible with NRZ signaling formats as well.[7] Another simple (single waveguide) logic gate is the all-optical AND gate based on four-wave mixing. Such gates have been used as demultiplexers,[4] wavelength converters,[5] and synchronizers[8] in recent experiments.

To achieve logic operations other than AND and NOT, interferometric switches, based on the intensity-dependent refractive-index effects in waveguides are necessary. To date, most interferometric switches have been based on the nonlinear optical loop mirror or NOLM.[9] Using either a fiber or an active semiconductor nonlinearity, AND, NOT, and XOR operation have been demonstrated. In addition, OR and NOR functionality have been demonstrated in an ultrafast nonlinear single-arm interferometer (UNI).[10] With this increased functionality comes complexity. In general, interferometric switches are more complicated to fabricate than simple single waveguide switches, they can be difficult to stabilize, and they require three input beams, the two logical inputs and a clock stream. Also, these devices are not, in general, cascadable. Recently, Mach-Zehnder interferometer and UNI configurations have been demonstrated that are cascadable. Still, without the use of optical amplifiers and filters, the fanout for these gates is low, limited by device loss and by the accumulation of amplified spontaneous emission noise.

The ultimate speed of all-optical logic gates is limited by the recovery time of the transmission and/or index nonlinearities responsible for the switching. That recovery time can be as short as the duration of the pulses doing the switching, as in the case of fiber-based switches, or as long as the carrier temperature equilibration time (approximately 1 ps),[11] as in the case of active semiconductor-based switches. Semiconductor-based switches are attractive because they are ultimately integrateable and have large nonlinear coefficients, facilitating smaller device dimensions. However, due to the nonlinear absorption effects accompanying the nonlinear index changes, it is unlikely that nonlinear waveguide lengths, using conventional semiconductor materials, can be reduced much below a hundred microns. Therefore, optical logic gates will not compete with electronic gates in terms of density on a chip. Also, without careful design, the semiconductor-based switching devices can be limited by carrier population and thermal effects to operation speeds of a few gigahertz.

With all these difficulties and drawbacks, optical logic gates are still attractive components for many applications. Any simple (small gate count) processor, such as an address recognition circuit or an encryption circuit, can be run at ultrahigh data rates using optical logic. Optical gates can be used as ultraprecise phase comparators in electro-optic phase-lock loops and synchronization circuits. Recently, optical gates have been used to generate microwave signals with high fractional bandwidth. It is clear that as the speed and reliability of optical logic gates improve, new circuits and applications will be demonstrated.

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6. N.S. Patel et al., in *Optical Fiber Communication Conference*, Vol. 2, 1996 OSA Technical Digest Series (Optical Society of America, Washington, D.C., 1996), paper PD14; Opt. Lett., in press.
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ThD2   9:00am

Improvement of input power dynamic range for 20 Gbit/s optical WDM switch nodes using an integrated Michelson wavelength converter

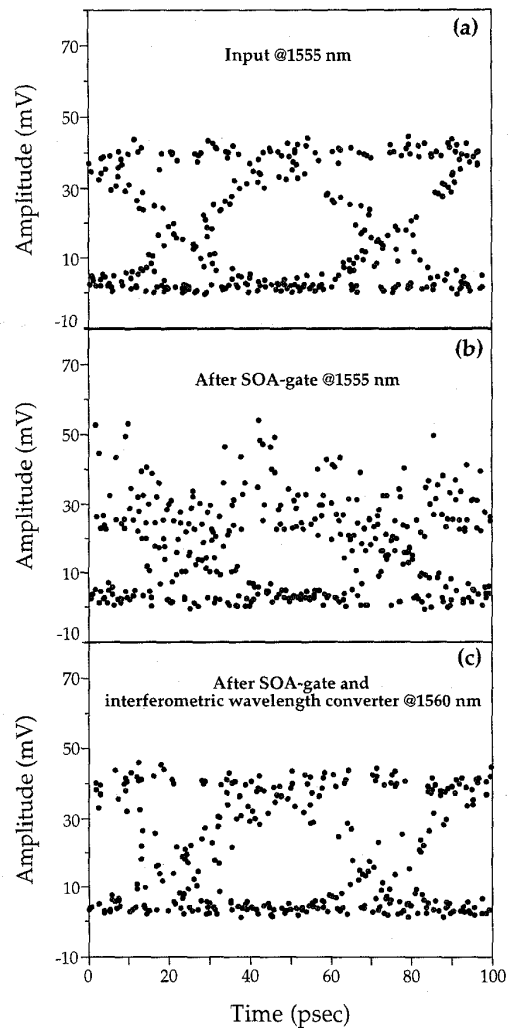S.L. Danielsen, P.B. Hansen, C. Joergensen, K.E. Stubkjaer, M. Schilling,* K. Daub,* K. Dütting,* M. Klenk,* W. Idler,* P. Doussiere,** F. Pommerau,** *Technical University Denmark, Department of Electromagnetics Systems, Building 348, DK-2800 Lyngby, Denmark; E-mail: sld@emi.dtu.dk*

The implementation of photonic wavelength-division multiplexing (WDM) switch nodes with wavelength converters allows for higher
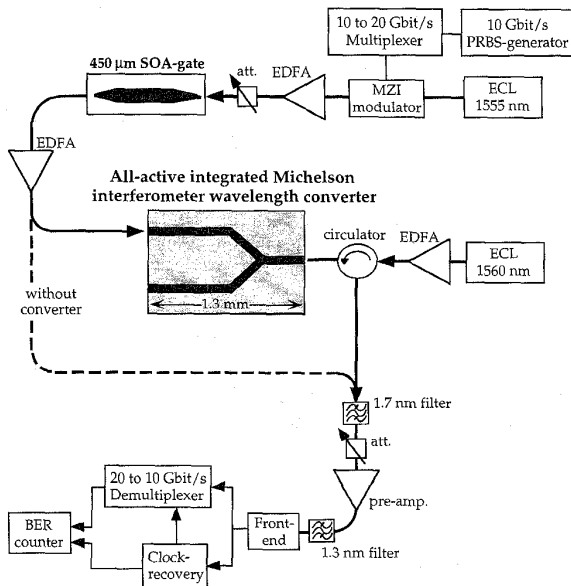
throughput and easier management, as well as wavelength reuse.[1] Furthermore, semiconductor optical amplifiers (SOAs) are attractive for space switching in the nodes because they offer short switching times (~1 ns), compensate for loss and, very importantly, have the high on-off ratios of 40–50 dB that are required to overcome cross talk induced penalty.[2] One disadvantage of the SOA gates is their limited input power dynamic range and, thus, limited cascadability caused by noise and gain saturation.[3] We show that even at a high bit-rate of 20 Gbit/s the latter imperfection can be compensated by the extinction ratio enhancing capability of interferometric wavelength converters (IWCs).[4] Consequently, the input power dynamic range for switch blocks using IWCs together with SOA gates can be improved compared to switch blocks without IWCs. This is especially important at high bit rates where the cascadability of the SOA gates decreases.[3] Here, more than 15 dB improvement of the input power dynamic range is achieved at 20 Gbit/s using a high-speed Michelson interferometer (MI) wavelength converter after the SOA gate compared to the SOA gate alone.

The experimental setup shown in Fig. 1 is used to measure the input power dynamic range for the SOA gate and for the gate followed by an MI wavelength converter. Light at 1555 nm is externally modulated at 20 Gbit/s before coupled to a 450-μm-long SOA gate[5] (operated at a fiber-to-fiber gain of 22 dB). Following the SOA gate an erbium-doped fiber amplifier (EDFA) in saturation boosts the signal to a power level of ~6 dBm before entering the receiver or wavelength converter. The converter is an integrated MI based on an all-active multiple quantum well structure[4] that converts from 1555 to 1560 nm using 9 dBm of input power at 1560 nm.
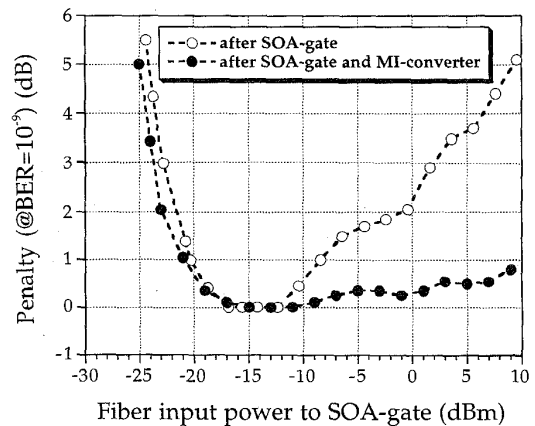
In Fig. 2 the regenerating capability of the interferomteric wavelength converter is illustrated by eye diagrams at: (a) the input of the SOA gate, (b) output of the SOA gate and (c) after the wavelength converter (c) for a relatively high input power of −3 dBm to the SOA gate. Due to gain saturation, the SOA gate clearly distorts the input signal leading to an extinction ratio of only 8 dB at the output compared to 12 dB at the input. However, when passing the interferometric wavelength converter

ThD2 Fig. 2. 20 Gbit/s eye diagrams at: (a) the input of the SOA gate at 1555 nm, (b) output of the SOA gate at 1555 nm and after the Michelson interferometer wavelength converter at 1560 nm. The input power to the SOA gate is −3 dBm.

ThD2 Fig. 1. 20 Gbit/s experimental setup for input power dynamic range measurements of SOA gate and SOA gate followed by an integrated all-active Michelson interferometer (MI) wavelength converter.

ThD2 Fig. 3. Power penalty (@BER = 10^{-9}) at 20 Gbit/s as function of the input power to the SOA gate. The curve indicated by (◯◯◯) is measured after the SOA gate while the curve given by (●●●) is measured after the SOA gate and MI wavelength converter.

the signal is regenerated and the extinction ratio enhanced to 10 dB. As seen in Fig. 3, this reduces the power penalty (@BER = 10^{-9}) from 1.8 dB after the SOA gate to about 0.4 dB after the wavelength converter. From Fig. 3, the important role of the 20-Gbit/s interferometric wavelength converter as a regenerating device in optical WDM switch nodes is obvious. Without the converter an input power dynamic range of ~12 dB is found while the input power dynamic range with the converter is increased by more than 15 dB.

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ThD3   9:15am

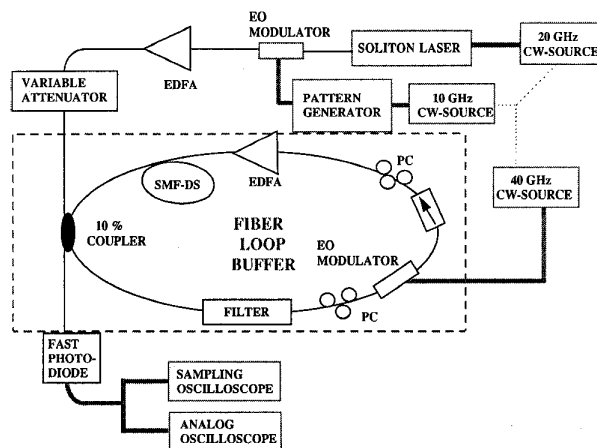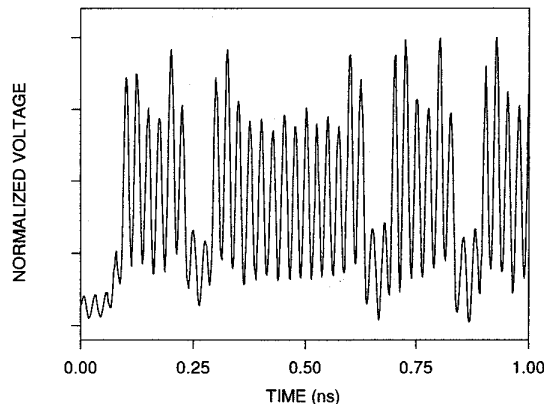### 40-Gbit/s optical packet buffering

K.L. Hall, *MIT Lincoln Laboratory, C-237, 244 Wood Street, Lexington, Massachusetts 02173-9108; E-mail: khall@ll.mit.edu*

Optical buffers storing single packets of optical data are important components for ultrahigh-speed multi-access time-division multiplexing (TDM) networks. Data packets must be stored while users wait for access to the network and while received packets are rate-converted to interface with slower speed electronics in the node.[1] Optical packet storage has been demonstrated at data rates of 10 Gbit/s in recirculating-loop transmission experiments.[2] Such loops are not applicable to data packet buffering in network applications because of their long lengths and because the sliding-guiding filters used to suppress continuum and reduce timing jitter can not be used to stabilize compact, (single packet), single-wavelength buffers. Previously, single-packet optical buffers have stored noise-generated data at rates up to 50 Gbit/s[3] and have stored externally generated data packets at 18 Gbit/s for 200 circulations.[4] Increasing the stored data rate is challenging because of the requirements for increased modulation bandwidth in certain loop components and increased power in the optical data streams. Also, fundamental issues such as the increased timing jitter introduced in the propagation of narrow pulses make scaling these devices to higher rates difficult. In this paper, we demonstrate the loading and unloading of 40-Gbit/s data packets in an optical buffer. Kilobit data packets comprised of 3-ps optical pulses are stored for more than 300 circulations. I believe this is the highest speed loading and unloading of an optical buffer to date.

The experimental setup is shown in Fig. 1. The optical buffer is similar to that described previously[3] except that we use a high-speed electro-optic (EO) modulator and drive it directly with a 40-GHz sine wave. The 15.5-MHz buffer fundamental frequency corresponds to a 2.58 kbit capacity at 40-GHz. The input data stream is generated by modulating the 3-ps pulses generated by a 40-GHz soliton compression source[5] with a 10-Gbit/s data signal generated by a high-speed pattern generator. A portion of the input data packet is shown in Fig. 2. Owing to the limited speed of the modulator and drive electronics, more than four optical pulses are transmitted by the modulator for each "1" in the

ThD3   Fig. 1.   Experimental setup. EDFA: erbium-doped fiber amplifier; SMF-DS: dispersion shifted fiber; PC: polarization controller.

ThD3   Fig. 2.   50-GHz digital sampling oscilloscope display of a portion of the input data packet detected by a 45-GHz bandwidth photodiode. The optical pulses are 3 ps in duration and have a center wavelength of 1553 nm.

electronic bit pattern. The 1.28-kbit-long input data packets are coupled into the buffer via one input arm of a 10% coupler, and out of the buffer via one output arm of this same 10% coupler. The stored packets are detected by a high-speed photodiode and displayed on an oscilloscope.

Figure 3 shows the buffer output displayed on a 1-GHz bandwidth oscilloscope. Because the scope bandwidth is not large enough to resolve the data bit pattern, the packet envelope is displayed. The largest amplitude packet corresponds to the input packet. The subsequent packets are stored copies of the input. In Fig. 3(a), the packet preceeding the input packet corresponds to the 80th circulation in the buffer, in Fig. 3(b) the 160th circulation and in Fig. 3(c), the 320th circulation.

The buffer successfully stores input packets with a large variation (approximately 10 dB) in average power. As a result, the buffer can be made insensitive to the polarization of the input data packet. The buffer can also be made insensitive to the timing of the input packet by turning off the drive to the EO modulator. However, without the timing stability introduced by loss modulation in the buffer, the 40-Gbit/s data packets are not stored for more than 50 circulations.

In conclusion, I have demonstrated the loading and unloading of a 40-Gbit/s data packet in an active fiber loop buffer. I believe this is the highest rate external loading of a loop buffer by more than a factor of two.