Compact All-optical Parity calculator based on a single all-active Mach-Zehnder Interferometer with an all-SOA amplified feedback

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TuQ2 **5:00 PM**

Compact All-Optical Parity Calculator Based on a Single All-Active Mach Zehnder Interferometer with All-SOA Amplified Feedback

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An all-optical signal processing circuit capable of parity calculations is demonstrated using a single integrated all-active SOA-based MZI, exploiting the integrated SOAs for feedback amplification.

1. Introduction

At present, all signal processing is done in the electronic domain. Issues such as power consumption, footprint requirements, and cost of high-speed electronics will make optical solutions more attractive as the bit rate increases, and thus simpler signal processing tasks may move into the optical domain [1]. Significant progress has been reported on optical signal processing circuits based on SOAs in fiber interferometers, including memory functionality through optical feedback [2-4]. Examples include an all-optical parity checker based on two TOADs [2], and a UNI based circulating shift register (CSR) with an inverter [4]. In both configurations an EDFA amplifies the output, which is fed back to the switch as a control signal. Since an EDFA contains many meters of fiber, it defines the latency of the circuit. This was identified as a problem in [2], and a bit-differential design was employed, in which an m-bit input word was injected m times before the parity of the word could be detected at the output. This is not realistic in a real system, and to solve the problem two things must be done: first, the time-of-flight (TOF) of the switch itself must be reduced. The only solution to this problem is integration, leaving SOA-based interferometers as prime candidates. Secondly, a feedback amplifier with minimum TOF, but still with sufficient output power to facilitate switching must be employed. The natural choice is the SOA, since ultimately integration with the switch and the feedback waveguide is desirable to further minimize the total TOF. The replacement of the EDFA with an SOA has already been demonstrated using the hybrid UNI [3], reducing the TOF of the feedback of an all-optical CSR to <10 ns. This paper reports on what we believe is the first demonstration of an all-optical signal processing circuit with feedback, based on a single integrated all-active MZI switch with (integrated) SOAs as feedback amplifiers. The circuit has a wide range of applications, e.g. parity calculation and parity check.

2. Principle, applications, and experiments

Fig. 1 (a) shows a schematic of an XOR gate with a feedback. Depending on the TOF of the feedback, the circuit has different applications: for a total delay D_T (incl. TOF through XOR gate) of one timeslot the circuit is an adjacent-bit parity calculator/checker, where the 1st bit is XOR'ed with the 2nd, the result of which is XOR'ed with the 3rd, etc. Assuming instead, that the data consists of slotted packets of fixed number of bits N_p, and D_T is adjusted to match the TOF of one packet, the output will represent the accumulated parity of a specific (payload) bit. Inserting the parity-bits into the header will enable performance monitoring downstream through re-calculation of the parity and comparison with header-bits. Fig. 1 (b) shows the implementation in terms of the experimental setup: a 10GHz clock at 1556.8nm from a gain-switched DFB laser (GS-DFB 1), is modulated with a periodic sequence **IN** from pulse pattern generator 1 (PPG 1), consisting of N_D bits at 10Gb/s, and launched into port #1 of the all-active MZI. The interferometer arms are 1200μm long, while all access-SOAs are 400μm. GS-DFB 2 emits a 10GHz clock at 1560.1nm, which is modulated with a gating sequence of period N_G effectively reducing the clock frequency of **CLK** to $(10/N_G)$ GHz, before it is injected into port #4 of the device. Without the feedback loop the output from port #3 represents the logic function **IN AND CLK** [5], which has a period of P_{AND}=LCM(N_D,N_G) (LCM:Least Common Multiple). By coupling this result into port #2 via the feedback loop, exploiting amplification in SOA #3 and SOA #2, and synchronizing the bits to the input sequence, the output of the circuit will represent the adjacent-bit parity calculator if N_G=1 and D_T=1 (timeslots of 100 ps). This is the case because the MZI works as a 2-input XOR gate for signals launched into ports #1 and #2 [5]. Alternatively, by setting N_G=D_T=packet length N_p, the output will be the accumulated parity of a specific (payload) bit. In general though, the output will represent the complex logic function **OUT(n)=(IN(n) XOR (IN(n-D_T) AND CLK(n-D_T))) AND CLK(n)**, where n is a bit counter. By studying this function it can be shown that for a total delay $D_T = X\times\text{LCM}(N_D, N_G)+Y$, where X belongs to N and Y to N_0, the period N_{out} of the output is given by the following, provided that Y=0 or Y can be divided by N_G: $N_{out}=D\times\text{LCM}(N_D, N_G)/\text{GCD}(\text{LCM}(N_D, N_G), y)$, where GCD: Greatest Common Divisor. The requirements correspond to the output from port #3 arriving at port #2 syn-

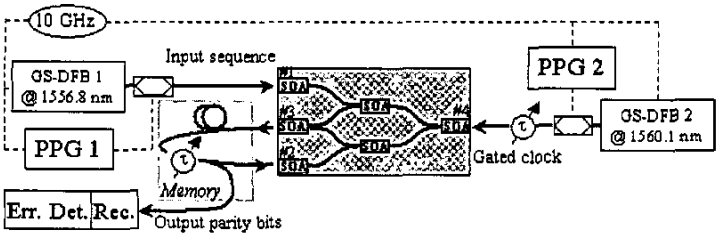

Fig. 1. (a) Schematic of XOR gate with feedback. (b) Experimental setup used to show proof of concept

chronized to **CLK** at port #4. If they are they not fulfilled, the output remains **IN AND CLK**, since the effect of the feedback will not be sampled by **CLK.**

The length of the fiber memory loop was ~ 20 m, and no attempt was made to reduce it, since this would require an irreversible customization of a 3-fiber-ribbon, while still not reducing D_T to near 1 timeslot. The TOF of the MZI is ~30ps, which means that the TOF of the feedback loop should be ~70ps or ~20ps for adjacent-bit parity calculation at 10 and 20Gb/s, respectively. Integrating a waveguide between SOAs #3 and #2 with a delay of ~20ps is technologically possible. Alternatively, the MZI could be placed in a planar lightwave circuit (PLC) containing a photonic crystal waveguide with sufficiently low loss, enabling very sharp bends. Another speed limiting factor is the counter-propagation induced transit time effects [6]. However, successful operation at 20Gb/s in counter propagation, also in a 1200μm long SOA, has been demonstrated [7].

To visualize the output pulse-pattern on a sampling oscilloscope the period N_{out} of the pattern must divide the trigger period N_T. The oscilloscope can be triggered by either PPG 1 or PPG 2, which transmit trigger signals with periods of LCM(N_D,128) and LCM(N_G256), respectively. Since the period P_{AND}=LCM(N_D,N_G) of **IN AND CLK** is independent of D_T, it is much easier to find a combination of N_D and N_G for which P_{AND} divides N_T than to divide N_T by the complex expression for N_{out} given above. Satisfying the requirements for obtaining the general output period, and visualizing the result on the scope, implies an optimization of D_T (by means of a delay line) while changing the periods N_D and N_G of the input and gating sequences to meet the triggering requirements. This is an extremely difficult task, so to visualize the output we have chosen (N_D,N_G)=(8,3), which fulfills the triggering requirements using PPG 2, for an output period of **IN AND CLK** of LCM(8,3)=24.

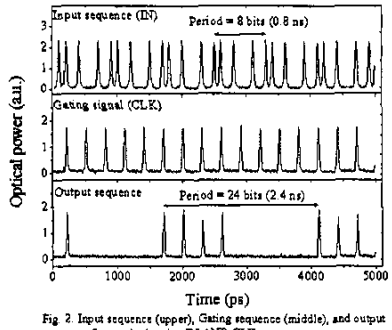

Fig. 2. Input sequence (upper), Gating sequence (middle), and output sequence (bottom), showing IN AND CLK

Fig. 2 shows pulse traces of the input sequence (upper), the gating sequence (middle), and the output sequence (lower), which unambiguously represents **IN AND CLK**.

Fig. 2 does not by itself prove that the feedback loop is active, since the output sequence is the same as if the input to port #2 is disconnected. By changing the input to a PRB sequence of word length 2^7-1 the output sequence no longer satisfies the triggering requirements, and the output can only be visualized as an eye diagram. By varying the delay in the memory we expect to observe an open eye diagram corresponding to **IN AND CLK**, when the synchronization between the gating clock and the feedback input to port #2 is so poor that the clock samples completely outside the switching window generated by the feedback signal. When the synchronization is perfect however, we expect an open eye diagram corresponding to the non-trivial function **OUT(n)**. In-between these extremes, the eye diagram will be closed due to partial synchronization. This is illustrated in Fig. 3 (a), which shows **IN**, the feedback at port #2 for three different synchronizations spaced by 100ps, and the clock **CLK**, respectively. The white set of feedback-bits in the second row corresponds to a missynchronization of 100ps between CLK and the feedback at port #2. As the delay is decreased towards 0, the eye will close, as the input to port #2 is misaligned with **IN** while the resulting distorted XOR switching window is sampled by the edge of the clock pulses. However, when the synchronization is perfect (delay = 0), the eye corresponding to **OUT(n)** opens up. This situation is shown with the gray set of bits in Fig. 3 (a). Decreasing the delay further, the eye will close again due to misalignment, and opens when the delay is -100ps, corresponding again to **IN AND CLK** (black set of bits). The measured eye diagrams in Fig. 3(b) correspond to delays of (clockwise): 100, 70, 60, 25, and 0 ps, and successfully demonstrate the transition from the white to the gray scenario in Fig. 3 (a). This proves that the feedback loop is active, since no change of eye diagram would have been observed otherwise. The transition of eye diagrams in Fig. 3(b), and the fact that a similar transition occurs as the current to SOA #2 is varied, are clear indications that the XOR function, and thus the feedback function, is working, and that the output does indeed represent the accumulating bit parity function. This is also verified by extensive modeling using a detailed time-domain model of a MZI introduced in [8].

3. Summary

We have proposed and demonstrated an all-optical signal processing circuit with feedback, consisting of a single all-active MZI, and using the built-in SOAs as feedback amplifiers. The circuit processed data at 10Gb/s, but is capable of calculating/checking the parity of successive bits at bitrates =20Gb/s, because of the low latency of the MZI combined with the promise of a very short, integrated, feedback owing to the use of SOAs for amplification. The scheme can also be used in a less demanding scheme for parity checking in packet switched networks.

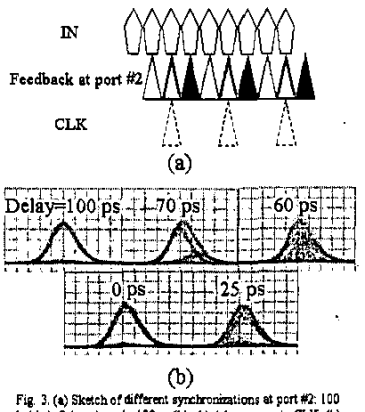

Fig. 3. (a) Sketch of different synchronizations at port #2: 100 (white), 0 (gray), and -100 ps (black) delay comp. to CLK. (b) Measured eye diagrams showing delay of 100 ps to 0

4. References

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TuQ3 **5:15 PM**

Photonic Random Access Memory Using Serial-to-Parallel and Parallel-to-Serial Conversion

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A novel photonic random access memory uses all-optical serial-to-parallel and electrical parallel-to-optical serial conversion, together with an optical clock-pulse generator and a silicon-based memory, and is demonstrated for 40-Gbit/s 16-bit burst optical packets.

1. Introduction

In future large-capacity optical packet-switched networks, many kinds of processing functions for high-speed asynchronous burst optical packets, such as label recognition, label swapping, buffering, bit-rate conversion, and 3R, may be needed. However, an increase in the optical packet bit rate will increase the difficulty in using electronic circuits. We have proposed a novel self-serial-to-parallel converter (self-SPC) [1] with a single optical clock pulse generator [2] for label recognition of a burst high-speed optical packet [3], and demonstrated 1-Tbit/s 16-bit SPC [4] and 40-Gbit/s 16-bit 1x4 self-routing [5]. In self-SPC, all bits of the incoming serial label are automatically converted to parallel bits using the single optical pulse generated based on the first bit of the label. This makes label recognition using CMOS electronic circuits easy. An attractive way to solve the remaining problems is to develop a photonic random access memory (RAM) that can process high-speed burst optical packets. So far, fiber-loop-type buffer memories have been demonstrated. They can store an optical packet in the optical domain, but cannot forward the stored packet at an arbitrary timing. Silicon electronic memory devices are very attractive because of their compact size, extremely large storage