



## Analysis and Design of a 1.8-GHz CMOS LC Quadrature VCO

Andreani, Pietro; Bonfanti, A.; Romanò, L.

*Published in:*

I E E E Journal of Solid State Circuits

*Link to article, DOI:*

[10.1109/JSSC.2002.804352](https://doi.org/10.1109/JSSC.2002.804352)

*Publication date:*

2002

*Document Version*

Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

*Citation (APA):*

Andreani, P., Bonfanti, A., & Romanò, L. (2002). Analysis and Design of a 1.8-GHz CMOS LC Quadrature VCO. *I E E E Journal of Solid State Circuits*, 37(12), 1737-1747. <https://doi.org/10.1109/JSSC.2002.804352>

---

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

# Analysis and Design of a 1.8-GHz CMOS *LC* Quadrature VCO

Pietro Andreani, *Member, IEEE*, Andrea Bonfanti, Luca Romanò, and Carlo Samori, *Member, IEEE*

**Abstract**—This paper presents a quadrature voltage-controlled oscillator (QVCO) based on the coupling of two *LC*-tank VCOs. A simplified theoretical analysis for the oscillation frequency and phase noise displayed by the QVCO in the  $1/f^3$  region is developed, and good agreement is found between theory and simulation results. A prototype for the QVCO was implemented in a 0.35- $\mu\text{m}$  CMOS process with three standard metal layers. The QVCO could be tuned between 1.64 and 1.97 GHz, and showed a phase noise of  $-140$  dBc/Hz or less across the tuning range at a 3-MHz offset frequency from the carrier, for a current consumption of 25 mA from a 2-V power supply. The equivalent phase error between I and Q signals was at most  $0.25^\circ$ .

**Index Terms**—CMOS, phase error, phase noise, quadrature, RF, voltage-controlled oscillator.

## I. INTRODUCTION

THE AVAILABILITY of accurate quadrature signals is a prerequisite for the implementation of image-rejection transceivers, the kind of radio architecture holding the promise of future complete transceiver integration [1]. It is therefore obvious that the study of quadrature generation has attracted the interest of many researchers. At present, the most popular method is to let the voltage-controlled oscillator (VCO), usually in the form of an *LC*-tank VCO, work at double the desired frequency, and then to obtain quadrature signals at the desired frequency via frequency division, performed either in the digital or in the analog domain [2]. The frequency-division approach has the additional beneficial effect of avoiding any pushing/pulling effect on the VCO due to a strong signal from the power amplifier (PA) in the transmitter chain of a fully integrated transceiver, since in this case the VCO is working at much higher frequencies than the PA. As a drawback, however, a higher oscillation frequency and the frequency-dividing circuitry result in an increased power consumption level.<sup>1</sup>

Quadrature can also be obtained by feeding the differential outputs of the VCO to a polyphase filter, usually realized as an RC polyphase filter [4]. Also, this approach introduces a substantial power consumption overhead, since the cascaded

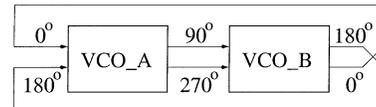


Fig. 1. Block schematic and signal phases for a QVCO.

RC filter stages needed to generate good quadrature signals in presence of the expected spread for resistance and capacitance values attenuate these signals significantly and possibly must be buffered from the preceding VCO (in order not to decrease the quality factor of the *LC*-tank) and from the following mixer.<sup>2</sup>

A third way of obtaining quadrature signals is through the use of a VCO design capable of directly delivering such signals. In principle, a ring oscillator fulfills this requirement, but the notorious high phase noise (or better, the low phase noise figure-of-merit, FoM) of ring oscillators [6] disqualifies this choice for most application in modern radio transceivers. A more attractive approach to direct quadrature synthesis relies on the possibility of coupling two symmetric *LC*-tank VCOs to each other, thereby exploiting the good phase noise performance of *LC*-oscillators [7]–[13] (provided that either good on-chip inductors are available or off-chip inductors are allowed). As exemplified by the block schematic in Fig. 1, the combination of a direct connection and a cross (inverting) connection forces the two VCOs to oscillate in quadrature. The first and best known implementation of this principle is the quadrature VCO (QVCO) proposed by Rofougaran *et al.* [7], reproduced in Fig. 2, where coupling between the two VCOs is enforced by transistors  $M_{\text{CPL}}$ , placed in parallel with the switch transistors  $M_{\text{SW}}$  (varactors have been omitted for readability, and all identical components have been named only once). We will refer to this topology as the parallel QVCO (P-QVCO) in the following. While the P-QVCO delivers four quadrature signals exhibiting low phase and amplitude errors, it has nevertheless not been used extensively because of the rather poor phase noise performance, despite being based on *LC*-tank VCOs.<sup>3</sup>

This issue was addressed by Vancorenland and Steyaert [14] and by van de Ven *et al.* [15], who proposed a modification of the original P-QVCO, where phase shifters are introduced between cascaded *LC* resonators, allowing each resonator to be optimally driven at a zero-degree phase shift. In this way, a QVCO with a superior phase-noise FoM was obtained [14]; however, phase shifters introduce some complication in the design and increase power consumption.

<sup>2</sup>Buffering can sometimes be avoided through a careful design optimization [5].

<sup>3</sup>Recent results [12] seem to be at variance with previous experience; this apparent contradiction will be explained in Section II.

Manuscript received April 30, 2002; revised June 23, 2002.

P. Andreani is with Ørsted-DTU, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark (e-mail: pa@oersted.dtu.dk).

A. Bonfanti, L. Romanò, and C. Samori are with the Department of Electronics and Information Technologies, Politecnico di Milan, 20133 Milan, Italy (e-mail: bonfanti@elet.polimi.it; lromano@elet.polimi.it; samori@elet.polimi.it).

Digital Object Identifier 10.1109/JSSC.2002.804352

<sup>1</sup>A higher oscillation frequency may allow the use of smaller, area-saving on-chip inductors, possibly increasing their quality factor ( $Q$ ), and the  $Q$  of the whole *LC*-tank, if the  $Q$  of the varactor is not too adversely affected [3].

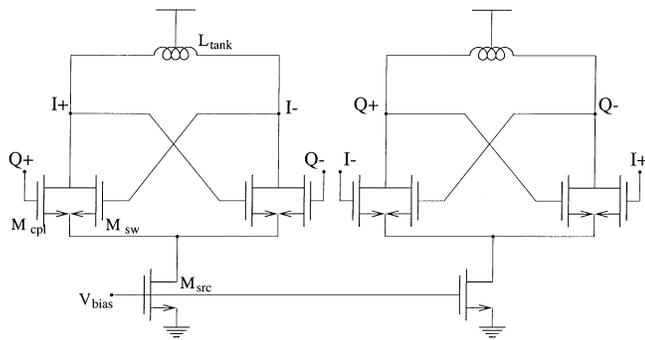


Fig. 2. Schematic view of the quadrature VCO presented in [7].

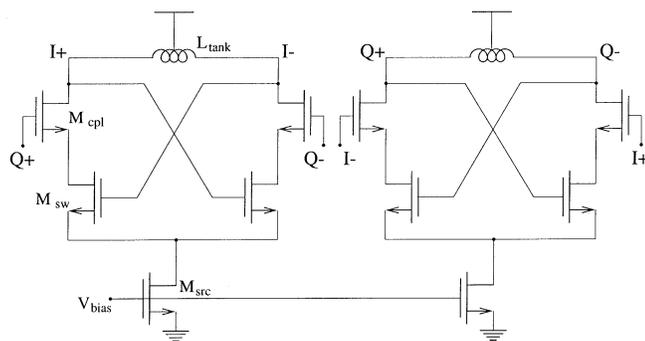


Fig. 3. Schematic view of the quadrature VCO proposed in this work.

The present paper analyzes an alternative way [16] of cross coupling two differential VCOs to obtain a QVCO, in which the coupling transistor  $M_{cpl}$  is placed in series with  $M_{sw}$ , rather than in parallel (Fig. 3). This choice is motivated by the consideration that  $M_{cpl}$  in the P-QVCO is responsible for a large contribution to the overall phase noise, and connecting  $M_{cpl}$  in series with  $M_{sw}$ , in a cascode-like fashion, should greatly reduce the noise from the cascode device. Admittedly, an oscillator having large signals present at every node works quite differently than a standard cascode circuit, but SpectreRF simulations show [17] that the new QVCO (to be referred to as series QVCO, S-QVCO) indeed displays an excellent phase noise behavior.<sup>4</sup>

The paper is organized as follows. Section II addresses the problem of how the performances of two different QVCOs can be compared in an objective way. Section III presents a simplified linear circuit model for the analysis of both P-QVCO and S-QVCO, while Section IV exploits this model for a quantitative analysis of the phase noise performance of the QVCOs in the  $1/f^3$  region (the mechanisms for the conversion of white noise into phase noise will not be dealt with in this paper). Despite the limitations of the model, the results of the phase noise analysis are in good agreement with those obtained with SpectreRF simulations. Finally, the experimental results for an S-QVCO implemented in a standard  $0.35 \mu\text{m}$  CMOS process will be illustrated in Section V.

<sup>4</sup>It is worth noting that there are more ways of achieving a series-like connection between  $M_{cpl}$  and  $M_{sw}$  [18]. We have recently discovered that yet another variant of the series QVCO topology has been proposed by Wu and Kao [19].

## II. COMPARING P-QVCO AND S-QVCO

The issue of how the performances of two different QVCOs can be compared in a fair and meaningful way is less trivial than it might seem at first sight, since the two qualifying data for a QVCO, that is, phase noise and phase error, are in general not independent of each other. In particular, this is the case for the P-QVCO, where both phase noise and phase error are strong functions of  $\alpha$ , defined as the ratio of the width  $W_{cpl}$  of transistor  $M_{cpl}$  to the width  $W_{sw}$  of transistor  $M_{sw}$  (assuming that both transistors have the same length)

$$\alpha = \frac{W_{cpl}}{W_{sw}}. \quad (1)$$

To see how the phase error varies with  $\alpha$ , the single-sideband (SSB) upconversion circuit [7], [16] in Fig. 4 has been used, so that the overall phase/amplitude errors between the phases, very difficult to measure directly in a reliable way, are translated into the ratio of the wanted upconverted band, to the unwanted, image band [to be referred to as image band rejection (IBR)]. In the case of the P-QVCO, simulations show that a mismatch of 0.1% between the inductors in the two LC-tanks results in an IBR of 70 dB for  $\alpha = 1$ , which drops to 60 dB for  $\alpha = 1/2$  and to 49 dB for  $\alpha = 1/3$  (Fig. 5). Clearly, the phase error gets quickly larger when the coupling between the two VCOs in the P-QVCO is weakened by decreasing  $\alpha$ . On the other hand, it is easy to check that the phase noise, too, greatly decreases with a decreasing  $\alpha$ . Thus, it is straightforward to improve the phase-noise performance of the P-QVCO at the expense of its phase-error performance. This is the case for the already mentioned P-QVCO presented by Tiebout [12], where a very high phase-noise FoM, the highest to date for QVCOs, was achieved by choosing  $\alpha = 1/3$ , while the original P-QVCO [7] had  $\alpha$  equal to unity.

Since we have seen that phase noise and phase error are in general not orthogonal (and can be traded for each other in the P-QVCO), it is not enough to compare only the phase-noise FoM between different QVCOs. If possible, the phase-noise FoM should be compared when the same level of component mismatch causes the same phase error. This is certainly possible when comparing P-QVCO and S-QVCO, since we have seen that the phase error in the P-QVCO can be tuned by changing  $\alpha$ . In the case of the S-QVCO, on the contrary, the phase error is almost independent of  $\alpha$  for all reasonable values of  $\alpha$ . This means that, while we can choose the value for  $\alpha$  which minimizes the phase noise, the phase error cannot be improved by allowing a higher phase noise. In this case, the phase error acts more like a design constant (dependent of course on the actual amount of mismatch between ideally identical components), once the QVCO architecture has been selected. In the case of the S-QVCO, assuming again a 0.1% LC-tank mismatch, the achievable IBR is 60 dB, that is, approximately the same IBR displayed by the P-QVCO when  $\alpha = 1/2$  (Fig. 5). If we now compare the phase noise displayed by P-QVCO and S-QVCO (Fig. 6; varactors were removed in these simulations, so that the resulting phase noise is due to the oscillator topology alone), when both QVCOs have the same IBR, center frequency, and

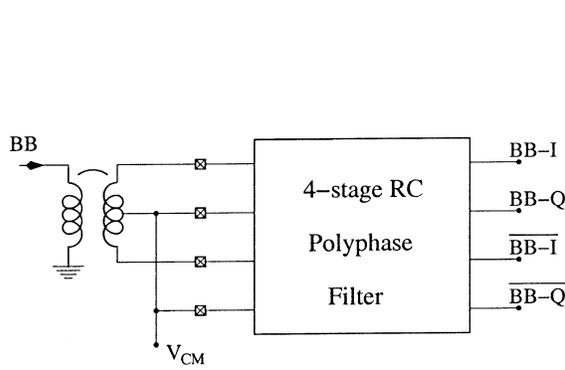


Fig. 4. Block schematic of the image rejection architecture (QVCO not shown).

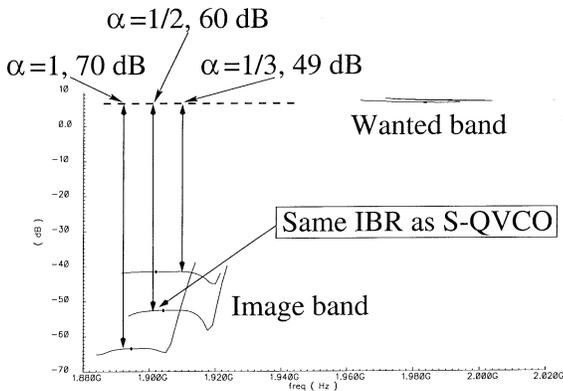
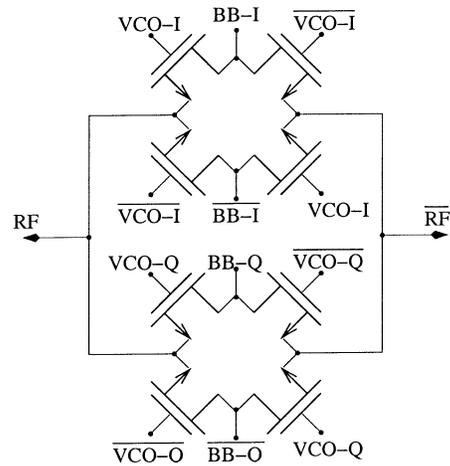


Fig. 5. IBR for the P-QVCO, in the presence of different values for  $\alpha$ .

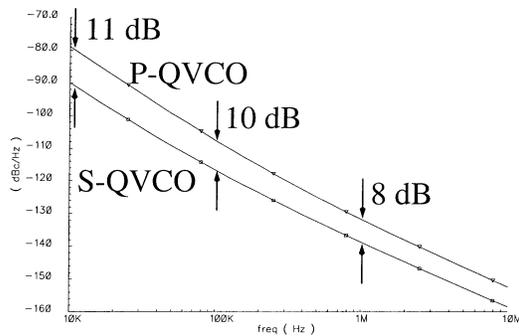


Fig. 6. Fair phase-noise comparison between P-QVCO and S-QVCO.

power consumption, there will be no doubt that the S-QVCO does outperform the P-QVCO.<sup>5</sup>

### III. A SIMPLIFIED QVCO MODEL

Fig. 7 introduces a linear model for the P-QVCO, where  $G_M$  represents the transconductance of the negative-resistance pair ( $M_{sw}$ ), and  $G_{Mc}$  the transconductance of the coupling pair ( $M_{cp1}$ ). Referring to this figure and also in the following, we consider voltage and current signals to be fully differential: the current flowing into the tank is the difference between the currents in the two branches of the differential stage. As a consequence,  $R_P$  is the loss resistance of one half-tank.

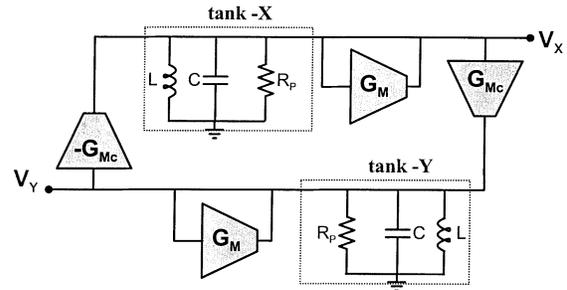


Fig. 7. Linear model for a QVCO.

<sup>5</sup>To complicate matters even further, an additional variable is the value of the sum of the transistor widths,  $W_{sum} \equiv W_{cp1} + W_{sw}$ . The results shown in Fig. 6 were obtained when both P-QVCO and S-QVCO shared the same value for  $W_{sum}$ . However,  $W_{sum}$  can be largely reduced for the P-QVCO, in which case its phase noise decreases by approximately 2 dB in the  $1/f^2$  region, but increases by several decibels in the  $1/f^3$  region. It should be noted that a lower value for  $W_{sum}$  allows the P-QVCO to achieve a higher maximum oscillation frequency, compared to the S-QVCO, or, when the oscillation frequency and the tuning range are the same for both P-QVCO and S-QVCO, the capacitance in the tank of the P-QVCO can be made more linear by introducing an additional metal-metal capacitor (when available) in parallel to the varactor, with the beneficial effect of reducing the conversion of low-frequency noise into phase noise due to the nonlinearities in the *LC* tank.

As shown in Appendix A, the oscillation frequency  $\omega_{OUT}$  results slightly displaced from the tank resonance  $\omega_0 = 1/\sqrt{LC}$  by an offset  $\Delta\omega$ , whose magnitude depends on  $G_{Mc}$ . This can also be explained in the following, intuitive way. Referring to  $V_X$  in Fig. 7, the losses in tank-X are balanced by a current in phase with  $V_X$ ,  $I_I = G_M V_X = V_X/R_P$ , which is provided by  $G_M$ . The tank is now lossless, and the current from  $G_{Mc}$  acts on an ideal *LC*-parallel. This second current,  $I_Q$ , is thus in quadrature with  $V_X$ , which in turn implies that  $V_X$  and  $V_Y$  are phase shifted by  $\pi/2$ . Fig. 8 shows the phasors of the voltage across the tank, and of the currents entering the tank. To find the relation between  $G_{Mc}$  and  $\Delta\omega$ , we consider the loop in Fig. 7 as composed by two ideal tanks coupled by  $G_{Mc}$ . The magnitude of each ideal tank, at an offset  $\Delta\omega$  from resonance, is approximately  $1/(2C|\Delta\omega|)$ . Since the loop gain must be unity at the

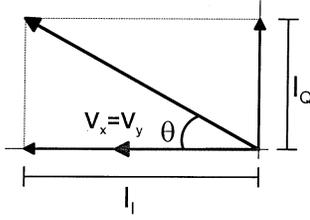


Fig. 8. Voltage and currents for tank- $X$  in Fig. 7. The first current harmonic is split into in-phase ( $I_I$ ) and quadrature ( $I_Q$ ) components.

oscillation frequency, we obtain  $G_{Mc}/(2C|\Delta\omega|) = 1$ , which yields two possible solutions for the frequency shift

$$\Delta\omega = \pm \frac{G_{Mc}}{2C}. \quad (2)$$

The shift is negative if  $I_Q$  is inductive and positive if  $I_Q$  is capacitive. The sign in (2) is established by the nonlinear mechanisms in the real oscillator and cannot be obtained from the linear model. Simulations show that both P-QVCO and S-QVCO seem to prefer the positive offset.

To a first approximation, the linear circuit can be used to analyze a nonlinear oscillator as well. In this case, we indicate with  $G_M$  the effective transconductance, given by the ratio of the component of the first current harmonic in-phase with  $V_X$ , here called  $I_{I,1}$ , to the oscillation amplitude  $A_0$ , which results in

$$G_M \equiv \frac{I_{I,1}}{A_0}. \quad (3)$$

Correspondingly, we define the effective coupling transconductance as

$$G_{Mc} \equiv \frac{I_{Q,1}}{A_0} \quad (4)$$

where  $I_{Q,1}$  is the quadrature component of the first current harmonic. In summary, the oscillation amplitude is set by  $I_{I,1}$  or, equivalently, by  $G_M$ , while the frequency offset is set by  $G_{Mc}$ .

Although counterintuitive, it is possible to extend the use of the linear model to the S-QVCO as well. In fact, it is easy to verify that even in this case the first harmonic of the current injected in the tank features an in-phase component that sets the amplitude  $A_0$ , and a quadrature term that determines the frequency shift  $\Delta\omega$ , so that (2)–(4) are still valid.

To estimate  $G_M$  and  $G_{Mc}$  in the P-QVCO, we schematize the circuit behavior as in Fig. 9. According to this model, it is possible to recognize four different working phases over a period, depending on what transistors are in the ON state. During phases 1 and 3, the tail current  $I_{TAIL}$  is shared between the cross-coupled transistors and the coupling transistors in a way that is best expressed with the parameter  $\delta$ , defined as

$$\delta = \frac{W_{cpl}}{W_{cpl} + W_{sw}} = \frac{\alpha}{1 + \alpha}. \quad (5)$$

The current levels indicated with  $I_1$  and  $I_2$  in Fig. 9 also depend on  $\delta$ , since

$$I_1 = -I_2 = (2\delta - 1)I_{TAIL}. \quad (6)$$

The picture of the current waveform is heavily simplified and makes the evaluation of  $I_{I,1}$  very easy, as follows:

$$I_{I,1} = \frac{1}{\pi}(2I_{TAIL} + I_2 - I_1) = \frac{4}{\pi}(1 - \delta)I_{TAIL}. \quad (7)$$

The oscillation amplitude is therefore

$$A_0 = \frac{4}{\pi}(1 - \delta)I_{TAIL}R_P \quad (8)$$

while  $I_{Q,1}$  and  $G_{Mc}$  are given by

$$I_{Q,1} = \frac{1}{\pi}(2I_{TAIL} + I_1 - I_2) = \frac{4}{\pi}\delta I_{TAIL} \quad (9)$$

and

$$G_{Mc} = \frac{I_{Q,1}}{A_0} = \frac{\delta}{1 - \delta} \frac{1}{R_P} \quad (10)$$

respectively.

The current waveforms for the S-QVCO are very similar to those for the P-QVCO, as shown in Fig. 10. During phases 2 and 4, the cross-coupled switches operate in the triode region and never switch off completely. Moreover, the coupling differential stage is never completely unbalanced, given the degeneration provided by the switches. The bias current is therefore shared between both branches during phases 2 and 4, while it is injected into only one branch during phases 1 and 3. It is not easy to express  $\delta$  for the S-QVCO with a simple formula, since  $\delta$  is related to the transistor sizes in a very nonlinear way, and circuit simulations become necessary. For the S-QVCO described in this work,  $\delta$  is approximately 0.3. The evaluation of  $I_{I,1}$  and  $I_{Q,1}$  yields of course once again (7)–(10), since the current waveform is the same as in the P-QVCO analysis.

If we now define the coupling strength between the two LC-tanks in a QVCO as the ratio  $G_{Mc}/G_M$ , it is noteworthy that the coupling strength for the S-QVCO is  $G_{Mc}/G_M = \delta/(1 - \delta) \cong 0.5$ , which is the same coupling strength displayed by the P-QVCO for  $\alpha = 0.5$ . Since it is reasonable to assume that the same coupling strength, in the presence of the same mismatch level between components, corresponds to the same phase error, these data offer an independent confirmation of the IBR simulation results discussed in the previous section, which showed that the P-QVCO with  $\alpha = 0.5$  had the same IBR value as the S-QVCO (Fig. 5). Thus, the simple QVCO model presented here, supplied with data from transient simulations, is nevertheless capable of capturing some of the complex behavior of the QVCOs.

#### IV. $1/f$ NOISE UP-CONVERSION

In this section, the mechanisms of  $1/f$  noise up-conversion into phase noise are analyzed for the two QVCOs. A peculiarity for both QVCOs is the dependence of their output frequency on  $G_{Mc}$ , as evident from (2). This makes  $\omega_{OUT}$  very sensitive to any fluctuation induced in  $G_{Mc}$ ; in particular,  $1/f$  noise can slowly modulate the average value of  $G_{Mc}$ , and thus be up-converted into close-in  $1/f^3$  phase noise. According to (10), in both circuits  $G_{Mc}$  is independent of the tail current and, therefore, also from its  $1/f$  noise. The  $1/f$  noise sources left are thus the ones in the switch transistors and in the coupling transistors.

We first refer to the P-QVCO, representing the  $1/f$  noise of a transistor with a current generator between its drain and source. Looking at Fig. 9, we notice that during phases 2 and 4 the

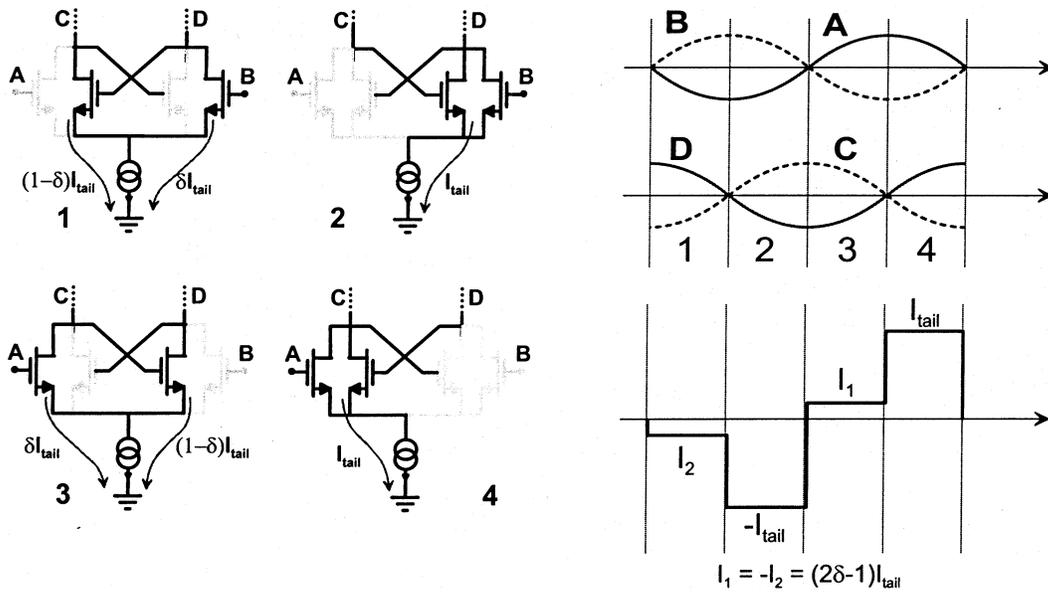


Fig. 9. A highly simplified picture for the differential current waveforms flowing into one LC-tank of the P-QVCO.

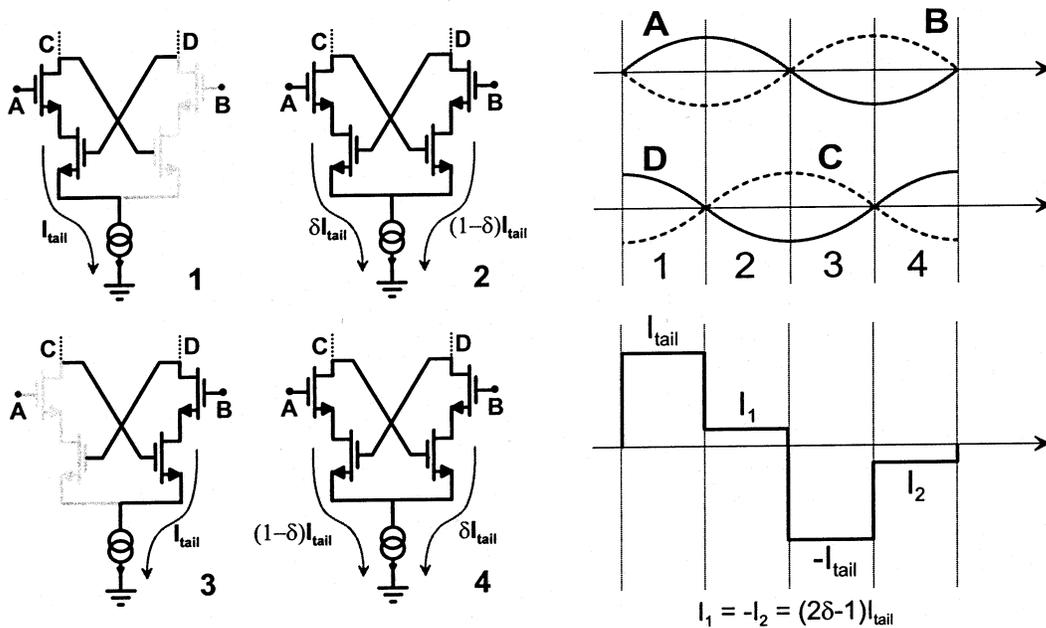


Fig. 10. A highly simplified picture for the differential current waveforms flowing into one LC-tank of the S-QVCO.

transistors are degenerated and their noise is rejected, while the noise finds a path to the tank during phases 1 and 3.

Fig. 11 depicts a half-oscillator during phase 3, where  $i_{cpl}$  and  $i_{sw}$  represent the  $1/f$  noise currents. Following [20], we consider the effect of these noise generators as producing a slowly varying current offset that affects the current level  $I_1$ , as shown in Fig. 12. This is equivalent to adding a square wave, with amplitude  $\Delta I_1$ , to the current injected into the tank. The frequency of this square wave is  $\omega_{OUT}$ , therefore both  $I_{Q,1}$  and  $I_{I,1}$  are changed. This in turn changes both  $G_{Mc}$  and  $A_0$  in the half-oscillator in Fig. 11, therefore changing the coupling exerted by  $G_{Mc}$  on the second half-oscillator. In this way, the  $1/f$  noise slowly modulates the average  $G_{Mc}$  in the loop, and  $\omega_{OUT}$  with it.

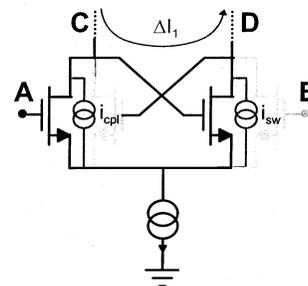


Fig. 11. Noise sources during phase 3 for the circuit in Fig. 9 (P-QVCO).

In the S-QVCO, the cross-coupled switches operate in the triode region for most of the oscillation period, and their  $1/f$

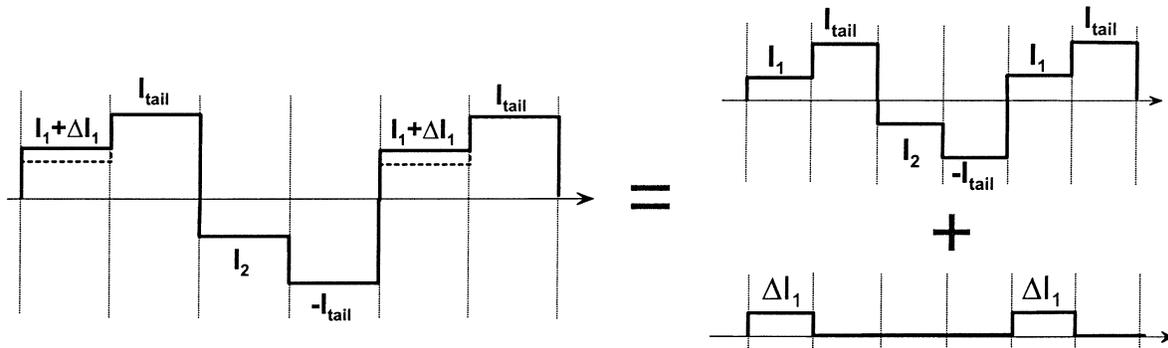


Fig. 12. Effect of the  $1/f$  noise generators in Fig. 11 (P-QVCO).

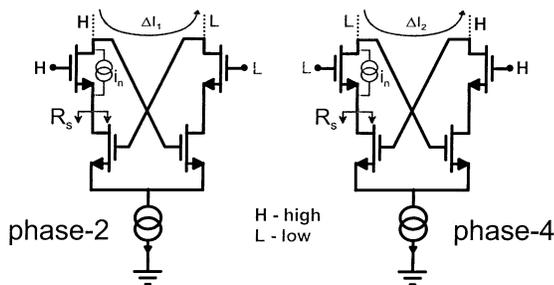


Fig. 13. Noise current from one coupling transistor in the S-QVCO. The noise current flows into the tank during phases 2 and 4.

noise is lower than the one for the coupling pair<sup>6</sup> [21]. As a first-order approximation, we neglect the  $1/f$  noise from the switches, focusing instead on the effect of the  $1/f$  noise from a single coupling transistor. It is enough to consider phases 2 and 4, as shown in Fig. 13, since such a noise is negligible under phases 1 and 3 (Fig. 10).

From Fig. 13 we see that the  $1/f$  noise again modifies both  $I_1$  and  $I_2$ , but its effect is reduced compared to the P-QVCO case, for two reasons. First, the degeneration provided by the cascoded structure reduces the noise current that can reach the tank, thus decreasing the modulation of  $I_1$  and  $I_2$ . Second, and more importantly, the variation on  $I_1$  induced by the noise generator is, to the first order, equal in magnitude and sign to the variation induced on  $I_2$ . Of course, this is again an approximation, being strictly true only if the switches are working in the triode region for the whole oscillation period, and if their combined effect can be modeled as a constant, large resistance  $R_S$  across phase 2 and phase 4 (Fig. 13). Under these conditions, the transistor noise injected into the tank is the same in the two phases. In fact, the  $1/f$  current noise power spectral density is proportional to  $g_m^2$  [22], while the noise transfer into the tank is given by  $(1/(1 + g_m R_S))^2 \cong 1/g_m^2 R_S^2$ . The product of the two terms is therefore independent of the current in the coupling transistor.

As shown in Fig. 14, a square current signal due to the slow varying noise is added to the ideal current waveform. Unlike the P-QVCO case, however, the frequency of this waveform is

<sup>6</sup>In reality, each switch visits the saturation region for a short time interval. Referring to Fig. 10, the switch on the left is pushed into saturation during a narrow time window at the center of phase 2 (phase 4 for the switch on the right). For most of phase 2, and for the rest of the oscillation period, the switch is in the triode region.

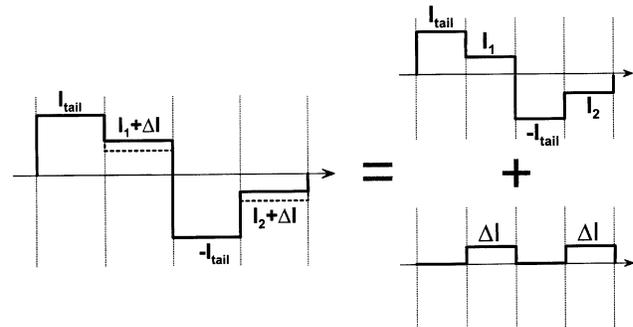


Fig. 14. Effect of the  $1/f$  noise generator in Fig. 13 (S-QVCO).

$2\omega_{\text{OUT}}$  and does not alter the first harmonic of the tank current, neither  $I_{I,1}$  nor  $I_{Q,1}$ . The contribution of this  $1/f$  noise to the output phase noise is therefore zero.

Obviously, in the real circuits, the previous approximations will work only to a limited extent. In particular, as mentioned in footnote 6, the switches are pushed into saturation for a time interval both in phases 2 and 4. The condition depicted in Fig. 14 thus represents a limit case, the best in terms of noise performance. On the other hand, if the switch was working in saturation during the whole phase 2, the transistor noise would reach the tank only under phase 4, a case analogous to the one sketched in Fig. 12. For the noise behavior of the real S-QVCO, we still expect a (strongly) reduced level of close-in phase noise, compared to the close-in phase noise for the P-QVCO.

The previous analysis can be validated by comparing its results with those obtained through SpectreRF simulations. For the P-QVCO, it is convenient to define the sensitivity  $K_{I_1}$  of  $\omega_{\text{OUT}}$  against fluctuations in  $I_1$ . In Appendix B, the following expression for  $K_{I_1}$  is derived:

$$K_{I_1} \equiv \frac{\partial \omega_{\text{OUT}}}{\partial I_1} = \frac{1}{4C} \cdot \left[ \frac{1}{4(1 - \delta)^2 I_{\text{TANK}} R_P} \right]. \quad (11)$$

The variation of  $I_1$  due to the current  $i_{\text{cpl}}$  (Fig. 11) is

$$\begin{aligned} \Delta I_1 &= 2i_{\text{cpl}} \frac{1/g_{m,\text{cpl}}}{1/g_{m,\text{sw}} + 1/g_{m,\text{cpl}}} \approx 2i_{\text{cpl}} \frac{1/W_{\text{cpl}}}{1/W_{\text{sw}} + 1/W_{\text{cpl}}} \\ &= 2i_{\text{cpl}}(1 - \delta) \end{aligned} \quad (12)$$

where the factor 2 is due to the currents being considered as fully differential, and where we have used the short-channel

*I*-*V* MOS equation for simplicity (the result is largely independent of this choice). The variation of  $I_1$  due to  $i_{sw}$  is found in an analogous way as

$$\Delta I_1 = 2\delta i_{sw}. \quad (13)$$

These two contributions for  $\Delta I_1$  will be added in power. From  $\Delta\omega_{OUT} \cong K_{I_1}\Delta I_1$ , the phase noise  $\mathcal{L}$  at a frequency offset  $\omega_m$  can now be calculated with the formula for narrow-band FM, yielding

$$\mathcal{L}(\omega_m) \cong 2K_{I_1}^2 \frac{S_{I_1}}{(2\omega_m)^2} \quad (14)$$

where  $S_{I_1}$  is the noise spectral density at low frequencies, superimposed onto  $I_1$ . As evident from Fig. 9, during phase 1 the current level  $I_2$  is slowly modulated by the noise of the other two transistors, and we obtain (see again Appendix B)

$$\frac{\partial\omega_{OUT}}{\partial I_1} = -\frac{\partial\omega_{OUT}}{\partial I_2}. \quad (15)$$

Thus, the noise on  $I_1$  and the noise on  $I_2$  add in power.

The numerical results yielded by this analysis for the P-QVCO are plotted (solid line) in Fig. 15. The close-in noise rises with the coupling strength, as expected from (11)–(14). These results can be compared with those from SpectreRF simulations (dashed line), for the same  $1/f$  noise level in the devices. The two curves have the same shape, which indicates that the up-conversion mechanism is the one discussed in this work. The maximum difference between the curves is approximately 4 dB and is due to the fact that the current waveform is in reality hardly the square wave represented in Fig. 9.

The noise simulation for the S-QVCO was carried out for  $G_{Mc}/G_M \cong 0.47$  ( $\delta = 0.3$ ), which is nearly a design constant (see the discussion in Section II). The close-in  $1/f$  noise has a nonzero value, because the noise perturbations on  $I_1$  and  $I_2$  due to a single noise source are not perfectly identical, as was instead assumed in Fig. 14. Switch transistors and coupling transistors contribute approximately the same amount of  $1/f$  noise.<sup>7</sup> The simulated  $1/f$  noise difference between P-QVCO and S-QVCO is approximately 9 dB.

## V. MEASUREMENT RESULTS

The S-QVCO has been fabricated [16] in a standard  $0.35\text{-}\mu\text{m}$  CMOS process with three metal layers of thickness less than  $1\ \mu\text{m}$  each. A die photograph is shown in Fig. 16. PMOS devices working in the accumulation and depletion regions have been used as varactors [23]–[25]. It must be recognized that the layout is clearly suboptimal, since the very long interconnections between the two coils introduce a significant amount of parasitic capacitance and, especially harmful, parasitic resistance. As a result, the estimated Q for each *LC* tank is approximately six at the frequencies of interest, while it was eight when the same tank was used in a single (nonquadrature) VCO [26]. As explained in Section II, we were allowed to assign  $\alpha$  the value which mini-

<sup>7</sup>Switch transistors contribute a substantial amount of upconverted  $1/f$  noise, despite the mentioned fact that the intrinsic  $1/f$  noise for a transistor working in the triode region is lower than in the saturation region, because of two second-order effects: the switch transistors do not always remain in the linear region (see footnote 6), and the conversion of  $1/f$  noise into phase noise for the switch transistors is strongly affected by the variations in their channel resistances across phases 2 and 4.

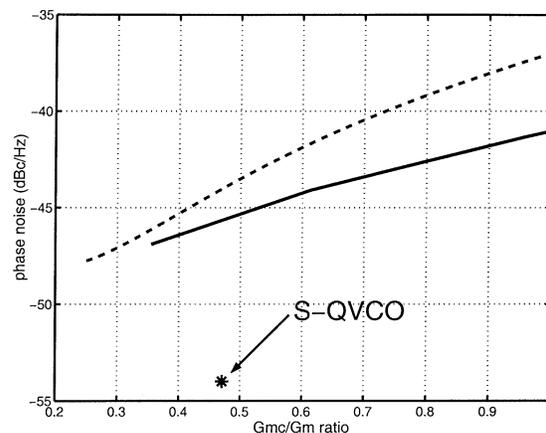


Fig. 15. Phase noise for the P-QVCO at a 1-kHz offset from the carrier, as a function of the coupling strength, obtained with SpectreRF simulations (dashed line), and with the theory developed in this work (solid line). The simulated phase noise difference between P-QVCO and S-QVCO is 9 dB.

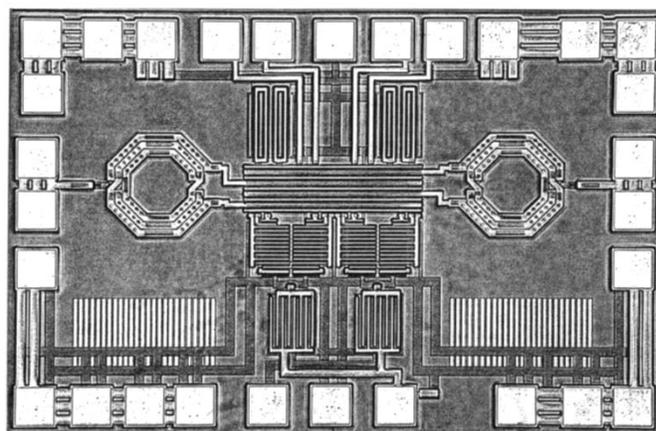


Fig. 16. Die photograph of the S-QVCO (chip dimensions:  $1.4\ \text{mm} \times 0.9\ \text{mm}$ ).

mized phase noise, since the phase error was almost independent of  $\alpha$ . As the phase noise varies but weakly around its minimum value, this optimization is very robust. For the present design, a value of five was chosen for  $\alpha$ . Table I shows dimensions and values for the various components in the S-QVCO and in the mixer used in the SSB upconverter.

### A. Phase Noise

All measurements have been performed with a 2-V power supply, for a current consumption of 25 mA in the core circuit. The S-QVCO could be tuned between 1.64 and 1.97 GHz, resulting in a tuning range in excess of 18%. As shown in Fig. 17, the phase noise at a 3-MHz offset from the carrier is  $-140\ \text{dBc/Hz}$  or less across the tuning range; Fig. 18 shows a plot of the phase noise for a carrier frequency of 1.82 GHz (the roll-off at offset frequencies higher than 5 MHz is an artifact of the Eurotest phase noise measurement system). The phase-noise FoM for the S-QVCO is calculated according to the commonly adopted expression [27]

$$\text{FoM} = 10 \log \left( \left( \frac{f_c}{\Delta f} \right)^2 \frac{1}{\mathcal{L}(\Delta f)P} \right) \quad (16)$$

where  $f_c$  is the oscillation frequency,  $\Delta f$  is the offset frequency, and  $P$  is the power consumption in milliwatts. Using the data in Fig. 17, the FoM ranges between 178 and 182 dB across the tuning range.

The noise filter technique described in [28] has been used in a second design of the same basic S-QVCO, since according to simulations this should afford a phase noise reduction between 2 and 3 dB across the tuning range. However, the parasitic capacitances extracted from the layout were severely underestimated, and the tuning range of the S-QVCO was in reality shifted down in frequency by approximately 200 MHz. Under such circumstances, the noise filter had in fact an adverse influence on the phase noise at lower oscillation frequencies (a fact well captured by post-measurement simulations). Further, the inductive degeneration of the tail transistors [29], [30], [26] leads in this case to very modest improvements (a 1-dB phase noise reduction at most across the tuning range), possibly due to the higher noise generated in the core circuit. As stated in [17], however, both the noise filter and the inductive degeneration technique should contribute an important phase noise reduction for higher LC-tank Q values.

1) *Comparison With Other QVCOs:* The *minimum* phase-noise FoM for the S-QVCO (which is, contrary to common practice, the truly relevant phase-noise data for a VCO) is approximately 3.5 dB lower than that for the QVCO in [14], which was built in a much more advanced CMOS process.<sup>8</sup> As a second phase-noise comparison, the already cited P-QVCO in [12] displays a minimum FoM 7 dB higher than the minimum FoM for the S-QVCO; however, this very good phase-noise behavior is at least partially obtained at the expense of the phase error, as explained in Section II (the phase error reported in [12] is indeed very large, but was obtained through unreliable, direct off-chip measurements).

### B. Phase Error

The IBR was measured with the same SSB upconverter used for the IBR simulations (Fig. 4). This circuit was implemented in yet another design, in order not to load the S-QVCO with both output buffers, needed to measure the phase noise, and mixers; this third S-QVCO oscillates at somewhat lower frequencies than the other two. The baseband (BB) quadrature signals are generated by an on-chip four-stage RC polyphase filter, while the S-QVCO outputs are directly fed to the gates of the transistors in the mixers. The measured deviation from quadrature derives of course from mismatches not only in the S-QVCO, but in the polyphase filter and mixers as well (a study of the impact of the passive mixer nonidealities on the IBR has been presented in [31]). The measured IBR is always equal or higher than 52 dB across the tuning range and for all seven tested samples. As an example, the IBR for one sample at a 1.75-GHz oscillation frequency is 56 dB (Fig. 19); the IBR as a function of the oscillation frequency for the same sample is shown in Fig. 20. Assuming that the IBR is entirely caused by a deviation from quadrature of

<sup>8</sup>This comparison is based on the usual definition of phase noise and not on the "quadrature" phase noise defined in [14], which, according to [14], would lead to a 6-dB higher FoM. According to our experience with SpectreRF simulations, the phase noise is almost independent of whether it is measured single-ended, differentially, or between quadrature phases.

TABLE I  
DIMENSIONS AND VALUES OF THE S-QVCO AND MIXER COMPONENTS

Transistors	
$M_{sw}$	$200\mu\text{m} \times 0.35\mu\text{m}$
$M_{cpl}$	$1000\mu\text{m} \times 0.35\mu\text{m}$
$M_{varactor}$	$1200\mu\text{m} \times 0.35\mu\text{m}$
$M_{src}$	$2000\mu\text{m} \times 1.0\mu\text{m}$
$M_{mixer}$	$100\mu\text{m} \times 0.6\mu\text{m}$
Reactors	
$L_{tank}$	$\approx 2.3\text{ nH}$
Q of the LC-tank	$\approx 6$ at 1.8 GHz

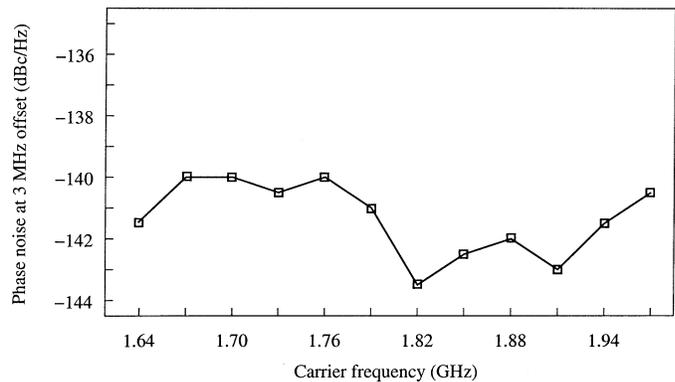


Fig. 17. Phase noise of the S-QVCO at a 3-MHz offset frequency, as a function of the oscillation frequency.

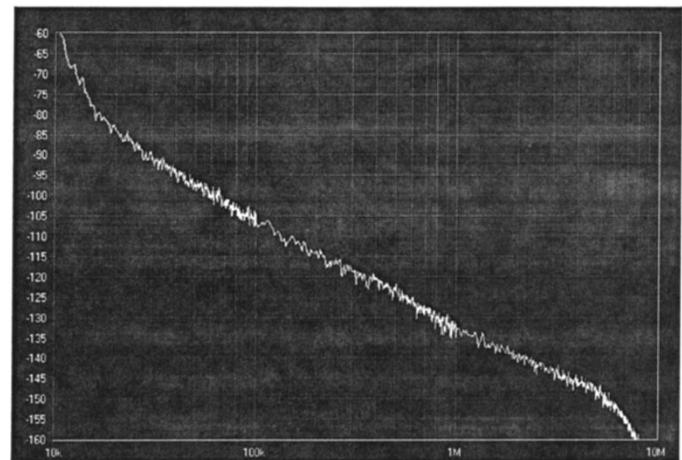


Fig. 18. Phase noise of the S-QVCO at a 1.82-GHz oscillation frequency.

the S-QVCO outputs, an IBR of 52 dB is equivalent to a phase error of approximately  $0.25^\circ$ .

## VI. CONCLUSION

This paper has presented a new design for a quadrature CMOS VCO, called the S-QVCO, which relies on the well-known technique of locking two independent LC VCOs to each other, but where the transistors coupling the two VCOs are placed in series with the cross-coupled switches implementing the negative resistances, rather than in parallel, as usual in the best known realization of a QVCO, here referred to as the P-QVCO. A simplified linear model has been developed which

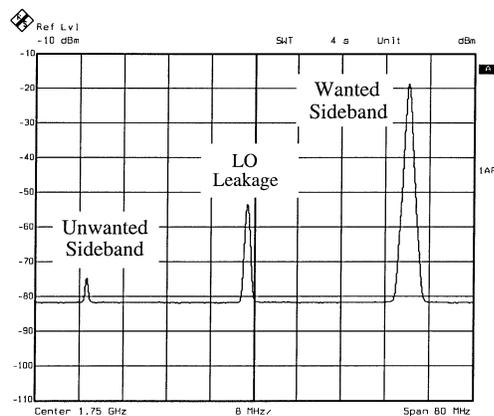


Fig. 19. Upconverted baseband signals and LO leakage at 1.75 GHz carrier frequency (IBR = 56 dB).

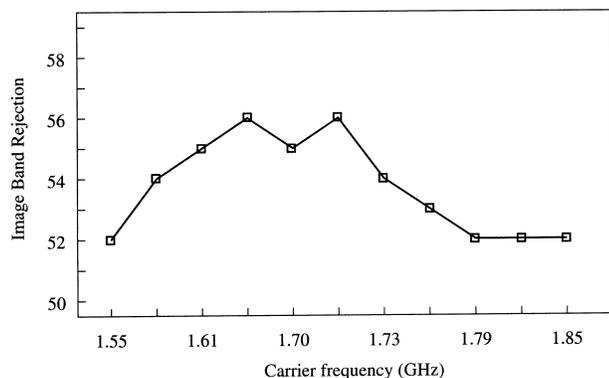


Fig. 20. IBR as a function of the oscillation frequency.

applies to both S-QVCO and P-QVCO, and the model has been used to derive the oscillation frequency of the QVCOs, and the influence of the various  $1/f$  noise sources on the generation of phase noise in the  $1/f^3$  region. This analysis provides quantitative results which agree well with the outcome of phase noise simulations performed with SpectreRF, indicating the superior performances of the S-QVCO compared to the P-QVCO. The measurement results for a prototype of the S-QVCO fabricated in a standard  $0.35\text{-}\mu\text{m}$  CMOS process show an oscillation frequency of 1.8 GHz, a tuning range of 18%, a phase noise of  $-140$  dBc/Hz or less at a 3-MHz offset frequency across the tuning range, and an equivalent phase error of at most  $0.25^\circ$ , for a current consumption of 25 mA from a 2-V power supply.

#### APPENDIX A

In this appendix, we find the possible oscillation frequencies for the linearized QVCO circuit in Fig. 7. The loop gain is easily calculated as

$$G_{\text{loop}}(s) = -G_{\text{Mc}}^2 \left( \frac{sL}{1 + sL(1/R_P - G_M) + s^2LC} \right)^2. \quad (17)$$

According to Barkausen's criteria, the circuit oscillates when the condition  $G_M = 1/R_P$  is satisfied; further, there are two

possible oscillation frequencies  $\omega_1$  and  $\omega_2$ , both differing from the natural tank resonance frequency  $\omega_0 = 1/\sqrt{LC}$ :

$$\omega_1 = \sqrt{\frac{LG_{\text{Mc}}^2 + 2C + \sqrt{L^2G_{\text{Mc}}^4 + 4LCG_{\text{Mc}}^2}}{2LC^2}}$$

$$\omega_2 = \sqrt{\frac{LG_{\text{Mc}}^2 + 2C - \sqrt{L^2G_{\text{Mc}}^4 + 4LCG_{\text{Mc}}^2}}{2LC^2}}. \quad (18)$$

These equations can be simplified noting that

$$\frac{G_M}{C} = \frac{1}{CR_P} \cong \frac{\omega_0}{Q} \quad (19)$$

$$G_M L = \frac{L}{R_P} \cong \frac{1}{\omega_0 Q} \quad (20)$$

and assuming that  $G_{\text{Mc}} \leq G_M$ . Using (20), we can approximate the inner square root in (18) as  $2G_{\text{Mc}}/\omega_0$ . According to (20), this term is much larger than  $LG_{\text{Mc}}^2$ , which can be neglected. Finally, using (19) and the approximation  $\sqrt{1+x} \approx 1+x/2$ , valid for  $x \ll 1$ , we arrive at

$$\omega_1 \cong \omega_0 + \frac{G_{\text{Mc}}}{2C}, \quad \omega_2 \cong \omega_0 - \frac{G_{\text{Mc}}}{2C} \quad (21)$$

which is the same as (2).

#### APPENDIX B

Equations (11) and (15) are derived in this appendix.

In the following, we call  $X$  the half-P-QVCO affected by noise sources (Fig. 11) and  $Y$  the other half. The low-frequency noise on  $I_1$  slowly modulates the quadrature current in  $Y$ , thus effectively modifying the coupling transconductance  $G_{\text{Mc}, Y \rightarrow X}$  from  $Y$  to  $X$ . Equation (10) yields

$$\frac{\partial G_{\text{Mc}, Y \rightarrow X}}{\partial I_1} = \frac{1}{A_0} \cdot \frac{\partial I_{Q,1}}{\partial I_1}. \quad (22)$$

Further, the same noise also varies the in-phase current in  $X$ , which modulates  $A_0$ , which changes the effective coupling transconductance  $G_{\text{Mc}, X \rightarrow Y}$  from  $X$  to  $Y$ . Using (10) again, we obtain

$$\frac{\partial G_{\text{Mc}, X \rightarrow Y}}{\partial I_1} = -\frac{I_{Q,1}}{A_0^2} \cdot \frac{\partial A_0}{\partial I_1}. \quad (23)$$

To estimate the effect on the frequency, we note that the term  $G_{\text{Mc}}$  appears squared in (17) and (18). It is therefore reasonable to define  $G_{\text{Mc}}$  in the expression of the loop gain as follows:

$$G_{\text{Mc}} = \sqrt{G_{\text{Mc}, X \rightarrow Y} \cdot G_{\text{Mc}, Y \rightarrow X}} \quad (24)$$

and therefore

$$\Delta G_{\text{Mc}} = \frac{1}{2} \Delta G_{\text{Mc}, X \rightarrow Y} + \frac{1}{2} \Delta G_{\text{Mc}, Y \rightarrow X}. \quad (25)$$

Using (25), the sensitivity of the oscillation frequency with respect to variations in  $I_1$  can be written as

$$\begin{aligned} \frac{\partial \omega_{\text{OUT}}}{\partial I_1} &= \frac{\partial \omega_{\text{OUT}}}{\partial G_{\text{Mc}}} \cdot \frac{\partial G_{\text{Mc}}}{\partial I_1} \\ &= \frac{1}{2} \cdot \frac{\partial \omega_{\text{OUT}}}{\partial G_{\text{Mc}}} \cdot \left( \frac{\partial G_{\text{Mc}, X \rightarrow Y}}{\partial I_1} + \frac{\partial G_{\text{Mc}, Y \rightarrow X}}{\partial I_1} \right). \end{aligned} \quad (26)$$

Simple but tedious manipulations of (2), (6)–(10), and (26) yield eventually

$$\frac{\partial \omega_{\text{OUT}}}{\partial I_1} = \frac{1}{2} \cdot \frac{1}{2C} \cdot \frac{1}{4(1-\delta)^2 I_{\text{TAIL}} R_P} \quad (27)$$

which is the expression for  $K_{I_1}$  given in (11).

Finally, the analysis above can be repeated unaltered when considering the effects of the noise on  $I_2$ , the only difference being the signs of  $I_1$  and  $I_2$  in (7) and (9). It is therefore straightforward to derive (15), repeated here:

$$\frac{\partial \omega_{\text{OUT}}}{\partial I_1} = - \frac{\partial \omega_{\text{OUT}}}{\partial I_2}. \quad (28)$$

#### ACKNOWLEDGMENT

The authors are pleased to acknowledge valuable interactions with I. Bietti at STMicroelectronics, Pavia, Italy; R. Castello at the Department of Electronics, University of Pavia, Italy; S. Mattisson and L. Sundström at Ericsson Mobile Platforms, Lund, Sweden; R. Strandberg at the Department of Electroscience, Lund University, Sweden; and J. van der Tang at the Mixed-Signal Microelectronics Group, Technical University of Eindhoven, The Netherlands.

#### REFERENCES

- [1] J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 269–282, Mar. 1998.
- [2] J. P. Maligeorgos and J. R. Long, "A low-voltage 5.1–5.8-GHz image-reject receiver with wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1917–1926, Dec. 2000.
- [3] P. T. M. van Zeijl, J.-W. Eikenbroek, P.-P. Vervoort, S. Setty, J. Tangenberg, G. Shipton, E. Kooistra, I. Keekstra, and D. Belot, "A Bluetooth Radio in 0.18  $\mu\text{m}$  CMOS," in *Proc. ISSCC 2002*, Feb. 2002, pp. 86–87.
- [4] J. Crols and M. S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.
- [5] M. S. J. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1895–1907, Dec. 2000.
- [6] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331–343, Mar. 1996.
- [7] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *Proc. ISSCC 1996*, Feb. 1996, pp. 392–393.
- [8] B. Razavi, "A 1.8GHz CMOS voltage-controlled oscillator," in *Proc. ISSCC 1997*, Feb. 1997, pp. 388–389.
- [9] T.-P. Liu, "A 6.5 GHz monolithic CMOS voltage-controlled oscillator," in *Proc. ISSCC 1999*, Feb. 1999, pp. 404–405.
- [10] J. J. Kim and B. Kim, "A low-phase-noise CMOS LC oscillator with a ring structure," in *Proc. ISSCC 2000*, Feb. 2000, pp. 430–431.

- [11] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 896–909, June 2001.
- [12] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1018–1024, July 2001.
- [13] A. M. ElSayed and M. I. Elmasry, "Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure," *IEEE J. Solid-State Circuits*, vol. 36, pp. 701–705, Apr. 2001.
- [14] P. Vancorenland and M. Steyaert, "A 1.57 GHz fully integrated very low phase noise quadrature VCO," in *Proc. 2001 Symp. VLSI Circuits*, June 2001, pp. 111–114.
- [15] P. van de Ven, J. van der Tang, D. Kasperkovitz, and A. van Roermund, "An optimally coupled 5 GHz quadrature LC oscillator," in *Proc. 2001 Symp. VLSI Circuits*, June 2001, pp. 115–118.
- [16] P. Andreani, "A low-phase-noise, low-phase-error 1.8 GHz quadrature CMOS VCO," in *Proc. ISSCC 2002*, Feb. 2002, pp. 290–291.
- [17] —, "Very low phase noise RF quadrature oscillator architecture," *Electron. Lett.*, vol. 37, no. 14, pp. 902–903, July 2001.
- [18] —, "A 2 GHz, 17% tuning range quadrature CMOS VCO with high figure-of-merit and 0.6° phase error," in *Proc. ESSCIRC 2002*, Sept. 2002, pp. 815–818.
- [19] C.-Y. Wu and H.-S. Kao, "A 1.8 GHz quadrature voltage-controlled oscillator (VCO) using the constant-current LC ring oscillator structure," in *Proc. ISCAS 1998*, vol. IV, May 1998, pp. 378–381.
- [20] M. Darabi and A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, pp. 15–25, Jan. 2000.
- [21] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, pp. 1323–1333, May 1990.
- [22] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
- [23] R. Castello, P. Erratico, S. Manzini, and F. Svelto, "A  $\pm 30\%$  Tuning range varactor compatible with future scaled technologies," in *Proc. 1998 Symp. VLSI Circuits*, June 1998, pp. 34–35.
- [24] T. Soorapanth, C. P. Yue, D. R. Shaeffer, T. H. Lee, and S. S. Wong, "Analysis and optimization of accumulation-mode varactor for RF ICs," in *Proc. 1998 Symp. VLSI Circuits*, June 1998, pp. 32–33.
- [25] P. Andreani and S. Mattisson, "On the use of MOS varactors in RF VCO's," *IEEE J. Solid-State Circuits*, vol. 35, pp. 905–910, June 2000.
- [26] P. Andreani and H. Sjöland, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 342–348, Mar. 2002.
- [27] P. Kinget, *Integrated GHz Voltage Controlled Oscillators*. Norwell, MA: Kluwer, 1999, pp. 355–381.
- [28] E. Hegazi, H. Sjöland, and A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921–1930, Dec. 2001.
- [29] P. Andreani and H. Sjöland, "A 2.2 GHz CMOS VCO with inductive degeneration noise suppression," in *Proc. CICC 2001*, May 2001, pp. 197–200.
- [30] —, "A 1.8GHz CMOS VCO with reduced phase noise," in *Proc. 2001 Symp. VLSI Circuits*, June 2001, pp. 121–122.
- [31] A.-K. Stenman, "Some design aspects on RF CMOS LNA's and mixers," Tech. Licentiate Thesis, Dept. of Electroscience, Lund University, Lund, Sweden, Dec. 2001.



**Pietro Andreani** (S'98–A'99–M'01) received the M.S.E.E. degree from the University of Pisa, Pisa, Italy, in 1988 and the Ph.D. degree from Lund University, Sweden, in 1999.

He joined the Department of Applied Electronics, Lund University, in 1990, where he contributed to the development of software tools for digital ASIC design. After working at the Department of Applied Electronics, University of Pisa, as a CMOS IC Designer during 1994, he rejoined the Department of Applied Electronics, Lund University, as an Associate Professor, where he was responsible for the analog IC course package between 1995 and 2001. He is currently a Professor at the Center for Physical Electronics, Ørsted-DTU, Technical University of Denmark, Kgs. Lyngby, Denmark, with analog/RF CMOS IC design as main research field.



**Andrea Bonfanti** was born in Besana B.za (Milan), Italy, in 1972. He received the Laurea Degree in electronics engineering from the Politecnico di Milano, Milan, Italy, in 1999. He is currently working toward the Ph.D. degree in electronics and communications at the Politecnico di Milano and his activity is focused on the design of oscillators for wireless applications.

His research interests also include *RF* frequency synthesizers and  $\Sigma$ - $\Delta$  analog-to-digital converters.



**Luca Romanò** was born in Milan, Italy, in 1976. He received the Laurea Degree in electronics engineering from the Politecnico di Milano, Milan, Italy, in 2001. He is currently working toward the Ph.D. degree in electronics and communications at the Politecnico di Milano.

His activity is focused on the design of fully-integrated frequency synthesizers for wireless applications in CMOS and BiCMOS technologies. His current research interests also include noise analysis in *RF* oscillators and frequency dividers.



**Carlo Samori** (M'98) was born in 1966 in Perugia, Italy. He received the Laurea Degree in electronics engineering in 1992 and the Ph.D. degree in electronics and communications from the Politecnico di Milano, Milan, Italy, in 1995.

In 1996, he was appointed Assistant Professor of Electronics at the Politecnico di Milano. He worked on solid state photodetectors and associated front-end electronics. His current research interests include design and analysis of integrated circuits for communications in bipolar and CMOS technologies, noise analysis in oscillators, and frequency synthesizer architectures. Since 1997, he is a consultant of wireless Circuit Research Department at Agere Systems, Bell Labs.