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Søbjærg, Sten Schmidl; Christensen, Erik Lintz

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2 GHz Self-aligning Tandem A/D Converter for SAR

Sten Schmidl Søbjærg and Erik Lintz Christensen
Ørsted•DTU, Technical University of Denmark,
DK-2800 Kgs. Lyngby, Denmark (e-mail: sss@oersted.dtu.dk).

Abstract-- A new generation of the Danish synthetic aperture radar system (EMISAR) is under development targeting a bandwidth of 800 MHz and a corresponding range resolution of around 25 cm. Two alternative approaches to achieve the wide bandwidth are considered. The one is to use analog I/Q demodulation before digitizing, and the other is to digitize the signal before digital I/Q demodulation [1]. In both cases the digitizing may be performed by a digital front end (DFE) with two parallel analog-to-digital-converters (ADCs) sampling at 1 GHz in phase or in anti-phase respectively, provided the analog bandwidth of the ADC is sufficient. In the first case each ADC has to digitize a 0-400 MHz signal, and in the second case both ADCs have to digitize a 100-900 MHz signal. In both cases the sampling time alignment is a critical parameter. The paper addresses some aspects of ADC alignment in the implementation of a DFE for the EMISAR system.

I. Introduction

Two ADCs in tandem can be used to double the sampling rate provided the analog bandwidth of the ADCs is sufficiently high and the sampling timing is properly aligned. A digital correlator can be used for automatic control of the sampling time. The correlator multiplies the input signals from the two ADCs and integrates the product, and the result is used as feedback to programmable digital delay devices in the clock circuit of each ADC. The delay devices allow a direct digital adjustment of ± 2 ns, and a fine-tuning to sub-picoseconds, using an analog input.

II. Correlation Measurement

For a radar using a coded pulse with a large time-bandwidth product, the reflected radar signal may be regarded as a stochastic signal with a Gaussian voltage distribution. For the two channel case, the input voltage may be regarded as two stochastic, Gaussian distributed variables, X and Y, characterized by the mutual correlation, ρ. The joint probability density function will have the form

$$p(x,y)=\frac{1}{2\pi\sigma^2\sqrt{1-\rho^2}}\exp\left(\frac{-\left(x^2+y^2-2\rho xy\right)}{2\sigma^2\left(1-\rho^2\right)}\right) \qquad (1)$$

where σ is the rms. signal level in each channel.

The correlator will sample, multiply, and integrate the two input voltages during a specified time, and the output will be given by

$$\rho=\frac{\langle X(t)*Y(t)\rangle}{\sqrt{\langle X^2(t)\rangle\langle Y^2(t)\rangle}} \qquad (2)$$

where "<>" represents the mean over the period T. For Gaussian distributed signals, the mean-square values will approach the rms. signal levels, σ_x and σ_y, for the two channels for long integration times.

The length of the integration period, T, is determined by the required precision in the measurement. Generally, for a Gaussian distributed signal, the standard deviation on the correlation measurement is given by

$$\Delta\rho=\frac{\sqrt{1+\rho^2}}{\sqrt{f_S T}} \qquad (3)$$

where f_s is the sampling frequency of the correlator. The standard deviation will be degraded, however, if subsequent samples are correlated, e.g. due to over-sampling.

Assuming a rectangular frequency characteristic, the autocorrelation function will be a sinc function

$$R(t)=\frac{\sin(2\pi Bt)}{2\pi Bt} \qquad (4)$$

where B is the signal bandwidth. The maximum will occur at zero delay difference, and zeros will be found at $t=n/(2B)$, where n is an integer. The situation for $n=1$ is the Nyquist sampling, but it is seen from the autocorrelation function, that the independence condition is fulfilled for all subsets of the signal, when sampled at Nyquist.

III. The Self-aligning parallel I/Q Receiver

The traditional wide-band DFE implementation includes two parallel channels for sampling an I/Q demodulated signal. In this application, a total bandwidth of 800 MHz is desired, and it may be implemented, using two ADCs, sampling simultaneously at 1 GHz.

For a single frequency input, the correlator output is a measure of the sampling misalignment between the two ADCs added to the phase difference from the demodulator. Assume sinusoidal signals, having the amplitudes, $A_1=A_2=\mathrm{sqrt}(2)$, and the phase difference, φ, applied to the input channels. The correlator output will be

$$\rho = \frac{1}{T}\int_0^T \sqrt{2}\cos(2\pi ft)\sqrt{2}\cos(2\pi ft+\varphi)dt \quad (5)$$

which may be rewritten as

$$\rho = \frac{1}{T}\int_0^T \cos(4\pi ft+\varphi)dt + \frac{1}{T}\int_0^T \cos(\varphi)dt \quad (6)$$

The first term will give a zero mean, and a standard deviation depending on the integration time. The latter term directly gives the cosine of the phase difference.

For a perfect I/Q demodulation in front of the correlator, a single frequency input signal results in correlator input signals, separated 90 degrees. The output may be considered as $\varphi_t = \pi/2+\varphi_e$, where φ_t is the total measured phase difference, and φ_e is the phase error caused by the ADC timing error. Removing $\pi/2$ causes a change from cosine to sine in the correlator output, directly giving the relation

$$\rho = \sin(\varphi_e) \quad (7)$$

The delay error may be calculated from

$$t_D = \frac{\varphi_e}{2\pi f} \quad (8)$$

when the input frequency is known. For an input signal consisting of a band of frequencies, *B*, the measured quantity will be an average over the band, and the output correlation will be determined by

$$\rho = \frac{1}{B}\int_{f_1}^{f_2} \sin(2\pi f t_D)df \quad (9)$$

Unfortunately a consequence of this result is, that a symmetric band of frequencies around f_0=0 will always give a zero correlation for any delay error. It is hence not possible to use the normal radar input signal as basis for the correlation calculation, and a dedicated test signal is needed during delay alignment.

A limitation on the test signal frequency is noted. The sinusoidal behavior of the correlation function causes delay error ambiguity at high frequencies, or at relatively long delays. Long delays, exceeding the unambiguous range may appear at system initialization due to the manufacturing tolerances and temperature differences, and it must be solved online by injection of a low frequency calibration signal during system initialization. Subsequent drift can be corrected automatically by a simple regulation system during the measurement sequence, as time slots without data recording will be free to apply the test signal and correct the alignment.

An obvious problem in the analog I/Q demodulation is the DC offset. Since the correlator is a simple multiplier with integration, it will not only be sensitive to the signal I/Q correlation, but it will also be strongly influenced by any DC in the I and/or Q signals, and this error must be eliminated before the correlation calculation.

A DC in I, V_I, and in Q, V_Q, will change the output to

$$\rho_{DC} = \rho + V_I V_Q \quad (10)$$

where ρ is the true correlation. The traditional way of solving offset problems in a digital correlator is by phase shifting the test signal. It includes application of a modulation function to the input signals before the ADC and, using orthogonal modulations for the two channels, the DC can be eliminated. The simplest modulation functions may be a constant, $m_1(t)$=1, to the I channel and a 50% duty cycle, $m_2(t)$=±1, to the Q channel. For $m_2(t)$=+1, the output from the correlator will be equal to the situation without modulation, while the $m_2(t)$=-1 period will give

$$\rho_{DC} = -\rho + V_I V_Q \quad (11)$$

With the 50% duty cycle, the true correlation may be found directly by subtraction.

An alternative solution to the DC offset problem might be adjusting the offset directly on the ADC. As it is sensitive to temperature drifts, however, it needs frequent correction, and for a coherent radar application, the DC in the I and Q channels contain information, which makes it problematic to use the normal data for DC offset determination. An obvious solution is again to take advantage of the test signal, used for delay adjustment, and as this signal can be generated DC free, a simple integration of the signal voltage will provide sufficient information on the DC level, and the ADC DC adjust voltage can be set.

IV. The Digital Demodulator

An alternative solution to the DFE implementation uses digital I/Q demodulation after down-conversion to e.g. 500 MHz±400 MHz and sampling and digitizing the full-bandwidth signal at 2 GHz. This approach requires a 2 GS/s ADC or a tandem pair of ADCs with at least 2 GHz analog bandwidth, clocked at 1GHz with 180 degrees phase difference.

The input signals to each of the two ADCs will be exactly equal, but using digital demodulation with carrier reference signals $\sin(\omega_S/4*t)$ and $\cos(\omega_S/4*t)$, where ω_S is 2π times the sampling frequency, the usual I and Q channels are generated. [1 and 2].

The correlation technique can be used for delay adjustment. In this case each of the ADCs with a sampling frequency of 1 GHz will under-sample the signal. The full bandwidth input signal will appear aliased in the sampled spectra, which will, however, still represent the original bandwidth. This results in an autocorrelation function, which will still give its maximum, ρ_A=1, for t=0, and which will decrease monotonously until t=1/2B. Taking advantage of the symmetry of the autocorrelation function, an algorithm for adjusting the delays can be developed.

With the normalized sampled signals from each of the two ADCs, $v_{1,1}$, $v_{1,2}$, $v_{1,3}$… and $v_{2,1}$, $v_{2,2}$, $v_{2,3}$… respectively, two correlations can be calculated

$$\rho_1 = \sum_{n=1}^{N} v_{1,n} v_{2,n} \qquad \rho_2 = \sum_{n=1}^{N} v_{1,n} v_{2,n+1} \tag{12}$$

where N is the integration length. First assume that the two ADCs have been adjusted to simultaneous sampling. It means, that the correlation, ρ_1, will be equal to 1, as samples are identical, while the correlation, ρ_2, will be equal to the autocorrelation for $t=1/f_s$. Now increasing the sampling delay between the two ADCs, ρ_1 will decrease, while ρ_2 will increase. Adjusting until the difference between the two correlations is zero will lead to a perfect alignment of the two sampling times (i.e. sampling in anti-phase).

Similar to the situation when using analog I/Q demodulation, the manufacturing tolerances and temperature differences can cause ambiguities to occur, and at system power up, there must be a coarse adjustment of the two ADCs to approximately equal delays. Subsequent one delay may be increased by 1/(2GHz) = 500 ps to reduce the settling time of the regulation loop.

The initial coarse alignment can be performed by applying a slow cosine test signal at the input. This will result in a cosine autocorrelation with maximum at t=0, slowly decreasing according to the frequency of the signal. At this point the regulator should search the maximum correlator output, which can be done by a simple iterative regulation.

With the offset input frequency it is possible to use the radar signals to adjust the DC offset, and a simple integrator, which integrates the signal amplitudes continuously, will provide sufficient information on the DC level to set the regulation voltage directly on the ADC.

V. The complete digital front end

The complete DFE is constructed to support both types of demodulation. This is achieved by connecting the two ADCs to a large field programmable gate array (FPGA), which will store the sampled data and regulate the sample delays.
As the correlator includes an 8*8 multiplier, according to the number of bits from the ADC, and a large adder to perform the integration, it is a major challenge to utilize the full bandwidth, when sampling at 1 GHz per ADC. In the FPGA these functions must be paralleled by a factor of 8, increasing significantly the amount of resources needed. An obvious solution is to limit the sampling speed, since it has been shown, that an under-sampling will not influence the result of the correlation, while the standard deviation will be increased by a factor of sqrt(N), when under-sampled by a factor of N.

An alternative to the under-sampling is a reduction of the number of bits in the calculation of the correlation. It can be shown [3], that even a severe reduction, down to a single bit, will only increase the standard deviation by a factor of $\pi/2$ compared to a real number representation. And with 2 bits, the loss is down to a factor 1.14.

VI. Conclusions

This paper describes the implementation of a digital front end for the EMISAR system, using two 1Gs/s A/D converters in tandem to achieve a bandwidth of 800 MHz. For traditional I/Q operation, it is shown, that a test signal is necessary to carry out the sampling delay alignment, since the full bandwidth I and Q signals will always de-correlate. DC offset canceling must be available, as the correlator result will be corrupted by the presence of DC. As the coherent radar signal contains a DC component, either a correction of the ADC input circuit using the test signal must be implemented, or phase switching must be applied.

The alternative digital front end implementation samples directly the 800 MHz bandwidth signal with 500 MHz center frequency, clocking the two ADCs 180 degrees out of phase. In this case the DC adjustment is simple, as the radar data, which contain no DC component, may be used directly. Likewise the sampling delay adjustment can be carried out using the radar data, and it is shown, how a simple measurement of the autocorrelation can be used to adjust the clock delays.

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