Schottky barrier enhancement on n-InP solar cell applications

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SCHOTTKY BARRIER ENHANCEMENT ON N-INP - SOLAR CELL APPLICATIONS

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ABSTRACT

It is demonstrated that the Schottky barrier height on n-type InP can be enhanced to values close to the energy bandgap (1.35 eV) by employing a AuZnCr metallization. The process is simple and requires only mild and fast annealing sequences with temperatures not exceeding 500°C. Also, no critical epitaxial growth step of junctions is needed, making the process fairly cheap. Thus, prospects for an efficient and simple solar cell device structure for space application purposes based on highly radiant-resistant InP are greatly improved.

INTRODUCTION

InP is considered to be a superior material for solar cell devices for space applications in comparison with Si and GaAs because of its high radiation tolerance [1,2]. Theoretically, for Schottky barrier solar cells (SBSC) based on InP, a maximum conversion efficiency of about 25% is possible if a Schottky barrier diode with a barrier height close to the energy bandgap, E_g, can be realized [3]. This has been considered impossible due to surface states between the metallization and the InP, pinning the barrier height on n-type InP to values around $E_g/3$. In this paper we demonstrate that the surface states can be depinned and that the Schottky barrier height on n-type InP can indeed have values close to E_g.

EXPERIMENTAL

Circular Schottky barrier diodes (diameter:500-5000 μm) were defined in a sputter deposited SiO_2 layer (200 nm) passivating the undoped n-type InP (10^{15} cm^{-3}) wafers by evaporation of a AuZnCr layered metallization (Au(50nm)/Cr(25nm)/Zn(100nm)/Au(2nm)). AuGe was deposited on the back of the wafers for reliable large-area contacts. Rapid thermal annealing (RTA) was employed to activate the Schottky barrier diodes. Temperatures were in between 440°C and 500°C for a constant annealing time of 20 sec. with fast ramp-ups (100°C/sec.) and free ramp-downs.

For electrical characterization of the contacts the samples were mounted on an aluminum chuck in a probing station. Vacuum on the backside of the samples ensured a good backside contact to the chuck. I-V measurements

for the diodes were performed by sweeping an appropriate voltage range (from -1 V to 0.8 V) then measuring the associated current through the diode, using a HP 4140B pA meter/DC voltage source-HP PC-AT set-up. C-V measurements for the diodes were performed using a HP 4280A 1 MHz C meter/C-V plotter-HP PC-AT set-up and the same probing station set-up as for the I-V measurements. The applied voltage was swept from -1 to a maximum of 0.2 V. Deep level transient spectroscopy (DLTS) was utilized to ascertain whether or not recombination levels were forming in the bandgap region under the processing of the contacts. A computer controlled Semilab 82E DLTS system was utilized, and the n-type diodes were placed in a continuous flow liquid nitrogen cryostat which could be cycled in between 80 and 400 K.

RESULTS AND DISCUSSION

The forward I-V characteristics for the diodes annealed at 440°C, 460°C, 480°C and 500°C are shown in Fig. 1. As can be seen, a large series resistance limits the current flow in the diodes for high current outputs. This is reasonable considering the high resistivity of the wafers (undoped), but the resistance of the metallization itself is also limiting the current flow (Fig. 1). The series resistance can be reduced by employing n-n$^+$ wafers with thin low doped layers (10^{16}-10^{17} cm^{-3}) deposited on heavily doped carrier wafers. Diodes annealed below 440°C showed poor ohmic behaviour. Diodes annealed above 500°C were not of a Schottky type, indicating diffusion of metallization elements into the bulk InP creating either a multiple of pn-junction diodes or recombination centers in parallel with Schottky diodes. The breakdown of the Schottky barrier diodes is initiated at the periphery of the diodes. This is demonstrated in Fig. 1d for diodes annealed at 500°C. Diodes with a large periphery/area ratio have poorer I-V characteristics than diodes with a small periphery/area ratio (Fig. 1d). From our observations the degradation from Schottky characteristics gets severe when the annealing temperature exceeds 500°C. I-V-T measurements, where the temperature T was varied from 25°C to a maximum of 175°C, was performed to judge on the transport limitations for electrons crossing the metal-semiconductor barrier. From Richardson plots it was found that the transport across the MS interface was limited by thermionic emission.
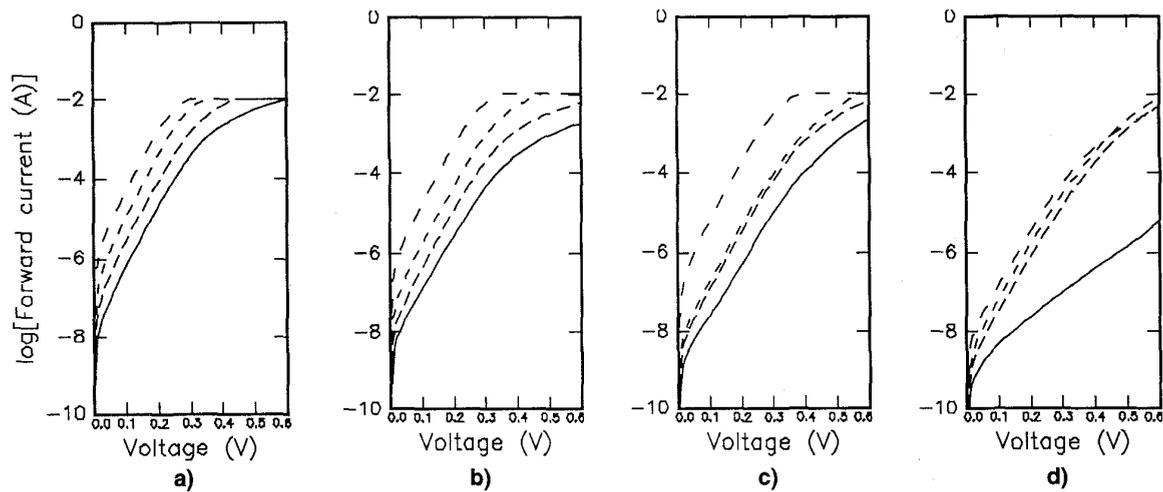
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Fig. 1 Forward I-V characteristics for different diameter AuZnCr/n-InP diodes annealed at a) 440°C, b) 460°C, c) 480°C and d) 500°C. Solid lines; 500 μm, dashed lines; 1000 μm, dashed-dotted lines; 2000 μm, dotted lines; 2500 μm and dashed-dotted-dotted lines; 5000 μm.

In Fig. 2 the $1/C^2$-V characteristics for the diodes are shown. From these, information about the height of the Schottky barrier can be obtained by extrapolating to the zero crossing of $1/C^2$ with the voltage axis. The $1/C^2$-V dependence for the diodes annealed at 460°C and 480°C are almost identical, and thereby lines in the plot are merged. There is a slight deviation from linearity for all the lines, and this is not in accordance with standard theory in which lines should be linear with values of the slopes determined by the background doping density. We will comment on this deviation in the discussion to follow.
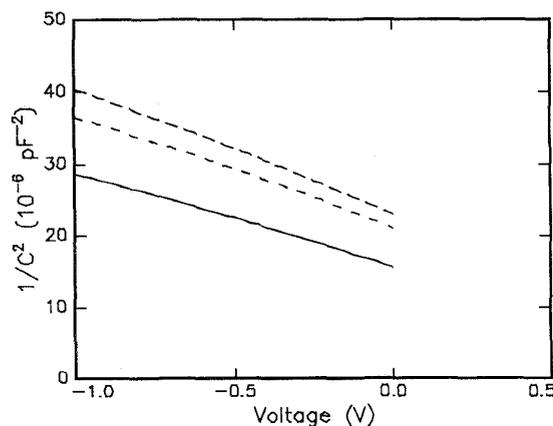
In Fig. 3, the Schottky barrier height and the ideality factor deduced from the I-V (using the intercept with the log J axis in a linear fit) and C-V measurements in Fig. 1 and 2 are plotted as a function of the annealing temperature. As can be seen from this figure, values of the Schottky barrier height close to 0.8 eV can be obtained from I-V measurements, while values of the Schottky barrier height close to the energy bandgap are deduced from C-V measurements. The reason for the large discrepancies between the I-V and the C-V method arise because the I-V method is more sensitive to low barrier phases at the interface between the

Fig. 2. C-V characteristics for AuZnCr/n-InP diodes annealed at 440°C (solid line), 460°C (dashed line), 480°C (dashed-dotted line) and 500°C (dotted line).
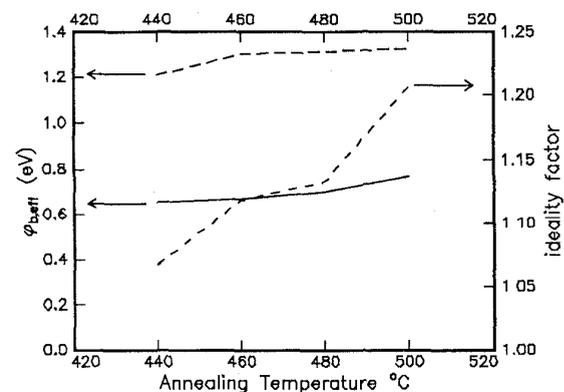

Fig. 3. Effective Schottky barrier height from I-V measurements (solid line) and C-V measurements (dashed line) as a function of the annealing temperature. Also shown is the corresponding ideality factor (dashed-dotted line) from I-V measurements.

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metallization and the InP than is the C-V method [4,5]. This will be discussed in more detail in the discussion.

Results from DLTS measurements showed that no deep levels had formed in the bandgap for annealing temperatures below 500°C. At 500°C a donor level formed ~0.59 eV below the conduction band edge. The most probable cause of the deep donor level is diffusion and activation of Au, as Au has a deep donor level located 0.55 eV below the conduction band level in InP.

DISCUSSION

The performance of a solar cell diode is governed solely by its I-V characteristics and not by its C-V characteristics. Thus, the maximum achievable barrier height from this experiment is around 0.8 eV, but by further optimizing the metallization layer sequence of the diode we believe that a barrier height close to the energy bandgap limit can be obtained. One of the biggest drawbacks of a Schottky barrier solar cell is the shadowing effect from the metallization electrodes. Moreover, the metallization used is rather thick and consists of Au. Therefore, the losses due to reflection are high. We will discuss the shadowing effect of the metallization and the low I-V barrier height (as compared to the C-V barrier height, Fig.3) of the diodes in more detail later in the discussion and present possible device structures that perhaps can minimize some of these deleterious effects. First, however, we will discuss the reason for the barrier height increase.

Enhancing the Schottky barrier height on n-type InP has been considered a difficult task to overcome, because of the insensitivity of the surface to almost all metals [6]. Careful processing and annealing is one way to make the semiconductor surface more sensitive to the metallization, and we have been reporting on the properties of standard Au-based ohmic contact metallizations to both n- and p-type InP [7-11]. In brief, we have found that the value of the specific contact resistance is closely related to the effective Schottky barrier height, $\phi_{b,eff}$, where $\phi_{b,eff}$ is the weighted average of all the different Schottky barrier structures in the contact taking into account their individual surface coverage. Thus, the lowest value of the specific contact resistance is obtained in a contact with maximum interfacial coverage of the Schottky barrier structure with the lowest barrier height [7-10]. The same of course applies to an annealed multilayer metallization Schottky diode with a multiple of Schottky barrier structures. In this case, however, low barrier height structures should be avoided, because they will have a dramatic effect on the measured value of $\phi_{b,eff}$ even with low surface coverages [4,5,10-11].

The mechanism responsible for the modulation of the effective Schottky barrier height is believed to be the formation of stable Zn-P phases in contact with the InP [7-11]. Formation of non-metallic Zn_3P_2 precipitates in the InP crystal with a well defined epitaxial relationship has been observed both by Eger et al. [12] by diffusing Zn into InP

and by Nakahara et al. [13] by evaporating Zn layers onto InP and annealing the MS contacts thereby formed. We believe that the Zn_3P_2 epitaxial formation is responsible for the ohmic behaviour that we observe for the AuZn-based metallizations to p-type InP and the Schottky behaviour that we observe for the AuZn-based metallizations to n-type InP. Zn-P phases can have semiconducting properties when prepared properly, and Zn_3P_2 has actually been considered as a potential for photovoltaic devices [14-17]. Thin films of Zn_3P_2 have been applied to an n-type sample in order to make abrupt p_+-n junctions with Zn diffusion [18]. It was found that diffusion started at 500°C for the annealing times employed [18]. This indicates that the Zn_3P_2/InP interface are abrupt for annealing temperatures below 500°C.

From the results presented above and the discussion on the mechanisms responsible for enhancing the barrier height we believe that semiconducting or semimetal highly doped p-type crystallites form in an epitaxial contact with the n-type InP forming a heterotype local Schottky barrier structure. This heterotype of Schottky diode locally gives the desired bandmodulation, and the multiple of high barrier height heterotype Schottky barriers in parallel with local lower barrier height diodes adds up to form an overall high barrier height diode. The heterotype structures must have a larger area in comparison with the local lower barrier height diodes in order to effeciently "pinch off" the effects of the lower barrier height diodes [4,5]. Also, due to the different barrier heights, the $1/C^2$-V plots (Fig. 2) can not be expected to be linear [4].

Au was added to the metallization in order to have a "sink" for outdiffusing In elements and to create an excess of P for Zn-P interactions [7-11]. Thus, Au is vital for the success of the experiment. However, Au should be avoided from the viewpoint of reflection losses. This inconsistency may limit the usefulness of the results with respect to the developement of a highly efficient Schottky barrier solar cell device. In Fig. 4 we propose a basis for a new solar cell device based on AuZnCr metallizations to n-type InP that possibly can circumvent some of these problems. As a first step metallization stripes are patterned in the protective SiO_2 layer passivating the surface of the InP as described in the experimental details given above. After the annealing the SiO_2 layer is removed in BHF followed by a $HCl:H_3PO_4$ etch for making a groove structure that maximizes the surface area of the diodes. An optimized etch process of InP using SiO_2 protective layers and $HCL:H_3PO_4$ etchants has been reported by us recently [19]. The etch process will somewhat underetch the metallization, but this is believed to be beneficial, because then breakdown at the periphery of the diodes is avoided. As a last step a thin film of Zn_3P_2 may be deposited on the sides of the grooves (Fig. 4) prior to an antireflection coating step to passivate and possibly create a heterojunction diode structure at the side of the grooves. However, annealing of that junction type should be mild in order not to disturb the AuZnCr/InP
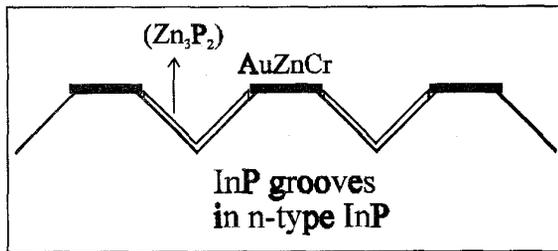
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Fig. 4. New Schottky barrier solar cell device structure.

diodes or annealing should also include the activation of the AuZnCr/InP diodes. A much simpler structure is of course the groove structure without AuZnCr/InP diodes, but with Zn_3P_2 coating of the whole surface area. Then the restrictions on the annealing sequence are somewhat looser, and an epitaxial growth method can maybe be used to grow the thin p-type Zn_3P_2 layer at reduced temperatures. The reduction of the processing temperature will minimize interdiffusion between the Zn_3P_2 layer and the InP crystal, ensuring the formation of an abrupt junction.

CONCLUSIONS

We have demonstrated that the Schottky barrier height on n-type InP can be enhanced by employing a AuZnCr metallization. From C-V measurements the barrier height is close to the energy bandgap of InP (1.35 eV). However, due to the presence low barrier height structures in parallel with the Zn-P based high barrier height structures the effective barrier height measured with I-V techniques is somewhat lower. Degradation starts at 500°C annealing and is caused mainly by diffusing Au and Zn, creating deep levels and pn-junctions in parallel with the Zn-P based high barrier height structures. A new device based on these findings that takes into account some effects of the metallization have been proposed, but not yet tested. Also, a new heterojunction device based on an epitaxial relationship between Zn_3P_2 and InP has been discussed.

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