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Published in:

Proceedings of the IEEE Instrumentation and Measurement Technology Conference

Link to article, DOI:

[10.1109/IMTC.1995.515120](https://doi.org/10.1109/IMTC.1995.515120)

Publication date:

1995

Document Version

Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

Citation (APA):

Kaulberg, T., & Bogason, G. (1995). Position detection with the use of MAGFETs. In *Proceedings of the IEEE Instrumentation and Measurement Technology Conference* (pp. 158-158). IEEE.
<https://doi.org/10.1109/IMTC.1995.515120>

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Position detection with the use of MAGFET's

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January 30, 1995

Abstract – An angledetector with a digital output is described. The component is meant as an alternative to the traditional slide potentiometer used as volume control in many hearing aid applications. The component is based on the use of magnetic field sensitive MOSFET's (MAGFET's) detecting the position of a tiny bar magnet placed above a silicon chip. Because of the galvanic separation between the angle-setting bar magnet and the electrical circuit, this component is insensitive to the rather hostile environment hearing aids are exposed to. The lifetime of the component is thereby increased significantly. The electrical circuit contains a switched current A/D – D/A conversion system for offset compensating the MAGFET's and for converting the MAGFET signal currents into a digital output proportional to the input angle. It is implemented using a commercially available $1.5 \mu\text{m}$ CMOS process.

I. INTRODUCTION

The volume control in hearing aid systems is often realized with a traditional slide potentiometer. Due to the hostile and humid environment in which it has to operate and the galvanic contact between the metal pointer and the carbon slide, the lifetime of the component is rather limited. One way of avoiding the galvanic contact is letting magnetic field sensitive transistors detect the position of a movable bar magnet as shown by Figure 1. An iron disk is placed beneath the chip to focus the magnetic field applied to the MAGFET's. The bar magnet can make a 2π turn (there can be a physical stop to make only one turn possible) and two MAGFET's are used. One is placed at the angle $\theta = 0$ and one is placed at the angle $\theta = \pi/2$.

On the assumption that the differential output current of a MAGFET is proportional to the magnetic flux through it [3], a possible *Angle to Current*-transfer function is showed in Figure 2. $I_{D,M1}$ and $I_{D,M2}$ are the differential output currents of the two MAGFET's M1 and M2. The exact transfer function is a rather complex function of the dimensions of the bar magnet, the placement of the MAGFET's and the chosen materials.

From Figure 2 it is clear that any angle position unambiguously can be detected. This paper describes a solution

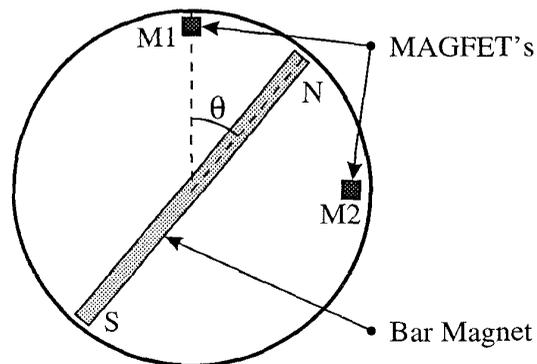


Figure 1: The Angledetecting system

where the angle position is to be represented by a 7 bit digital number proportional to the input angle. The two most significant bits (MSB) can be determined by simply reading the signs of the two MAGFET currents. This will divide the input angle into four equally sized intervals which can be represented by the two most significant bits. The third MSB can be provided by comparing the two currents numerically, $|I_{D,M1}| > |I_{D,M2}|$. The four least significant bits can be generated by A/D converting the numerically smallest current using the numerically largest current as a reference. This is in effect a division expressed by Eq. (1).

$$4 \text{ LSB} = f_{\text{dec}}(D_3 \dots D_0) = \frac{\min\{|I_{D,M1}|, |I_{D,M2}|\}}{\max\{|I_{D,M1}|, |I_{D,M2}|\}} \quad (1)$$

The f_{dec} function indicates that a decoding of the result is taking place. Simulations on the transfer function of the system indicate that an approximately linear *Angle to digital output*-transfer function is indeed achievable with a appropriate choice of dimensions and placement of the bar magnet and the MAGFET's and magnetic material. The simulations were based on the 'finite element' analysis method using the ANSYS program [1].

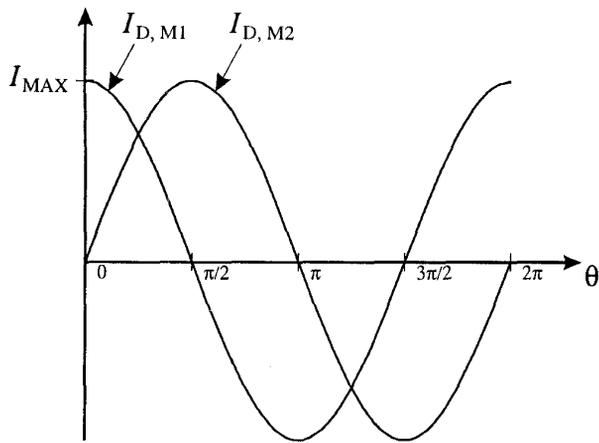


Figure 2: The MAGFET signal currents

II. THE MAGFET TRANSISTOR

A MAGFET is a MOSFET transistor with multiple drain terminals (typically 2 or 3 drains) [2] [3]. Due to the implementation (see Figure 3) of the MAGFET the differential drain current is dependent on the magnetic field applied to it.

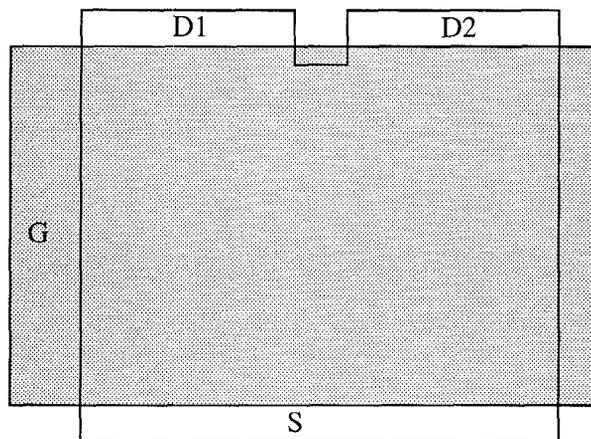


Figure 3: MAGFET Layout

The dimensions, the biasing and the topology of the MAGFET will influence important values such as sensitivity to magnetic field, linearity, noise, offset errors and the use of power and area. Measurements and calculations concerning MAGFET characteristics can be found in [4]. In this specific project the MAGFET has been implemented using four two-drain MAGFET's in cascade as shown in Figure 4. The dimensions of each MAGFET is $W/L = 62 \mu\text{m}/62 \mu\text{m}$ and a common centroid structure has been used for the layout for lowering offset errors. The resulting MAGFET was found to have an approxi-

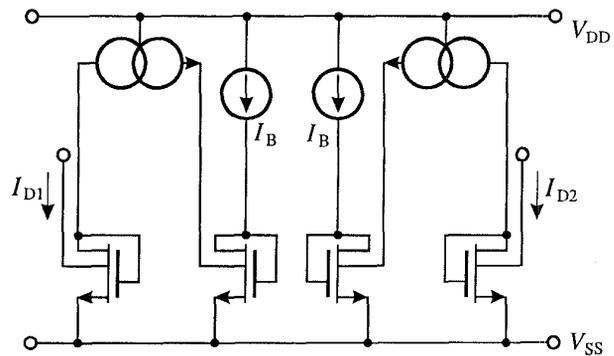


Figure 4: Cascade coupled MAGFET

mate transfer function given by Eq. (2).

$$I_{D1} - I_{D2} = 0.32 T^{-1} I_B B_{z, MAG}(\theta) + I_{OFF} \quad (2)$$

where $B_{z, MAG}(\theta)$ is the magnetic flux in the vertical direction at the MAGFET.

The bias current was set to $I_B = 15 \mu\text{A}$ giving a maximum differential signal current of $\pm 1.2 \mu\text{A}$. The cascade coupled MAGFET uses $120 \mu\text{A}$ and the offset current I_{OFF} is measured to be as high as 50% of the maximum output current. This is mainly due to variations on the threshold voltage V_T . This large offset current cannot be accepted. An offset compensation is necessary to bring it to an acceptable level. For this purpose an 8 bit A/D - D/A system will be used. The same A/D - D/A system is also used to convert the position of the magnet to a digital number.

III. THE A/D - D/A SYSTEM

The A/D - D/A system must be able to measure the offset error by an A/D conversion and make a permanent digital storage of the offset error. The stored offset error is then D/A converted and subtracted from the MAGFET current. The measuring and storing of the offset errors has to be done without any magnetic field applied to the MAGFET, i.e. before the bar magnet is placed on the top of the chip. The D/A conversion and the subtraction of the stored error from the MAGFET current must be carried out before any processing on the MAGFET currents can take place. It was decided to use the *successive approximation method* for A/D conversion because this conversion is based on a D/A converter (DAC). By using the same DAC in both the A/D and the D/A conversion undesired nonlinearities in the D/A transfer function will cancel out. This will be explained in more detail in the next section. Also it is an efficient solution in terms of minimizing area.

For this purpose a serial DAC, which generates the MSB first and the LSB last, has been developed. The advantage

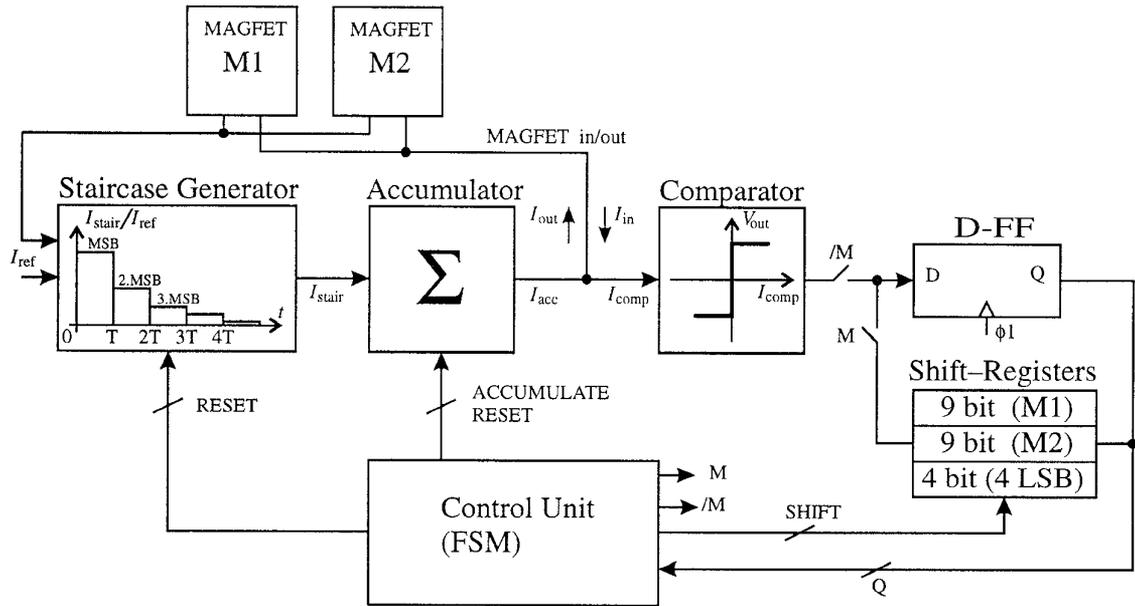


Figure 5: The AD/DA system

of this solution, compared to a traditional parallel DAC, is less use of area and no use of a *successive approximation register*. The D/A converter has been realized with the use of *switched current* (SI) technique and is described in detail in [4]. A block diagram of the entire system is shown in Figure 5. The system is controlled by a finite state machine realized with a PLA. It works in two different modes. In **Mode 1** the two offset currents are measured (A/D converted) and stored digitally. In **Mode 2** the stored error signals are D/A converted and subtracted from the MAGFET currents and the position of the bar magnet is determined from the two offset compensated MAGFET currents using the same A/D conversion system. The sequences are shown schematically below.

Mode 1 : Storage of offset errors (No magnetic field applied)

1. 8 bit A/D conversion of $I_{M1,OFF}$
2. Storage of $I_{M1,OFF}$
3. 8 bit A/D conversion of $I_{M2,OFF}$
4. Storage of $I_{M2,OFF}$

Mode 2 : Position detection (Magnetic field applied)

1. 8 bit D/A conversion of $I_{M1,OFF}$
 $I_{M1,SIGNAL} = I_{M1} - I_{M1,OFF}$
2. 8 bit D/A conversion of $I_{M2,OFF}$
 $I_{M2,SIGNAL} = I_{M2} - I_{M2,OFF}$

$$3. \left. \begin{array}{l} I_{M1,SIGNAL} > 0 ? \\ I_{M2,SIGNAL} > 0 ? \\ |I_{M1,SIGNAL}| > |I_{M2,SIGNAL}| ? \end{array} \right\} \Rightarrow 3 \text{ MSB}$$

$$4. 4 \text{ bit A/D conversion : } \frac{\min\{|I_{D,M1}|, |I_{D,M2}|\}}{\max\{|I_{D,M1}|, |I_{D,M2}|\}} \Rightarrow 4 \text{ LSB}$$

A/D conversion : The A/D conversion of **Mode 1** utilizes all of the building blocks of Figure 5. The staircase generator is generating a sequence of exponentially decaying current pulses, i.e MSB followed by 2.MSB etc. ending with LSB. When the output is MSB the output of the accumulator (MSB as well) is subtracted from the MAGFET current which is to be measured and the sign of the resulting current appears at the output of the comparator. This sign signal is both shifted into the shift register and passed to the control unit. Depending on the sign the control unit decides whether the accumulator should accumulate the output from the staircase generator (sign is positive) or not (sign is negative). The same scheme now is repeated for 2.MSB and so on, and the staircase outputs are only accumulated when the output of the comparator is positive. The digital number representing the offset error is now stored in the shift register and is ready for D/A conversion of **Mode 2**.

D/A conversion : In this mode the operation of the staircase generator and the accumulator is the same but the comparator is not used. Instead the digitally stored offset current is now shifted out from the shift register, into the control unit (FSM), to control the accumulation of the

current pulses from the staircase generator. The resulting output of the accumulator is subtracted from the uncompensated MAGFET current and stored in a current copier.

The compensating subtraction and inversion of current signals are carried out with the use of the basic building blocks of the switched current circuitry, the *current copiers* [5]. The current-copiers used in this system are designed as shown in Figure 6.

Because of the large current consumption of the MAGFET, a current copier is used to sample and hold the MAGFET current. The MAGFET now only has to be turned on for one clock cycle for measuring the MAGFET current. The operating clock frequency for the switched current system is 25 kHz. An angledetection has to be done at every 100 ms meaning that the *turn on* dutycycle for the MAGFET is less than 0.1%. The total process of **Mode 2** is carried out in 32 clock cycles making the *turn on* dutycycle for the entire circuit (including all digital operations) less than 2%.

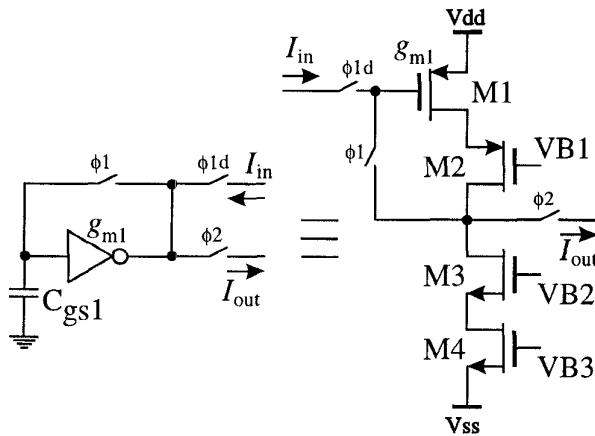


Figure 6: The current copier

IV. LIMITATIONS IN THE A/D AND D/A SYSTEM

The accuracy of the A/D - D/A system is set by the accuracy of the serial D/A conversion. The serial D/A converter is built from the staircase generator and the accumulator. Therefore the accuracy of the overall system is determined by the accuracy of the staircase generator and the accumulator. The staircase generator produces some exponentially decaying current pulses: $I_{\text{stair}} = I_{\text{ref}} \cdot (a, a^2, a^3, \dots)$, which are sent to the accumulator. Ideally we would like to have $a = 0.5$. The accumulator accumulates the current pulses arriving from the staircase generator, controlled by the FSM. Unfortunately, the accumulator is not ideal and will therefore lose some of its contents for every clock cycle. To predict the effect of this, we can model the accumulator as a linear

system having an impulse response sequence given by: $h_{\text{acc}} = (b, b^2, b^3, \dots)$. An ideal accumulator would have $b = 1$, but in our case we have b slightly less than one. The contents of the accumulator, while performing an A/D or D/A conversion, can now be treated as the convolution of the output sequence of the staircase generator with the impulse response sequence of the accumulator.

After n clock cycles the contents of the accumulator will therefore be given by:

$$I_{\text{acc}} = k \cdot I_{\text{ref}} \cdot (D1 + D2 \cdot c + \dots + Dn \cdot c^{n-1}) \quad (3)$$

In the ideal case we would like to have $c = 0.5$, because it would result in a linear conversion. But because of the errors in the staircase generator and in the accumulator this will not be the case. To see how variations in c will influence the linearity of the D/A converter we will make use of Figures 7 and 8. These two figures show the linearity of the D/A converter around changes in the MSB, where the errors are largest. The error when the MSB changes, i.e. a change from (0111...1) to (1000...0), is given by:

$$\delta = 1 - (c + c^2 + \dots + c^{n-1}) = 1 - c \frac{1 - c^{n-1}}{1 - c} \quad (4)$$

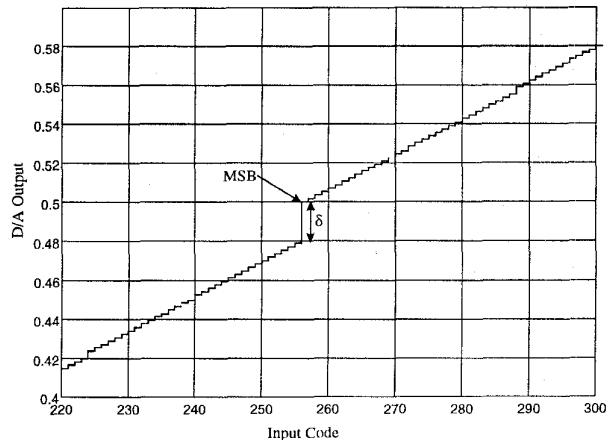


Figure 7: Linearity of D/A around MSB, with $c = 0.49$

First we will look at Figure 7 where we have $c < 0.5$. Let us now assume that we want to make an A/D conversion of a signal current which is slightly less than MSB. Because of the successive approximation algorithm the MSB will not be used and we will end up representing the signal by the sequence (MSB...LSB) = (0111...1). Therefore the error between the A/D converted and the D/A converted signal can be as large as δ . Let us now look at Figure 8 where we have $c > 0.5$. And let us again assume that we want to make an A/D conversion of a signal current

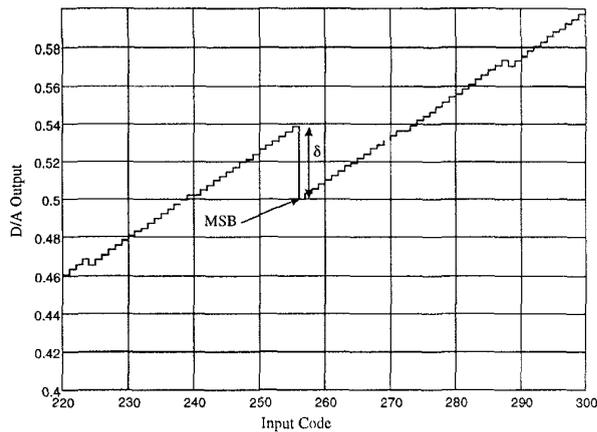


Figure 8: Linearity of D/A around MSB, with $c = 0.52$

which is somewhere inside the range of δ . Now, because of the successive approximation algorithm the MSB will be maintained and some of the less significant bits will be added to approximate the signal current. Therefore the maximum error between the A/D converted and the D/A converted signal will be only 1 LSB ($\approx c^n$). If we consider all the error sources in the staircase generator and in the accumulator the relative accuracy of c will be around 1% – 2%. If we want to represent the signal current by 9 bits and if we allow the error between the A/D and D/A converted signal current to be less than 2 LSB (this is equal to an accuracy of 8 bits) c should be in the range $0.499 < c < 0.545$. Because of this we chose $c = 0.52$ ensuring that it will always be possible to perform a fairly accurate conversion of the signal current even when c should be 2% less than expected i.e. $c = 0.51$. We have implemented the choice of $c = 0.52$, by letting the staircase generator generate current pulses with $a = 0.52$. The dynamic range for our A/D – D/A conversion system, defined as the largest signal current divided by the smallest signal current, is given by:

$$DR = \frac{I_{max}}{I_{min}} = \frac{1 + c^2 + \dots + c^{n-1}}{c^{n-1}} = \frac{1 - c^{-n}}{1 - c^{-1}} \quad (5)$$

In our case with $c = 0.52$ we get $DR = 388.6$ which equals 8.6 bit.

V. EXPERIMENTAL RESULTS

The circuit has been laid out in an industry standard $1.5\mu\text{m}$ CMOS process. The chip size is $2\text{ mm} \times 2\text{ mm}$ and the circuitry uses approximately 60% of this area. The reason for the chip size being this big is that it should fit to the bar magnet, which for practical reasons could not be made smaller. The dimensions of the bar magnet are $0.5\text{ mm} \times 0.65\text{ mm} \times 2\text{ mm}$ (HWL). The MAGFET will be exposed to a magnetic field in the range of $\pm 0.25\text{ T}$.

All the described operations of the A/D – D/A system and of the MAGFET's have been tested. Measurements show that the system can operate with supply voltage down to 2.3 V. The current consumption of the switched current A/D – D/A conversion system is $38.5\mu\text{A}$ and each MAGFET uses $120\mu\text{A}$. However, because of the small *turn on duty-cycle* the average current consumption is as low as $1.5\mu\text{A}$. The peak current, i.e. when the SI system and one of the MAGFET's are active at the same time is close to $160\mu\text{A}$. The system operates correctly with the clock frequency range of 5 Hz to 25 kHz.

VI. CONCLUSION

An angledetector with 7 bit digitally output has been described. It is meant as an alternative to the traditional slide potentiometer used as volume control in many hearing aids systems. Because of the absence of galvanic contact between the angle-setting device and the electric circuitry the component is expected to increase lifetime of the component significantly. The average current consumption of the component is approximately $1.5\mu\text{A}$. The peak current is approximately $160\mu\text{A}$. It works with supply voltage down to 2.3 V and operates with clock frequencies in the range of 5 Hz to 25 kHz.

ACKNOWLEDGMENT

The project has been carried out in cooperation with Microtronic A/S, Roskilde, Denmark. We would also like to thank Ole Hansen who introduced the idea of using magnets and MAGFET's for position detection.

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