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Le, Khanh Hoang; Nielsen, Søren Nørskov; Dittmann, Lars; Gliese, Ulrik Bo

*Published in:*  
Proceedings of the 48th IEEE Vehicular Technology Conference

*Link to article, DOI:*  
[10.1109/VETEC.1998.686555](https://doi.org/10.1109/VETEC.1998.686555)

*Publication date:*  
1998

*Document Version*  
Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

*Citation (APA):*  
Le, K. H., Nielsen, S. N., Dittmann, L., & Gliese, U. B. (1998). Base station MAC with APRMA protocol for broadband multimedia ATM in micro/pico-cellular mobile networks. In *Proceedings of the 48th IEEE Vehicular Technology Conference* (pp. 234-238). IEEE. <https://doi.org/10.1109/VETEC.1998.686555>

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# Base Station MAC with APRMA Protocol for Broadband Multimedia ATM in Micro/Pico-Cellular Mobile Networks

K. H. Le<sup>1</sup>, S. Nørskov<sup>2</sup>, L. Dittmann and U. Gliese

Center for Broadband Telecommunications, Department of Electromagnetic Systems,  
 Technical University of Denmark, Building 348, DK-2800 Lyngby, Denmark  
 Phone: +45 45 88 14 44, Fax: +45 45 93 16 34, E-mail: ug@emi.dtu.dk

**Abstract** — The concept for a wireless ATM access system that enables seamless mobile connectivity to the B-ISDN is presented. It is based on small, low cost and intelligent base stations running a medium access control (MAC) protocol using adaptive packet reservation multiple access (APRMA). Both the principles and the performance of this protocol are discussed. A channel efficiency of more than 70 % and a mean cell transfer delay of less than 17 cells are obtained in the range of 1-50 simultaneously connected users even with bursty traffic. For this, the cell dropping rate is kept below  $10^{-9}$  when the mobile terminals use buffer lengths of only 200-300 cells. The different components of this access system are currently under implementation and the MAC unit has been successfully implemented for a 32 Mbit/s wireless channel supporting 25 Mbit/s ATM introducing only 22 % of protocol overhead.

## I. Introduction

Integration of future broadband mobile communication networks into the B-ISDN seems highly desirable for both the user and the mobile tele-operator [1]. For the user, it ensures a seamless connectivity where the same services can be accessed from both fixed and mobile connections. For the operator, a greater flexibility and cost efficiency in mobile network planning, deployment and operation is gained as the B-ISDN can be used as a backbone for the mobile networks.

According to the ITU-T recommendations, asynchronous transfer mode (ATM) will be used for traffic transport and switching in the B-ISDN. Consequently, a full mobile/B-ISDN integration implies the use of ATM throughout mobile networks. This requires development of wireless ATM access systems and appropriate radio access protocols. At present, there is significant focus on the realization of wireless ATM, and a number of different concepts have been suggested and experiments performed. Overviews are given in [2], [3].

In this paper, we present a new broadband wireless ATM access system that enables full adoption of ATM in the mobile networks. This system facilitates the integration with the B-ISDN. The concept and protocol layers are shown in Fig. 1. The network is divided into a fixed network segment and a wireless access segment. It is the purpose of the wireless ATM access system to handle the wireless access segment as well as

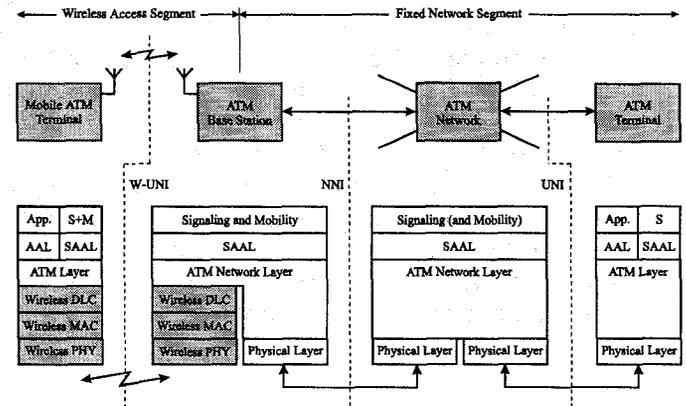


Figure 1: Concept and protocol layers for an ATM/B-ISDN network with full integration of wired and wireless access.

the seamless interfacing to the fixed network segment without alteration of the ATM related layers.

The small and low cost base stations (BSs) are designed to operate as intelligent self-contained ATM network units that connect directly to the B-ISDN or to any local mobile ATM network. This gives a high network planning flexibility and an efficient utilization of the B-ISDN for the mobile network infrastructure. The wireless access from the mobile terminals (MTs) is controlled by a medium access control (MAC) protocol using the recently proposed Adaptive Packet Reservation Multiple Access (APRMA) method [4], [5].

Connection of an MT is performed over the wireless user-network interface (W-UNI) where the physical (PHY) layer handles the radio transmission, the MAC layer handles the wireless access, and the data link control (DLC) layer handles the link reliability. As the BS acts as an ATM unit, it can be directly connected at any ATM network-network interface (NNI). Based on this configuration the mobile user cannot distinguish the wireless connection from a fixed connection, and all applications and signaling run over the ATM adaptation layer (AAL) and signaling AAL (SAAL), respectively. It is envisioned that the user mobility management is handled locally by the BS and MT and on a larger scale by MSCs connected to the fixed network segment.

<sup>1</sup> K.H. Le is now with NEC C&C Research Laboratories, Princeton, USA

<sup>2</sup> S. Nørskov is now with Nokia Mobile Phones R&D, Copenhagen, Denmark

## II. Base Station Architecture

The architecture for the BS is shown in Fig. 2. As seen, the BS consists of a transceiver, a base station controller (BSC) and a CPU supported by appropriate software. The transceiver takes care of the wireless transmission, carrier synchronization, modulation/demodulation and bit timing (wireless PHY layer). The MAC and DLC unit handles all aspects of the radio channel access (MAC layer) and link reliability (DLC layer). An ATM switch element is added for routing of the ATM-cells. Control and management cells for the BS are routed via an ATM segmentation and reassembly (SAR) unit to the CPU. All other cells are routed to the network interface (uplink) or to the MAC and DLC unit (downlink). An ATM line driver provides the connection to the ATM network (PHY layer). The ATM SAR unit performs the ATM layer, ALL, and SAAL functions where the ATM-cell payloads are unpacked before they are sent to the CPU via the PCI bus. The CPU and associated software perform monitoring and control of the BS, some traffic and quality of service control, and some signaling and mobility management (higher layers). The use of a PCI bus enables fast processing and easy connection of the BS modules to a PC for testing and software download.

All functions on the PHY, MAC, DLC, ATM, AAL, and SAAL layers are implemented in hardware in both the BS and the MT. This permits fast processing of the radio packets and ATM-cells.

## III. Principles of APRMA

Dynamic medium access control is necessary in order to provide efficient support of multimedia ATM traffic over the radio channel. In the following, the principles of the APRMA method are presented. As opposed to many other access methods, APRMA is developed with main focus on a highly efficient channel utilization for wireless transmission of multimedia ATM traffic. The fundamentals of APRMA are based on PRMA [6], and its characteristic features are:

1. Packet transmission; the ATM-cell is adopted as the basic unit of the radio packet.
2. Channel access by contention; the contention mechanism is based on a permission probability  $p$ .
3. Adaptive slot reservation; reservations are obtained dynamically according to the current need of bandwidth.
4. Adaptive contention control; the contention process is controlled by varying the  $p$ -parameter in relation to the number of connections.

In APRMA, an adaptive algorithm is used to provide full support of multimedia traffic with both very different and variable bit rates. According to the traffic variations, the algorithm dynamically adjusts the assigned capacity to each connection. Connections with traffic bursts are therefore only assigned capacity during bursts. Consequently, APRMA is a very flexible access method, where generally all traffic types are supported, and the adaptive capacity assignment enables an effective channel utilization.

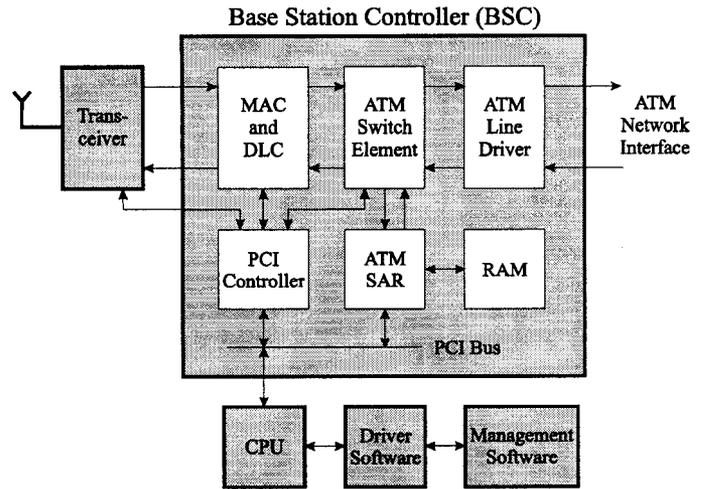


Figure 2: Architecture for the ATM base station

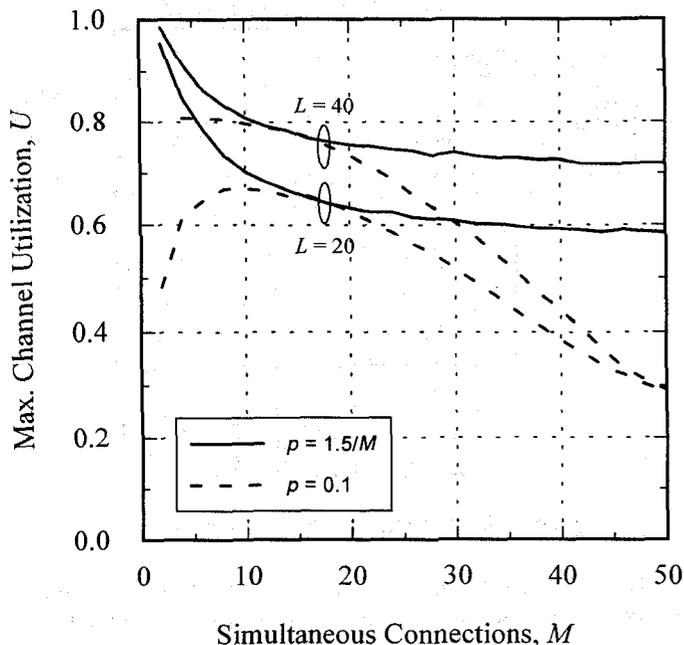
The APRMA channel is basically a time division multiplexed channel, where a frame structure with  $N$  identical time slots is used. Each time slot is used to transfer one packet containing one ATM-cell and the required protocol overhead. The two channels for uplink and downlink transmission may be either frequency division duplexed (FDD) or time division duplexed (TDD). In this paper, we assume the use of FDD.

Basically, each uplink time slot is either *reserved* to a specific connection or *available* for contention. Slot reservation is controlled by the BS, and the status of each uplink slot is transmitted to the MTs via the downlink traffic as embedded acknowledgments. Slot reservations are gained through contention of available time slots in the uplink frame. Before transmission from an MT, the ATM-cells are temporally stored in its output buffer. Each MT contends for reservation of available slots in the frame according to its number of stored cells. An MU is only allowed to contend when the following 3 conditions are fulfilled:

1. The slot must be available for contention.
2. The MU must have more stored ATM-cells than reserved slots.
3. The permission number, that is randomly generated between 0 and 1 by the MU, must be less than the value of the permission probability,  $p$ .

The second condition permits the MT to increase its bandwidth automatically. Whereas, the last condition reduces the probability of collision with requests from other MTs, and it prevents the deadlock situation when two or more MTs continue to request all available slots.

Reservation of a slot is granted by the BS, if a packet from one MT is received without collision with requests from other MTs. The reservation of specific slots are only maintained in subsequent frames as long as the MT continues to transmit packets in the slots. Otherwise, the unused slots are released by the BS.



**Figure 3:** Channel utilization versus the number of simultaneous connected mobile terminals. The buffer length,  $L$ , and the permission probability,  $p$ , are used as parameters.

#### IV. Performance of APRMA

In detail, the performance depends on a large number of factors. It is influenced by the number of simultaneous connected MTs,  $M$ , their traffic type (load and burst length), the acceptable cell dropping rate (CDR) and cell transfer delay, the number of slots per frame,  $N$ , the MT's buffer length,  $L$ , and the permission probability,  $p$ . In the following, the channel utilization,  $U$ , and the cell transfer delay are evaluated in relation to  $M$ ,  $L$ , and  $p$  for a frame of 20 slots.

Simulation results for the channel utilization as a function of the number of simultaneous connected MTs are shown in Fig. 3. The simulations are performed for random variable bit rate (VBR) traffic allowing a maximum CDR of  $10^{-3}$  due to buffer overflow. The MT buffer length,  $L$ , and the permission probability,  $p$ , are used as parameters to investigate their influence. The throughput per mobile unit is equal and given as the channel utilization divided by the number of simultaneous connected MTs,  $U/M$ .

It is seen that, even with a very short buffer of  $L = 20$  and a fixed permission probability of  $p = 0.1$ , a channel utilization of over 55 % is obtained in the range of 5-25 connected MTs. For less than 5 connected MTs, the utilization decreases because the MTs are not allowed to contend often enough due to the low  $p$ -value. It is also seen that, the utilization is decreasing for an increasing number of simultaneous connected MTs. This is because the  $p$ -value is now getting too high resulting in an increasing amount of contention collisions. This means that the MT load must be decreased to maintain the CDR of  $10^{-3}$ . Naturally, the situation can be improved by increasing the buffer length. As seen, for a buffer length of  $L = 40$ , the utilization is more than 60 % in the range of 1-30 connected MTs. This is a high channel utilization for random VBR traffic.

**Table 1:** Performance parameters for different traffic types at a channel utilization of 70 % and a  $p$ -value of  $1.5/M$ .

Traffic Type	Delay		CDR	Buffer Length
	$M = 5$	$M = 50$		
Random VBR	3	6	$10^{-3}$	30
			$10^{-6}$	65
			$10^{-9}$	95
Bursty VBR $B = 5$	11	6	$10^{-3}$	60
			$10^{-6}$	115
			$10^{-9}$	180
Bursty VBR $B = 10$	17	6	$10^{-3}$	90
			$10^{-6}$	190
			$10^{-9}$	280

From the above described problems with too low and high  $p$ -values it can be envisioned that an optimum  $p$ -value exists for a given number of simultaneous connected MTs. This has been confirmed by simulations. Therefore, the channel utilization can be even further improved by adaptively adjusting the permission probability. From detailed investigations, it is found that, by varying  $p$  according to the simple relation of  $p = 1.5/M$ , a very high utilization can be obtained. As seen in Fig. 3, a utilization of more than 70 % is obtained in the entire range of 1-50 connected MTs for a buffer length,  $L$ , of only 40 cells.

Delay simulations are performed for a total channel load of 70 %, which gives a mean channel load per MT of  $70/M$ %. Furthermore, the mean delay is normalized to the load per MT to evaluate the delay in relation to the MTs source rate. The normalized mean delay is expressed as

$$\bar{D}_{\text{Norm}} = \frac{l_{\text{Ch}}}{M} \bar{D}_{\text{Ch}}, \quad (1)$$

where  $l_{\text{Ch}}$  is the total channel load and  $\bar{D}_{\text{Ch}}$  is the mean delay in relation to the channel rate.

An overview of resulting delay and required buffer lengths for different types of traffic and different required CDRs is given in table 1. The delay and the required buffer length to maintain a maximum CDR of  $10^{-3}$ ,  $10^{-6}$  and  $10^{-9}$  are given for three different traffic types: random VBR, bursty VBR with an average burst length of  $B = 5$  cells, and bursty VBR with  $B = 10$  cells. The buffer length results are obtained for  $M = 20$ .

It is seen that the buffer length must be increased to accommodate both higher traffic burst and lower CDRs. This can be related directly to the delay increase at lower number of simultaneous connections ( $M = 5$ ). Whereas, the delay is constant at high  $M$  ( $M = 50$ ), even for increasing burst lengths. This is due to a more efficient statistical multiplexing at the higher number of simultaneous connections where the load per MT is relatively small. As seen, the delay and required buffer lengths are very low even for very bursty VBR traffic and low CDRs. This clearly demonstrates that APRMA is highly efficient for multimedia wireless ATM.

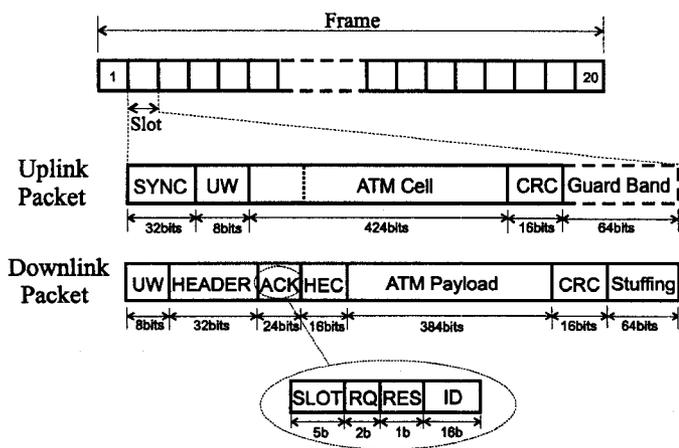


Figure 4: Uplink/downlink frame and packet formats.

### V. MAC and DLC Protocol Description

The APRMA frame and packet formats are shown in Fig. 4. In defining the number of slots per frame, many different aspects of the system must be taken into account, such as channel load, cell transfer delay, source bit-rate and traffic type. Therefore, a detailed investigation of the frame length has been performed. Based on this, it has been chosen to divide the frame into 20 slots. This gives a good channel utilization with a low delay for a wide range of user profiles as also evident from Fig. 3 and table 1.

At uplink, the basic element of the packet is the ATM-cell. The SYNC field provides a bit sequence permitting the receiver of the BS to establish carrier and bit timing synchronization. To mark the start of the ATM-cell, a unique word (UW) is inserted. This UW is used together with the ATM-cell header error control (HEC) field to provide a reliable packet detection. A cyclic redundant code (CRC) is added to detect bit errors within the payload. If errors are detected then a retransmission request scheme is initiated and the errored ATM-cell is retransmitted from the MT. Finally, the guard band absorbs the fluctuations in packet arrival time that arise due to the varying propagation delay of the radio signals.

At downlink, no bits are required for carrier and bit-timing recovery as all downstream bits are transmitted continuously. The format of the ATM-cell is slightly altered with the insertion of acknowledgment bits and the extension of the HEC field from 8-bit to 16-bit. This causes no complications as the ATM-cell can easily be reshaped after reception at the MTs.

The ACK field contains important acknowledgments and slot reservation status information for the uplink access. The downlink slots are numbered using the SLOT field. This feature will permit the MTs to update information at slot level. The RQ, RES and ID fields contain request for retransmission, slot reservation status and user identification data respectively. Certain bits of the received ATM-cell VPI and VCI are extracted and inserted into the ID field as an acknowledgment of reception and identification of the MT that has accessed the time slot. The MTs use the RES field to determine if a slot is free for contention and a combination of RES and ID fields to determine if a contention is successful and a reservation has been obtained. The feedback information is important for a

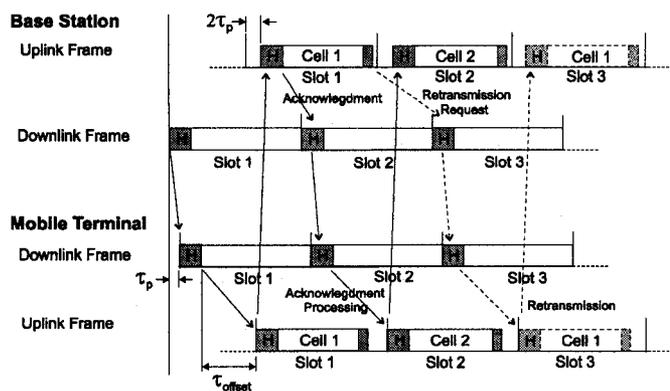


Figure 5: Uplink and downlink synchronization.

stable operation of the APRMA protocol. It is therefore protected through the expanded HEC field. Finally, to maintain the symmetry between up- and downlink frames, stuffing bits are inserted after the CRC.

In the following, the synchronization mechanism between up- and downlink frames is presented. As shown in Fig. 5, the uplink frame is synchronized to the downlink frame with a fixed delay,  $\tau_{offset}$ , which is the time from a downlink packet header is detected until an uplink packet is transmitted. The MT synchronizes with the BS via the downlink frame. The downlink packet stream is continuous, where idle packets are inserted if no traffic packets are ready to be transmitted by from the BS. It is assumed that the MT has previously updated all uplink slots reservation status before initiating a transmission. This is performed by continuously monitoring the feedback information contained in the ACK fields of the downlink packets. After transmission from the BS, the downlink slot reaches the MT after a variable propagation delay,  $\tau_p$ . If the MT has packets to transmit then it will do so according to the APRMA algorithm. The uplink packet experiences another delay of  $\tau_p$ , before detection at the BS. Acknowledgments for ATM-cell reception and slot reservation are then generated and inserted into the ACK field of the packet sent in the next downlink slot. The acknowledgments are processed at the MT where the slot reservation status is updated and the next ATM-cell in the buffer can be transmitted.

As described briefly in Section I, the DLC layer ensures that packets with bit-errors in the payload are retransmitted. In our system, the DLC protocol runs an automatic retransmission request (ARQ) scheme based on selective repeat which is initiated upon the detection of bit-errors. This is illustrated in Fig. 5, where the uplink packet in Slot 1 is assumed to contain bit-errors. The ATM-cell with payload errors (Cell 1) is discarded at the BS and a retransmission request is inserted into the RQ field of downlink packet in Slot 3, along with the acknowledgments for the uplink packet of Slot 2. The MT will then receive the RQ and reschedule the uplink packets such that the packet with errors is retransmitted in the next reserved slot or as a slot contention. Notice that the acknowledgments for ATM-cell detection and slot reservation at uplink Slot (i) are fed back at the downlink Slot (i+1), whereas the retransmission request is fed back at downlink Slot (i+2). In the worst

case situation which is depicted in Fig. 11, the cell sequence will be out-of-order if the MT transmits the next ATM-cell in its buffer before the reception of the retransmission request. Therefore, the DLC protocol must include a re-sequencing scheme which is performed at the BS. Several other ARQ and re-sequencing techniques are currently under consideration.

## VI. BS-MAC Architecture and Implementation

A first version of the MAC unit for the BS of Fig. 2 has been designed and implemented. The full DLC layer functionality has not yet been incorporated into the. As shown in Fig. 6, the BS-MAC consists of three main modules denoted as UPLINK, APRMA Algorithm and DOWNLINK.

In the UPLINK module, upon detection of the UW, a HEC check is performed to test the validity of the presumed ATM-cell. If the outcome is positive then the "cell\_detect" signal is asserted and the first four bytes of the ATM-header are extracted and sent to the APRMA Algorithm module. The ATM-header is processed in the APRMA Algorithm module while the payload is tested for errors in the UPLINK module. This scheme permits a faster processing of acknowledgments. If errors have been detected within the payload then the "crc\_not\_ok" signal is asserted and the cell is discarded. Otherwise, the "crc\_ok" signal is asserted and the ATM-cell is transferred from the UPLINK first-in first-out (FIFO) memory to the FIFO at the UTOPIA interface. The ATM-cell is then ready for transfer to the ATM switch element of the BS.

The downlink frame is generated in the DOWNLINK module. The "new\_slot" signal is asserted at the start of each downlink slot for synchronization of up- and downlink frames. Acknowledgments, generated by the APRMA Algorithm module, are inserted into the ACK field of each downlink packet. HEC and CRC values are calculated and inserted into the appropriate fields as well. If no ATM-cells are present at the DOWNLINK FIFO for transmission then idle cells are generated instead.

In the APRMA Algorithm module, an algorithm is implemented to provide the appropriate acknowledgments, according to the uplink slot access situation.

For test and monitoring purposes, a PCI CTRL is used to provide the interface to the PCI bus. For each generated acknowledgment, a message is transmitted to the CPU (here a PC) specifying the slot number, type of acknowledgment and information about the user that had accessed the slot. This gives the opportunity to continuously monitor the outcome of the uplink slot access.

The MAC unit has been implemented and successfully tested for a 32 Mbit/s channel rate supporting a 25 Mbit/s ATM rate. This has been done using four field programmable gate arrays (FPGAs). The use of FPGAs enables fast prototyping and easy testing and modification of the protocol before a final version is put into VLSI implementation.

## VII. Conclusion

The concept for a wireless ATM access system and its components that enables seamless mobile connectivity to the B-ISDN/ATM network have been presented.

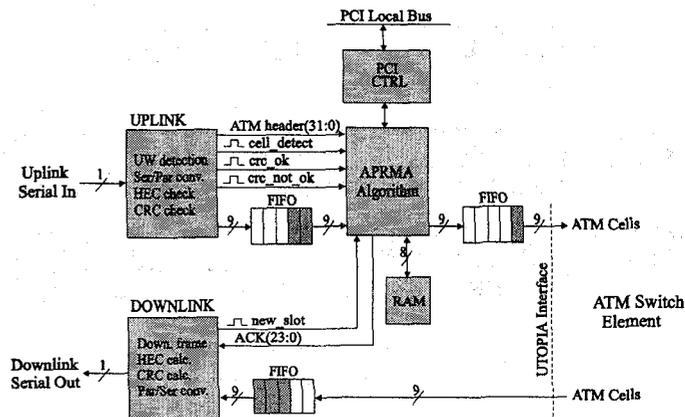


Figure 6: Block diagram of the BS-MAC.

For this, an efficient access method termed adaptive packet reservation multiple access (APRMA) has been developed. It has been shown that APRMA with adaptive control of the contention process gives a channel utilization as high as 70% in the range of 1-50 simultaneous connected MTs. This high utilization can be maintained with a maximum CDR of  $10^{-9}$  for both random and bursty VBR traffic using MT buffer lengths of only 200-300 cells. Furthermore, the mean cell transfer delay in relation to the MT source rate is less than 17 cells even for traffic with burst lengths of up to 10 cells.

A MAC protocol using APRMA and introducing only 22% of overhead has been developed. Initial development of a DLC protocol has also been performed.

The MAC unit for the BS has been designed and implemented for a 32 Mbit/s wireless channel supporting 25 Mbit/s ATM. All functionalities have been successfully tested.

At present, the MAC unit for the MT is under development. This will allow a real time access and transmission test. Further, several techniques for retransmission and resequencing for the DLC protocol are under investigations as are methods for QoS control.

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