High Efficiency Power Converter for Low Voltage High Power Applications

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Preface

This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree at the Technical University of Denmark, DTU Elektro, Electronics Group. The work was carried out during the period from September 2006 until January 2010 and was supervised by Professor Michael A. E. Andersen at the Technical University of Denmark. This work was supported by the Danish Energy Association (Dansk Energi - Net) under the national Public Service Obligation Program, project number 338-032 entitled “Modular Power Electronic Converters in the Power Range 1 to 10 kW,”. The work is conducted as part of a joint research cooperation between the universities Aalborg University, Technical University of Denmark, and University of Southern Denmark and the industrial companies Grundfos A/S, Danfoss A/S, KK-electronic A/S, and IRD A/S.

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- My dear friend Ole Seiersen for all his good advices and encouragement.
- All of my colleagues for their help, support, and for giving me this opportunity.

Abstract

The topic of this thesis is the design of high efficiency power electronic dc-to-dc converters for high-power, low-input-voltage to high-output-voltage applications. These converters are increasingly required for emerging sustainable energy systems such as fuel cell, battery or photo voltaic based energy systems. Applications include systems for emergency power back-up (UPS), de-centralized combined heat and power systems, traction applications such as hybrid electrical vehicles, forklift trucks and special applications such as low emission power generation for truck and ship containers, and remote power generation for light towers, camper vans, boats, beacons, and buoys etc.

In chapter 2, a review of current state-of-the-art is presented. The best performing converters achieve moderately high peak efficiencies at high input voltage and medium power level. However, system dimensioning and cost are often determined by the performance at the system worst case operating point which is usually at minimum input voltage and maximum power. Except for the non-regulating V6 converters, all published solutions exhibit a very significant drop in conversion efficiency at minimum input voltage and maximum output power.

In chapter 3, a detailed analysis of dominant loss factors in high power converters for low voltage applications is presented. The analysis concludes that:

- Power transformers for low voltage high power, if properly designed, will have extremely low leakage inductance.
- If optimally designed, boost converters will be much more efficient than comparable buck type converters for high power low voltage applications.
- The use of voltage clamp circuits to protect primary switches in boost converters is no longer needed for device protection. On the other hand, they will dramatically increase power losses. Moreover, if a converter is properly designed, primary side voltage clamp circuits will not even work in low voltage high power converters.
- Very high conversion efficiency can be achieved. Peak efficiency of 98% and worst case minimum efficiency of 96.8% are demonstrated on a 1.5 kW converter.

In chapter 4, the ability to - and challenges involved in - scaling of power converters for low voltage applications in the power range of 1-10 kW are analyzed. The analysis concludes that power MOSFETs needs to be paralleled extensively to scale power level to 10 kW. Maintaining fast current switching and reliable current sharing is essential. Further, the high ac-current carrying loop on the converter primary side will become increasingly difficult to scale due to fundamental issues such as physical size of components and penetration depth in copper.

Finally in chapter 5, a new method for partial paralleling of multiple primary power stages in isolated boost converters is presented. Maximum benefit of scaling in terms of higher efficiency and lower cost is preserved by only paralleling primary switches and the critical high ac-current loop. Dynamic current sharing is inherently guaranteed between parallel power stages. The principle can be applied to all isolated boost type converters and, in principle, an unlimited number of power stages can be paralleled. Feasibility and operation of the new topology are demonstrated on a dual 3 kW and a quad 10 kW prototype converter. Measured peak efficiency is 98.2% and worst case minimum efficiency is between 96.5% and 96.9%.

Resumé

Emnet for denne Ph.d. afhandling er design af effektelektroniske dc-dc konvertere med meget høj virkningsgrad til anvendelser med høj udgangseffekt, lav indgangsspænding samt høj udgangsspænding. Disse konvertere anvendes i stigende grad indenfor vedvarende energisystemer baseret på brændselsceller, batterier eller solceller. Anvendelserne omfatter nødstrømsanlæg (UPS), decentrale mikro-kraftvarmeanlæg, transportsystemer så som elektriske hybridbiler, gaffeltrucks samt særlige anvendelser indenfor generering af elektrisk energi til kølecontainere på lastvogne og skibe samt forsyning af fjerntliggende fyrtårne, campingvogne, både, afmærkningsbøjer m.m.

I kapitel 2, gennemgås state-of-the-art på området. De bedste af de præsenterede konvertere opnår rimelige høje virkningsgrader ved høje indgangsspændinger og lavere effekter. Men da de fleste systemers størrelse og pris afhænger af virkningsgraden i det kritiske arbejdspunkt, bliver virkningsgraden ved minimal indgangsspænding og maksimal udgangseffekt afgørende for det samlede system. Bortset fra en ureguleret V6 konverter udviser alle offentliggjorte konvertere dog kraftigt faldende virkningsgrader ved lav indgangsspænding og høj udgangseffekt.

I kapitel 3, foretages en detaljeret analyse af de væsentligste tabsfaktorer i konvertere til høje effekter og lave indgangsspændinger. Analysen konkluderer at:

- Korrekt dimensionerede effekttransformatorer til lav indgangsspænding og høj effekt vil have særdeles lav spredningsinduktans.
- Hvis boost konvertere designes optimalt, vil disse kunne opnå langt højere virkningsgrad end tilsvarende buck konvertere.
- Anvendelsen af voltage clamp kredsløb til beskyttelse imod overspændinger på switch-kontakterne i boost konvertere vil øge tabene kraftigt. Voltage clamps er ikke længere nødvendige og virker i øvrigt ikke, hvis konverteren er korrekt designet.
- Det er muligt at opnå særdeles høj virkningsgrad. Virkningsgrader på op til 98% er demonstreret på en 1,5 kW konverter. Worst case virkningsgraden er 96,8%.

I kapitel 4, gennemgås mulighederne for at skalere udgangseffekten på konverteren i området fra 1-10 kW. Der skal parallelkobles et stort antal power MOSFETs for at opnå en udgangseffekt på 10 kW. Der er behov for pålidelig og robust parallelkobling, som ikke nedsætter switch tiderne. Endvidere viser analysen, at de høje vekselstrømme på primærsiden vil være svære at skalere p.g.a. komponenternes fysiske størrelse kombineret med indtrængningsdybden i kobber.

Endelig, præsenteres der i kapitel 5 en ny metode til delvis parallelkobling af flere effekttrin i isolerede boost konvertere. Ved at begrænse parallelkoblingen til de få kritiske områder med høj belastning opnås en kosteffektiv løsning med høj virkningsgrad. Løsningen sikrer automatisk strømdelingen mellem alle parallelkoblede effekttrin. Løsningen kan endvidere anvendes i alle typer boost konvertere og kan – i princippet – udvides til parallelkobling af et ubegrænset antal effekttrin. Det nye princip er demonstreret i 2 prototype konvertere; en dobbelt 3 kW konverter og en firdobbelt 10 kW konverter. Der er målt virkningsgrader op til 98,2%, og de laveste virkningsgrader ved lav indgangsspænding og højeste udgangseffekt ligger imellem 96,5% og 96,9%.

TABLE OF CONTENT

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Nomenclature

D	Switch duty cycle
D_L	Inductor duty cycle
f_S	Converter switching frequency
T	Converter period time, $T=1/f_S$
T_L	Inductor period time, $T_L=T/2$
T_1	Period time one
n	Transformer turns ratio, $n=N_S/N_P$
F_R	AC resistance factor, $F_R=R_{ac}/R_{dc}$
$F_{R,P}$	AC resistance factor of primary winding
$F_{R,S}$	AC resistance factor of secondary winding
$F_{R,T}$	AC resistance factor of complete transformer
h	Height of conductor
h_P	Height of P^{th} winding portion
h_Δ	Height of primary-secondary intersection
h_w	Total height of transformer winding
H	Magnetic field strength
B	Flux density
w	Stored energy in magnetic volume
δ	Penetration depth in material
φ	Conductor height in penetration depth at fundamental frequency, $\varphi = h/\delta$
p	Winding portion
m	Number of layers in winding portion
l_w	Mean turn length
b_w	Breadth of winding
M	Number of primary-secondary intersections
N	Number of winding turns
N_P	Number of primary turns
N_S	Number of secondary turns
μ_0	Permeability of free space
V_e	Magnetic volume
x	Distance from H-field zero crossing, $0 \le x \le h_P$
E_C	Stored energy in diode capacitance
κ	Primary switch loss factor
N_{sw}	Number of parallel power MOSFETs in switch
L_{LK}	Transformer leakage inductance
$L_{LK,P}$	Transformer leakage inductance referred to primary side
$L_{LK,S}$	Transformer leakage inductance referred to secondary side
L_{CS}	Common source inductance
L_X	Commutation inductance, $L_X = L_{SP} + L_{LK} + L_{SS}/n^2$
L_{SP}	Primary stray inductance
L_{SS}	Secondary stray inductance
L_S	Stray inductance of interconnection wiring
L_{loop}	Total parasitic circuit inductance of loop
η	Converter conversion efficiency
V_{in}	Converter input voltage
V_o	Converter output voltage
$V_{in,min}$	Converter minimum input voltage
$V_{(BR)DSS}$	Rated drain-source break down voltage

v_{LCS}	Induced voltage across common source inductance
v_{GS}	Instantaneous gate-source voltage
V_{GS}	Gate-source dc voltage
v_g	Gate driver output voltage
V_C	Voltage clamp level
V_{S4}	Switch drain-source voltage
V_D	Diode forward voltage drop
V_R	Diode reverse voltage
v_L	Loop voltage driving current change
$I_{S,rms}$	Switch rms current
I_{in}	DC input current
I_{L1}	Inductor L1 current
i_{DS}	Drain-source current
I_o	DC output current
i_{T1}	Transformer current
I_{S4}	Switch current
I_D	Diode current
$R_{DS(on)}$	Power MOSFET drain-source on-resistance
$R_{S(on)}$	Total primary switch on-resistance
$R_{in,min}$	Minimum converter dc input resistance
$P_{in,max}$	Maximum converter input power
$P_{DS,con}$	Power MOSFET conduction loss
P_{CL}	Total current commutation loss
$P_{CC\text{-}VL}$	Converter current commutation loss in voltage limited mode (mode 1)
$P_{CC\text{-}CL}$	Converter current commutation loss in current limited mode (mode 2)
$P_{D,con,}$	Diode conduction loss
$P_{D,SW}$	Diode switching loss (capacitive)
P_R	Total converter rectifier losses
$P_{R,con}$	Total converter rectifier conduction losses
$P_{R,SW}$	Total rectifier switching losses
$P_{FB,con}$	Total primary full-bridge conduction loss

1 Introduction

1.1 Scope

The scope of this report is to present the results obtained in the PhD project "Modular Power Electronic Converters with Galvanic Isolation in the Power Range 1 to 10 kW," performed by the author during the period from September 2006 through January 2010. Many of the scientific results obtained in the project have been published in the form of peer reviewed conference and journal papers and a patent application. The published papers form an integral part of this thesis and are included in appendix [A1]-[A7].

The objective of this report is to supplement the already published information in [A1]-[A7] by placing the published papers in the context of the overall project and thereby present a more coherent and complete overview of the work and results obtained.

Further, it is the hope that this thesis can serve as a small condensed "designer's theoretical handbook" on key fundamental issues related to the design and optimization of high power converters for low voltage applications.

1.2 Background and Motivation

The background and motivation for this work is the emerging need for high power converters to boost voltage levels from low voltage electrical power sources to higher voltages required by the load. Figure 1, presents the typical power architecture of these systems.

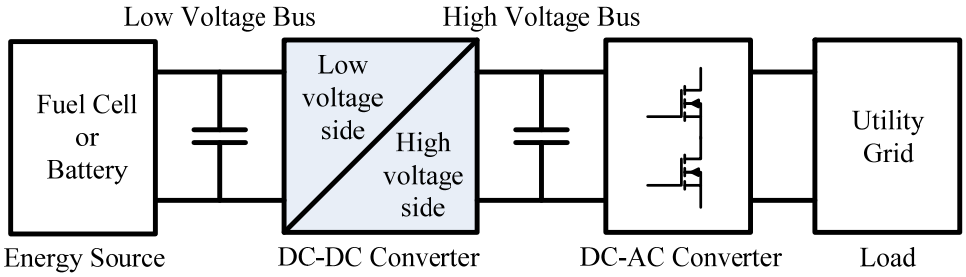

Fig. 1. Typical power system architecture for high-power low-voltage application.

An isolated dc-dc converter boosts the unregulated low voltage supply to a much higher dc voltage, typically 400 V for single phase and 7-800 V for three phase utility grid interface. Wide input voltage range, typically in the range of 30-60 V, is normally required.

Subsequently, a dc-ac inverter will typically convert high voltage dc output into single- or three phase ac voltage for interface to the utility grid or control of electrical motors etc.

Since the dc-ac converter operates at high voltage and is well known from other high power applications such as in UPSs, motor drives, solar inverters etc., the objective of this study is to focus on achieving high efficiency in the critical low voltage to high voltage dc-dc converter.

Typical systems include fuel cell systems, battery powered systems and even some photovoltaic systems. Applications include systems for emergency power back-up (UPS), de-centralized combined heat and power systems, traction applications such as hybrid electrical vehicles, forklift trucks and special applications such as low emission power generation for truck and ship containers and remote power generation for light towers, camper vans, boats, beacons, and buoys etc. [1]-[2].

Common to all of these applications is that cost of initial investment is high due to high cost of fuel cells, batteries or solar cells. Low conversion efficiency in the power electronic converter will significantly increase the required investment since more/larger cells will be needed.
High cost of fuel (hydrogen etc.) will further add to the total cost. Even size and cost of the electronic power converter itself may increase as a consequence of higher dissipated power and consequently increased thermal stress of components and system.

Achieving higher conversion efficiency in the power electronic converter required for boosting the low source voltage to the higher voltage required by the application, will therefore become a major competitive parameter in these applications.

In recent years, significant research effort has been devoted internationally to address the diminishing conversion efficiency which has been seen in high power low voltage applications [1]-[3].

A large number of alternative converter topologies and implementations have been proposed [4]-[5], [9]-[37] typically achieving high conversion efficiency at the medium to high input voltage range and at medium power levels. Best designs achieve peak efficiencies up to 96% [4], [9], [10], [15], [27], [28], [32]-[35]. At maximum output power and minimum input voltage, however, efficiency typically drops significantly to 90 % or below.

In fuel cell applications (and many others), peak power is reached at minimum input voltage, and available system peak power is directly affected by the decreased efficiency of the power converter. Thus, power source needs to be oversized in order to compensate for the reduced efficiency of the power converter. Furthermore, thermal design of the power converter itself needs to be dimensioned for this high peak power dissipation further increasing size and cost of the power electronic converter.

1.3 Project Objectives

The primary objective of this project is to study and demonstrate the absolutely maximum achievable conversion efficiency in high power converters for low-input-voltage to high-output-voltage applications.

In view of the requirements for fuel cell applications, the project focuses on solutions that provide galvanic isolation between input and output and are capable of operating over a wide input voltage range of typically a factor 2:1 [38].

Special consideration has to be given to achieving high conversion efficiency in the worst case operating point i.e. at maximum output power and minimum input voltage.

A second objective is to analyze and suggest the most efficient way - in terms of conversion efficiency and cost – to scale power level in the power range from 1 to 10 kW.

1.4 Common Specification

To ensure clear and ambitious goals for the research work, a list of high level converter requirements was formulated, see table I. The purpose of the list is to ensure that the project outcome will be adaptable to the relevant applications and thus constitute useful solutions.

A second purpose is to allow comparison of achieved results with a similar PhD study being conducted by Mr. Pawel Klimczak at the University of Aalborg on non-isolated converters for the same specification.

In order to avoid unnecessary limitation of creativity, the list of requirements only contain fundamentally needed high level requirements thus ensuring that solutions can realistically be applied to the applications foreseen [1]-[3], [38]-[41].

Thus, the primary focus is to achieve maximum conversion efficiency while still satisfying real life requirements to input voltage range, current and voltage control, and ripple currents. Such that presented results are realistic, and conclusions are valid for typical applications.

TABLE I.
CONVERTER SPECIFICATION

Parameter	Value	Comments
Output power P_{out}	1000 W	Maximum achievable power in single converter
Input voltage range V_{in}	30-50 V_{DC}	Start-up voltage up to 60V
Output voltage V_o	400 V_{DC}	Galvanic isolation required
Efficiency target η	98 %	Converter efficiency to be optimized at low input voltage.
Output power regulation	0-100 %	For full control of input current transients
Input current ripple >10kHz	<15 %	For load range 15-100%
Input current slew rate	<3 A/s	Slow dynamics of fuel cell

1.5 Project Plan and Content

A flow chart presenting the work packages carried out during this PhD project is shown in fig. 2. The flow chart also illustrates how the published papers, articles, and the patent application relate to key parts of the work carried out.

Following definition of project objectives including the target specification presented in table I, a state-of-the-art analysis is performed in order to establish current status on achievable conversion efficiency and proposed solutions.

In parallel with the detailed design of a 1.5 kW isolated boost converter [A1]-[A2], a detailed analysis of converter losses in high power converters for low voltage applications is carried out. The analysis confirms the choice of boost converter as the most efficient converter topology - but only because voltage rating of primary switches has been dramatically reduced by

eliminating primary side clamping circuits. To further verify the analysis, an isolated full-bridge buck converter is designed, built, tested, and compared with the 1.5 kW boost converter [A3].

Next phase is to analyze and suggest possibilities for increasing power level within the power range of 1-10 kW. Instead of immediately reverting to paralleling of complete converter modules - which will definitely be feasible - it is decided to identify those particular areas in the boost topology, where scaling of power is critical – and thus will benefit the most from paralleling. Apart from the obvious need to parallel power MOSFETs, it is found that the high ac-current loop from primary switches to the transformer primary windings is a particularly critical area with respect to scaling of power level.

A new method for partial paralleling of isolated boost converters is then proposed [A5]-[A7]. A patent application covering the new principle is filed [A7]. Two prototype converters are designed, built, and tested to demonstrate the feasibility of the new principle. The 3 kW dual version is published in [A5] and the quad 10 kW converter is published in [A6].

1.6 Thesis Structure and Content

The structure, organization and content of this PhD thesis is visualized in the flow chart presented in fig. 3.

The published journal paper, conference papers and the patent application [A1]-[A7] form an integral part of this PhD thesis and are therefore appended. As illustrated in fig. 2, the published papers cover a broad range of the work performed in this PhD study.

The purpose of this report is therefore to complement the already published papers by providing a condensed and coherent presentation of the overall project and its results. Special focus will be devoted to presenting a coherent derivation of the key fundamental theoretical aspects of this project.

Since most of the experimental results are already included in the published material [A1]-[A7], they are only included in a very restricted form in this thesis. And mostly where it serves the purpose of extending analysis of experimental results in order to verify or illustrate significance of the theoretical results.

Generally, the thesis is organized to reflect the general research approach adopted in the project i.e. definition of objective => state-of-the-art analysis => detailed design and analysis => demonstration of single converter => extension of power level => conclusion. The intension of this thesis organization is to present the project results in a condensed and straightforward manner.

PhD Project Overview

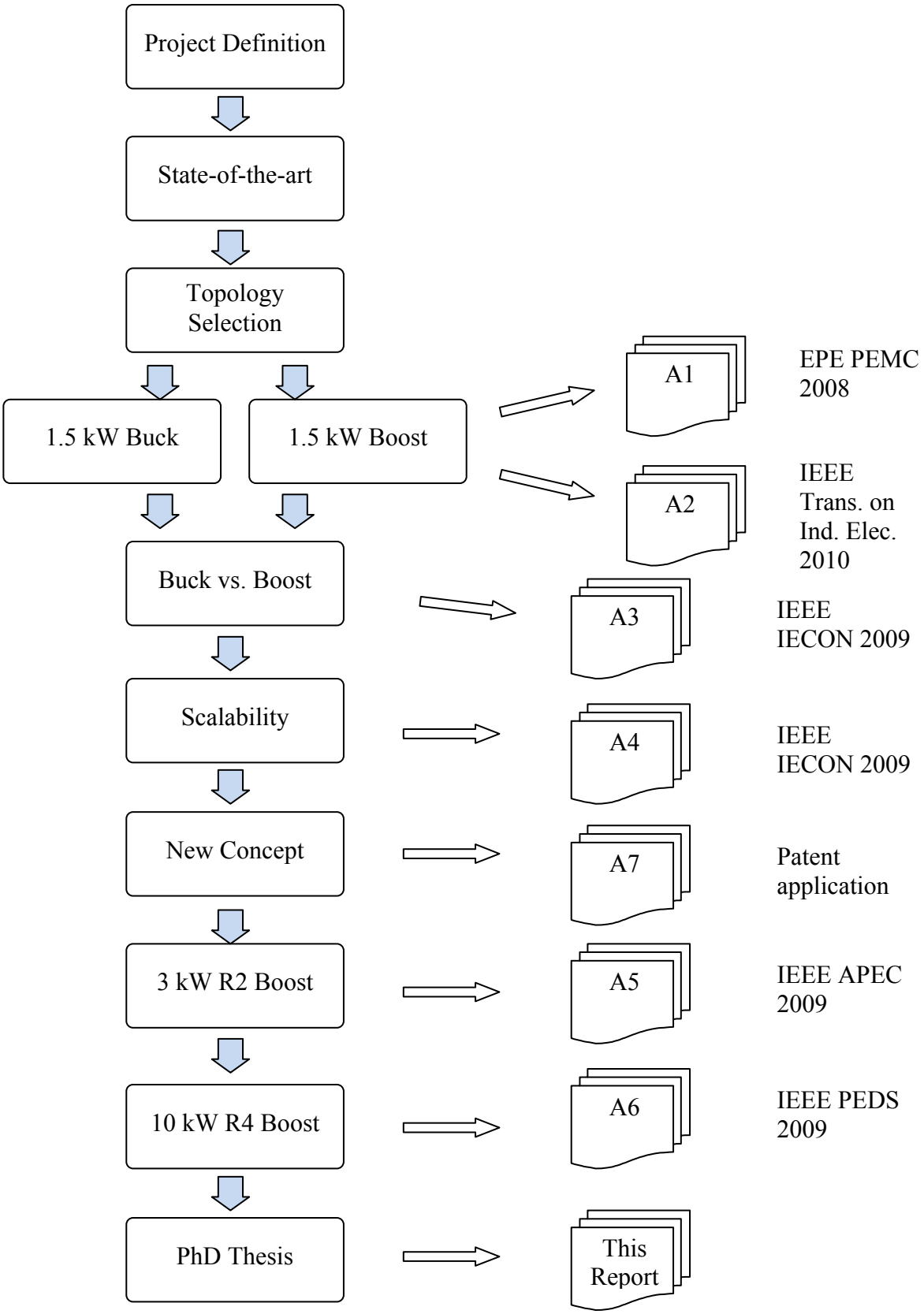

Fig. 2. PhD project work plan.

PhD Thesis Structure

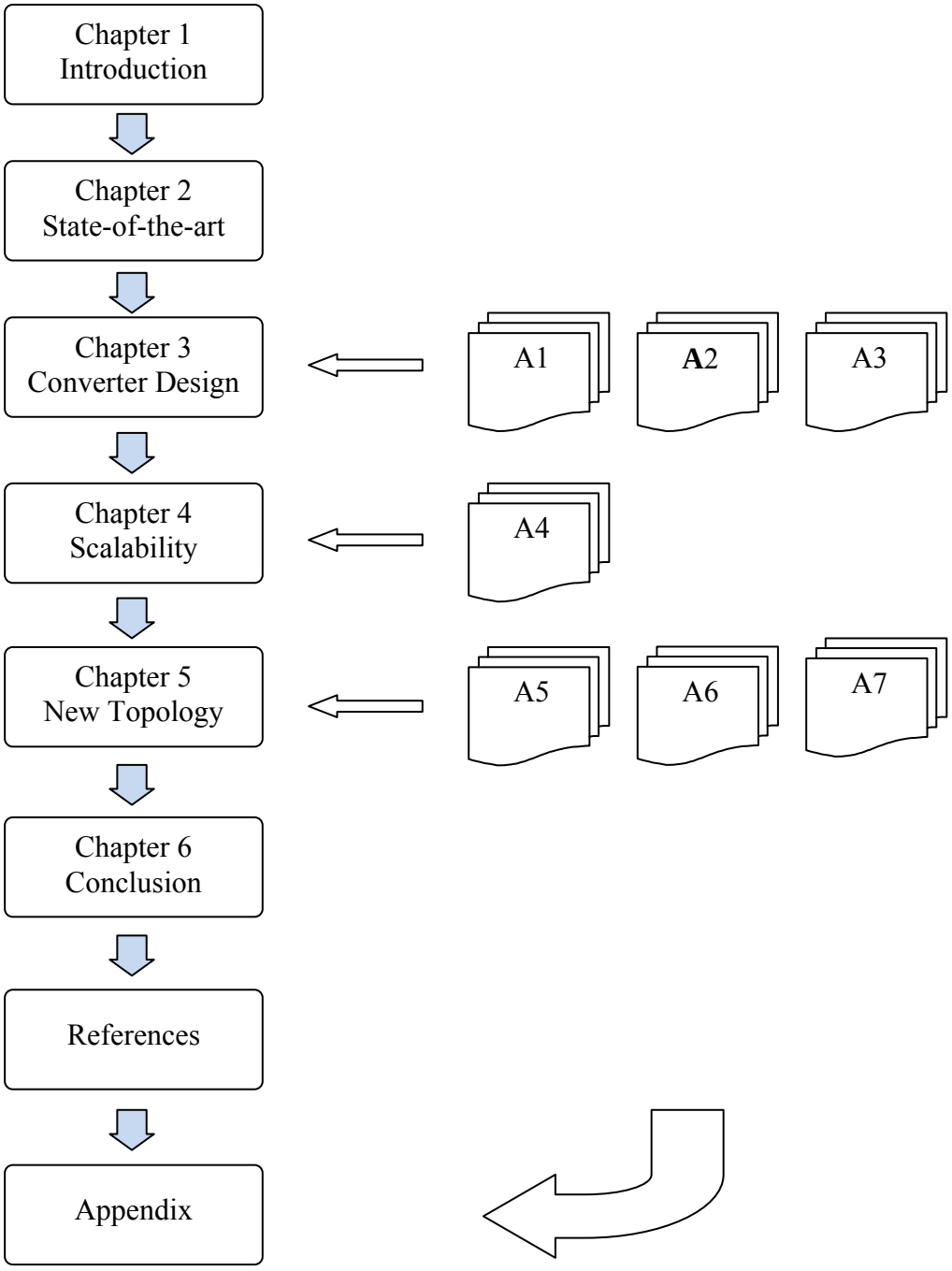

Fig. 3. PhD thesis structure.

2 State-of-the-Art

The purpose of this chapter is to present an overview of the present state-of-the-art within isolated dc-dc converters for low voltage high power applications. Recent published literature primarily in the form of journal papers, conference papers and tutorial notes, has been searched and analyzed to establish the present state-of- the-art. Main focus has been devoted to material presenting technical results, preferably supported by experimental results, useful for or relating to the overall specification defined for this project (table I).

In recent years, research on improving conversion efficiency in high power low voltage dc-dc converters for fuel cell applications, has attracted widespread international attention. Consequently, a significant amount of scientific literature has been published on the subject. Despite this fact, achieved efficiency results are often not published. Even when results are published, test conditions are often not reported. Further, measuring efficiencies in the high nineties are not trivial requiring strict attention to measurement tolerances and calibration of test set-up. Reliable efficiency results are thus scarce and generally very difficult to compare across alternative solutions.

Despite the general lack of reliable efficiency data, this chapter attempts to present an overview of published solutions, techniques and correspondingly achieved efficiencies for low voltage high power dc-dc converters.

For each published solution, a short description of the proposed solution is given together with a short summary of the published efficiency data. For a more in-depth presentation of the published material, the reader is referred to the full papers on the CD-ROM attached in the back of this thesis.

To best be able to compare efficiency data across the many different solutions, two sets of data have been selected. The maximum (or peak) efficiency achieved simply because it is often the only available data published i.e. the data that everyone wants to publish. However, much more useful data is the efficiency at minimum input voltage and maximum output power. Since this is most often the system-wise worst-case-point and therefore the driving parameter for overall system performance, size, and cost.

Papers published as part of this project are not included in the state-of-the-art analysis, they are attached in appendix A. However, they are included for reference in table II: “Comparative efficiency of low voltage high power converters.”

2.1 Isolated Boost Type Converters

This section lists selected published isolated boost type converter designs intended for high efficiency conversion of low input voltage high power to high output voltage. For each published design, a brief description of the topology used and the published efficiency results are provided.

Figure 4, presents a generic isolated boost converter including voltage clamp circuit across primary switches.

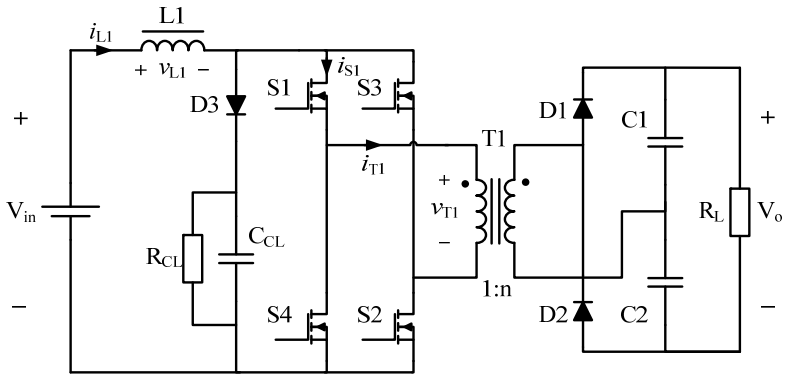

Fig. 4. Isolated full-bridge boost with voltage doubler and voltage clamp circuit.

2.1.1 Isolated Push-Pull Boost Converter

PP Boost 1:
A 1 kW fuel cell converter consisting of an isolated push-pull boost dc-dc converter followed by an H-bridge dc-ac converter is presented in [4]. The push-pull converter is hard switched and uses a common voltage clamp circuit across both primary switches.

Input voltage range is 25-45 V, and output voltage is 350-400 V. Maximum measured efficiency reaches 96.4% at 300 W output and 42 V input. At maximum output power and minimum input voltage (900 W at 25 V input) efficiency is 91%.

PP Boost 2:
A 1.5 kW fuel cell power converter consisting of an isolated resonant push-pull dc-dc converter followed by an H-bridge dc-ac converter is presented in [5]. A voltage doubler on output is used to tune converter current resonance such as to reduce output diode reverse recovery losses. Active clamp circuits are used across the two primary switches.

Input voltage range is 30-70 V and dc-dc converter output voltage is 350 V. System peak efficiency reaches 94% at 70 V input and 700 W output. Minimum efficiency is 92.5% at 1.5 kW output and 30 V input. No separate efficiency measurements for the dc-dc converter are provided.

2.1.2 Isolated Two-Inductor Boost Converter

The isolated two-inductor boost converter was first presented by P. J. Wolfs in 1993 [6]. The converter topology is the boost version of a HY-Bridge rectifier, also known as the current doubler, invented by O. S. Seiersen [7]-[8].

A large number of papers related to the high power low input voltage application of the two-inductor boost have been published, among these [9]-[15].

TI Boost 1:
A 500 W isolated two-inductor boost with active clamping is presented in [9]. An active clamp and reset circuit is used to clamp the allegedly severe voltage overshoot on primary switches due to the stored energy in the transformer leakage inductance. Primary switch currents are

triangular having large rms values. Input voltage range is not published, output voltage is 380 V. Peak efficiency is 96% measured at 300 W output and approximately 52 V input.

TI Boost 2:
A 1 kW modified isolated two-inductor boost with active clamping and reset is presented in [10]. Two transformers with individual rectifiers are effectively in parallel on input and in series on output. Due to the active clamping switch currents are triangular. Input voltage range is 26-50 V and output voltage is 400 V. Measured maximum efficiency is 95.6% at 600 W output power. Input voltage condition for the measured efficiency is not published.

TI Boost 3:
Two phase shifted two-inductor boost power stages are interleaved in [11]. Two voltage doubler rectifiers are in parallel on output sharing the same capacitors. By operating close to discontinuous conduction mode, current sharing between parallel power stages is achieved. A 200 W prototype converter verifies operation.

TI Boost 4:
A 1 kW two-inductor boost converter with active clamping is presented in [12]. Input voltage is 48 V and output voltage is 350 V. Peak efficiency of approximately 87% is reached at 500 W. At 1 kW output, efficiency has dropped to 77%. A comparable full-bridge boost converter is claimed to be 6-10% less efficient.

TI Boost 5
A 1 kW two-inductor boost stage is presented in [13] as part of a two-stage dc-dc converter for fuel cell applications. Input voltage is 80 V and output voltage is 400 V. At 750 W output power, efficiency is 67%.

TI Boost 6:
In [14], a 300 W two-inductor boost with soft turn-off snubbers is presented. Input voltage range is 18-32 V and output voltage is 48 V. Maximum efficiency is 92% at 28 V input and 300 W output power.

TI Boost 7:
A 1.5 kW bi-directional two-inductor boost intended for bi-directional interface between a 28 V and a 270 V aircraft power bus is presented in [15]. Active clamping and reset is used on low voltage side to clamp switch overvoltage. A phase-shift plus pulse-width modulation is used to create near square-wave low rms switch currents. Input voltage range is 22-32 V. Peak efficiency in boost mode is 96% at 32 V input and 750 W output. At 22 V input and 1.5 kW output, efficiency drops below 89%.

2.1.3 Isolated Full-Bridge Boost Converter

Isolated full-bridge boost converters have also been proposed extensively for high power low voltage applications, among these [16]-[27].

FB Boost 1:
A 5 kW isolated full-bridge boost converter is proposed for fuel cell electrical vehicles in [16]. Input voltage is 24 V and output voltage is 300 V. A passive voltage clamp circuit is used to limit voltage spikes across primary switches due to transformer leakage inductance. Peak efficiency at maximum output power is 94%. Very few design details or test results are given.

FB Boost 2:
A 1.2 kW interleaved isolated full-bridge boost converter is presented in [17]. Two separate isolated full-bridge boost converters with voltage doubler rectifiers are series connected on output and parallel connected on input. The series connected outputs guarantee average current sharing between converter stages, but at the expense of higher rectifier losses. Voltage clamp circuits across primary switches are used to clamp over voltages caused by transformer leakage inductance. Input voltage is 33 V and output voltage is 400 V. Maximum measured efficiency is 90.5% at 1.2 kW output.

FB Boost 3:
A 1 kW isolated full-bridge boost converter with zero current switching (ZCS), is presented in [18]. Large series resonant inductance and parallel capacitance form a slow resonant commutation during primary switch overlap time i.e. the storage inductor charging time. Zero current turn-on and zero current turn-off in primary switches are thereby obtained. Voltage- and load regulation is performed by wideband frequency modulation in order to achieve constant storage inductor charging time and thereby maintain zero current switching. Input voltage range is 22-27 V and output voltage is 1 kV. Peak efficiency is 92% at 1 kW output and 27 V input. At 22 V input and 1 kW output, efficiency is 88%.

FB Boost 4:
A 1.4 kW resonant isolated full-bridge boost converter is presented in [19]. Adding resonant capacitors across primary switches in addition to the series parallel resonant tank used in [18], a full resonant converter is obtained. Zero voltage and current turn-on and zero voltage turn-off are achieved. Regulation is performed by narrowband frequency control (250-370 kHz). Input voltage is 100 V and output voltage is 374 V. Maximum efficiency is below 90%.

FB Boost 5:
A 20 kW isolated full-bridge boost converter is analyzed in [20]-[22]. Input voltage range is 90-200 V and output voltage is 700 V. The converter is only tested up to 10 kW input power and no efficiency results are published. An active voltage clamp circuit designed to clamp 5-10% of converter output power is presented in [22]. At 9 kW input power, measured clamping energy is 505 W. Measured transformer stray inductance is 750 nH. Primary switches are rated for 600 V.

FB Boost 6:
Three bi-directional isolated full-bridge boost converters intended for electrical vehicles are presented in [23]-[25]. Specifications are quite similar, low voltage battery terminal is 8-15 V and output voltage is in the range of 250-450 V.

In [23]-[24] maximum boost mode power is 1.6 kW and maximum buck mode power is 5 kW. An active voltage clamp circuit as described in [26] is used to clamp primary switch over voltages caused by large transformer leakage inductance. Following a design rule of thumb in [24], voltage rating on primary switches is 55 V i.e. more than 3 times maximum input voltage.

In [25], boost power is up to 3 kW and maximum buck power is 2 kW. A soft commutation method to reduce voltage clamping energy is presented. By keeping secondary switches on, transformer secondary winding is shorted during current commutation right after primary switches have been turned off. The full clamp voltages are thus available for current commutation thereby reducing current switching time and consequently clamp energy.

Maximum efficiency in boost mode is approximately 94% at 10 V input and 1500 W output power. At 2.5 kW output and 8.5 V input, efficiency drops below 82%.

FB Boost 7:
A 500 W three phase isolated boost converter with active clamp circuit is presented in [27]. Three half-bridge primary switching legs operate in interleaved mode, each sequentially transferring the input current to output through three power transformers and a three phase rectifier. Due to the active clamp circuit, switch current is triangular having high rms value. Input voltage is 30-60 V and output voltage is 400 V. Maximum efficiency is 96% at 200 W output. Input voltage condition for the measured efficiency is not published.

2.2 Isolated Buck Type Converters

This section lists selected published isolated buck type converter designs intended for high efficiency conversion of low input voltage high power to high output voltage. For each published design, a brief description of the topology used and the published efficiency results are provided.

Figure 5, presents a generic isolated buck converter.

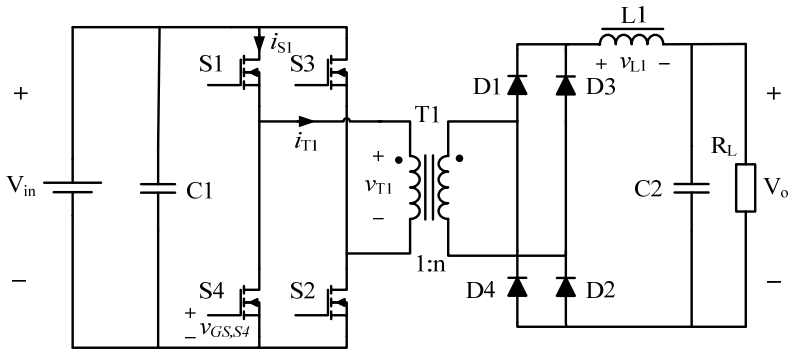

Fig. 5. Isolated full-bridge buck converter with full-bridge rectifier.

2.2.1 Isolated Full-Bridge Buck Converters

A number of isolated full-bridge buck converters for high power low voltage applications have been presented, among these [28]-[32].

FB Buck 1:
A 75 kW isolated full-bridge buck converter for fuel cell applications is presented in [28]. Input voltage range is 200-380 V and output voltage is 380 V. Measured efficiency is approximately 95%. No design details are published.

FB Buck 2:
A 5 kW isolated full-bridge buck converter is presented as part of a power system for fuel cell applications [29]. A single primary full-bridge inverter supplies two power transformers in parallel, each having separate full-bridge rectifiers and output filters. The two outputs are series connected in order to reduce rectifier voltage stress. Input voltage range is 22-41 V and output

voltage is 400 V. Measured efficiency of dc-dc converter is 90% at 4.4 kW output. Input voltage condition for the measured efficiency is not published.

FB Buck 3:
A system of multiple phase-shifted full-bridge buck converters is proposed in [30]. By introducing storage inductors between primary inverter phase legs of neighboring phase shifted power stages, conduction loss of primary switches is reduced. The design of a 500 W per bridge converter is analyzed. No test results are published. Simulated efficiency projects an efficiency of 95% for a 24-40 V input and 400 V output converter – when switching at 256 kHz.

FB Buck 4:
A 1.2 kW isolated full-bridge buck converter with a lossless output diode clamp circuit is presented in [31]. Using a new lossless output diode clamp circuit and phase shift control of primary switches, zero voltage and zero current switching of primary switches can be achieved. Input voltage range is 27-46 V and output voltage is approximately 200 V. Maximum measured efficiency is 94.2% at 32 V input and 700 W output power. At 28 V input and 1.2 kW output, efficiency is 92.5%.

FB Buck 5:
Finally, a 3 kW isolated full-bridge converter for fuel cell applications is proposed in [32]. The converter is unregulated operating at fixed 50% duty cycle. Adaptation to variable input voltage (due to fuel cell output voltage drop) is achieved by sequentially adding transformer secondary windings - by means of relay switching - to increase transformer turns ratio. Input voltage range is 44-96 V and output voltage is variable in the range 217-310 V. A maximum efficiency of approximately 96.5% is achieved at 60 V input and 1 kW output power. Efficiency drops to 94% at 45 V input and 2 kW output power.

2.2.2 Isolated Three Phase Full-Bridge Buck Converters

This section is mainly devoted to the much published three phase isolated buck converter also known as the V6 topology. Although it is basically an interleaved derivative of the phase shift controlled full-bridge buck converter, the number of publications related to this topology – and its apparently high performance – justifies the creation of a special section.

FB Buck V6:
The isolated three phase V6 converter presented in [33]-[37] consists of three phase-shift controlled full-bridge inverter stages which are interleaved by means of phase-shifting each inverter stage 120 degree apart. Each H-bridge inverter stage drives the primary winding of a single phase transformer. The secondary windings of the three power transformers are star-connected (Y-connected) and fed to a common 6-pulse three phase rectifier followed by a single storage inductor and output capacitor.

Since all three power stages are controlled by the same phase angle (however phase shifted 120 degree apart), a single common controller can control all three power stages. Current sharing between power stages is guaranteed by the common output inductor. Due to cancellation, input ripple current is significantly reduced and ripple frequency at input and output is tripled.

The star-connection of transformer secondary windings reduces transformer turns ratio by a factor of two. Input power is shared between three parallel power stages, reducing ac-current

levels in each power stage by a factor of 3 thereby reducing susceptibility to resistive and inductive losses (i^2R and Li^2) in interconnections.

Very high efficiencies have been reported for this topology. In [33]-[34], a 3 kW converter intended for fuel cell applications is presented. Input voltage range is 20-50 V and output voltage is 200 V. Measured efficiency seems to peak just below 97% at half output power. At maximum output power, efficiency is 96%. Measurement tolerances are however ±1% and input and output voltage conditions for the measured efficiency curve are not published.

Furthermore, the converter is tested in the efficiency sweet spot at a phase angle of 150 degree where the converter is operating as a dc-transformer without any possibility of control. At phase angles below 120° when converter is in regulation, rms-current in primary switches will be significantly higher than in comparable full-bridge buck converters. Published efficiency data for the V6 converter operated in regulated mode ($\alpha<120°$) has not been found.

2.3 Summary of State-of-the-Art Analysis

Twenty-two different converter designs intended for low voltage high power applications have been identified and analyzed. In table II, the published efficiency performance is listed for comparison.

Unfortunately, published efficiency results are generally rare and difficult to compare since important operating test conditions such as input voltage level, output voltage levels and measurement tolerances are often not published.

To perform the best possible comparison of the available data, both best case efficiency and the more important worst case efficiency data are compared.

For comparison, efficiency data from the three boost converters [A1]-[A2], [A5], and [A6], as well as the buck converter [A3], published as part of this PhD project is included in table II.

The system performance, cost, and size critical worst case efficiency column is highlighted in red. Best performance within each topology group is highlighted in light blue, and overall best performance is highlighted in blue.

In addition to the comparison of achieved efficiencies, a number of observations and conclusions can be drawn from the study of the published literature:

1. Many converter designs achieve modest to high efficiency at high input voltage and medium power. However, except for the V6 converters (though not in regulation) and the converters presented in this PhD project, all converters exhibit a very significant drop in efficiency in the critical low-input-voltage and maximum-output-power point.
2. High power transformers for low voltage applications have high leakage inductance [9], [20]-[22]. Further, power transformers with high turns ratio have high leakage inductance [24], [33], [35], [42]. Large transformer leakage inductance is generally considered a significant source of switching losses in boost type converters. None of the published papers have substantiated this claim or analyzed transformer ac-resistance and leakage inductance.

3. Primary switch voltage rating must be oversized by a factor of 2-3 in boost converters [10], [20]-[25] to allow headroom for the voltage clamp circuits to operate. Alternatively, active clamp- or reset circuits introduce additional switches and create triangular current waveforms thus increasing conduction losses.
4. Voltage clamp circuits are needed on boost converter primary switches [2], [4], [9], [10], [12], [14], [15], [20]-[27]. As a consequence of the allegedly large transformer leakage inductance, many forms of voltage clamping techniques and circuits are widely used to clamp voltage spikes across primary switches in boost type converters.
5. Soft switching is needed to achieve high conversion efficiency in low voltage applications [2], [3], [26], [27], [33], [35]. None of the published papers have presented any measured or analyzed data on switching losses.

The validity of these five key-design-assumptions will be analyzed in the next chapter.

TABLE II.
COMPARATIVE EFFICIENCY OF LOW VOLTAGE HIGH POWER CONVERTERS

Topology	No.	Power Level [W]	Input Voltage [V]	Output Voltage [V]	Best case Efficiency			Worst case Efficiency			Reference
					η	Vin	Pout	η	Vin	Pout	
Push-Pull Boost	1	1000	25-45	350-400	96.4	42	300	91	25	900	[4]
	2	1500	30-70	350	94	70	700	92.5	30	1500	[5][1]
Two-Inductor Boost	1	500	--60	380	96	52	300	-	-	-	[9]
	2	1000	26-50	400	95.6	-	600	-	-	-	[10]
	3	200	-	-	-	-	-	-	-	-	[11]
	4	1000	48	350	87	48	500	77	48	100	[12]
	5	1000	80	400	67	-	750	-	-	-	[13]
	6	300	18-32	48	92	28	300	-	-	-	[14]
	7	1500	22-32	270	96	32	750	<89	22	1500	[15]
Full-Bridge Boost	1	5000	24	300	94	24	4500	-	-	-	[16]
	2	1200	33	400	90.5	33	1200	-	-	-	[17]
	3	1000	22-27	1000	92	27	1000	88	22	1000	[18]
	4	1400	100	374	<90	100	1000	-	-	-	[19]
	5	10000	90-200	700	-	-	-	-	-	-	[20]-[22]
	6	3000	8-15	250-450	94	10	1500	<82	8	2500	[23]-[26]
	7	500	30-60	400	96	-	200				[27]
	8	1500	30-60	400	98	50	1200	96.8	30	1500	[A1]-[A2][2]
	9	3000	30-60	400	98	50	2900	96.9	30	2850	[A5][2]
	10	10000	30-60	7-800	98.2	50	9000	96.5	30	10000	[A6][2]
Full-Bridge Buck	1	75000	200-380	380	95	200	75000	-	-	-	[28]
	2	5000	22-41	400	90	-	4400	-	-	-	[29]
	3	500	24-40	400	-	-	-	-	-	-	[30]
	4	1200	27-46	200	94.2	32	700	92.5	28	1200	[31]
	5	3000	44-96	217-310	96.5	60	1000	94	45	2000	[32][3]
	6	1500	30-60	400	96.7	30	600	95.4	30	1500	[A3][2]
Full-Bridge V6	1	3000	20-50	200	<97	-	1500	96	-	3000	[33]-[35][3,4]

- No data available.
1 Efficiency data include dc-ac converter losses
2 Converter designs published in this project
3 Converter operated in unregulated dc-transformer mode
4 Input voltage and output voltage conditions are not published

3 Design of High-Power Low-Voltage Converters

In this chapter some fundamental issues related to design of high-power low-voltage converters are analyzed.

In the state-of-the-art analysis in chapter 2, a number of more or less generally accepted and widely adopted design approaches (myths) were identified:

1. High power transformers for low voltage applications and power transformers with high turns ratio have high leakage inductance.

2. Primary switch voltage rating must be oversized by a factor of 2-3 in boost converters.

3. Voltage clamp circuits are needed on boost converter primary switches.

4. Soft switching is needed to achieve high conversion efficiency in low voltage applications.

Following the analysis and presentation in this chapter, it becomes evident that all of these assumptions are wrong. Further, this chapter points out the special design issues that are particularly important in achieving high conversion efficiency in high-power low-voltage converters. These are:

a) Extensive interleaving of transformer windings is needed to reduce/avoid high conduction losses due to proximity effect.

b) Transformer leakage inductance does not depend on transformer turns ratio.

c) Transformer leakage inductance is proportional to number of turns squared.

d) The extensive interleaving required to reduce proximity effect in combination with the low number of primary turns will result in extremely low primary side transformer leakage inductances.

e) Voltage clamp circuits are effectively bypassed by the extremely low transformer leakage inductance rendering voltage clamps superfluous.

f) Current switching speed is critical in achieving high conversion efficiency.

g) Low stray inductance and low ac-resistance layout are very important in high-power low-voltage converters.

Finally, comparative analysis of buck and boost converters for low voltage high power applications shows that boost converters have fundamentally lower conduction losses in primary switches as well as lower reverse voltage stress on rectifier diodes. Thus, properly optimized boost converters will achieve higher conversion efficiency than comparable buck converters.

These findings are obviously very important in the process of selecting optimum converter topology and in the detailed design and optimization of high-power low-voltage converters.

3.1Low Impedance Level in High-Power Low-Voltage Converters

High-power low-input-voltage converters have extremely low primary side impedance levels.

Minimum converter steady state dc input resistance is given by

$$R_{in,min} = \frac{V_{in,min}^2}{P_{in,max}}. \quad (1)$$

The extremely low impedance levels seen on converter primary side essentially turn the converter circuit into a current switching circuit where resistive and inductive elements are far more important to losses than capacitive elements.

In order to process power efficiently at these low impedance levels, all circuit elements including primary switches, transformers and interconnection wiring have to exhibit comparatively low impedance levels. For a 1% power loss, any resistive series element has to be lower than 1% of the minimum input impedance.

All circuit impedances in a high efficiency circuit therefore have to scale according to the minimum circuit impedance level. From (1), it therefore becomes evident that it is extremely important to achieve low conduction impedances (resistances and inductances) in low-voltage high-power circuits.

3.2 Basic Operation of Isolated Full-Bridge Converters

As a reference for the analysis made in the following chapters, the basic operating principles of the isolated full-bridge boost and full-bridge buck converters are presented in the following sections.

3.2.1 Isolated Full-Bridge Boost Converter

A schematic of the isolated full-bridge boost converter is presented in fig. 6. Timing diagram with basic operating waveforms is presented in fig. 7.

Output rectifier configuration is a voltage doubler, effectively saving two rectifier diodes and reducing transformer turns ratio by a factor of two at the expense of larger output capacitors. The input capacitor, C_{in}, effectively removes the residual input ripple current i.e. the inductor ripple current, Δi_{L1}.

3.2.1.1 Basic isolated boost converter operation

Primary switches, S1-S4, are hard switched and operated in pairs, S1-S2 and S3-S4 respectively. Drive signals are 180 degree phase shifted. Switch transistor duty cycle, D, is above 50 percent to ensure switch overlap and thus a continuous current path for the inductor, L1, current.

Basic converter operation can be divided into four main states, T_1-T_4.

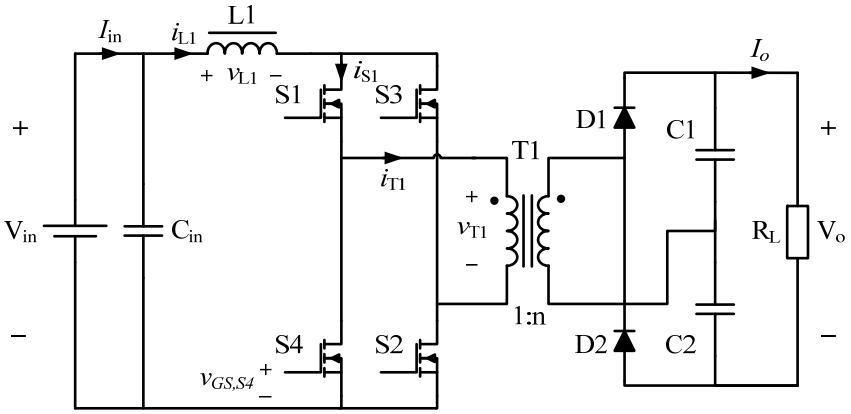

Fig. 6. Isolated full-bridge boost converter with voltage doubler.

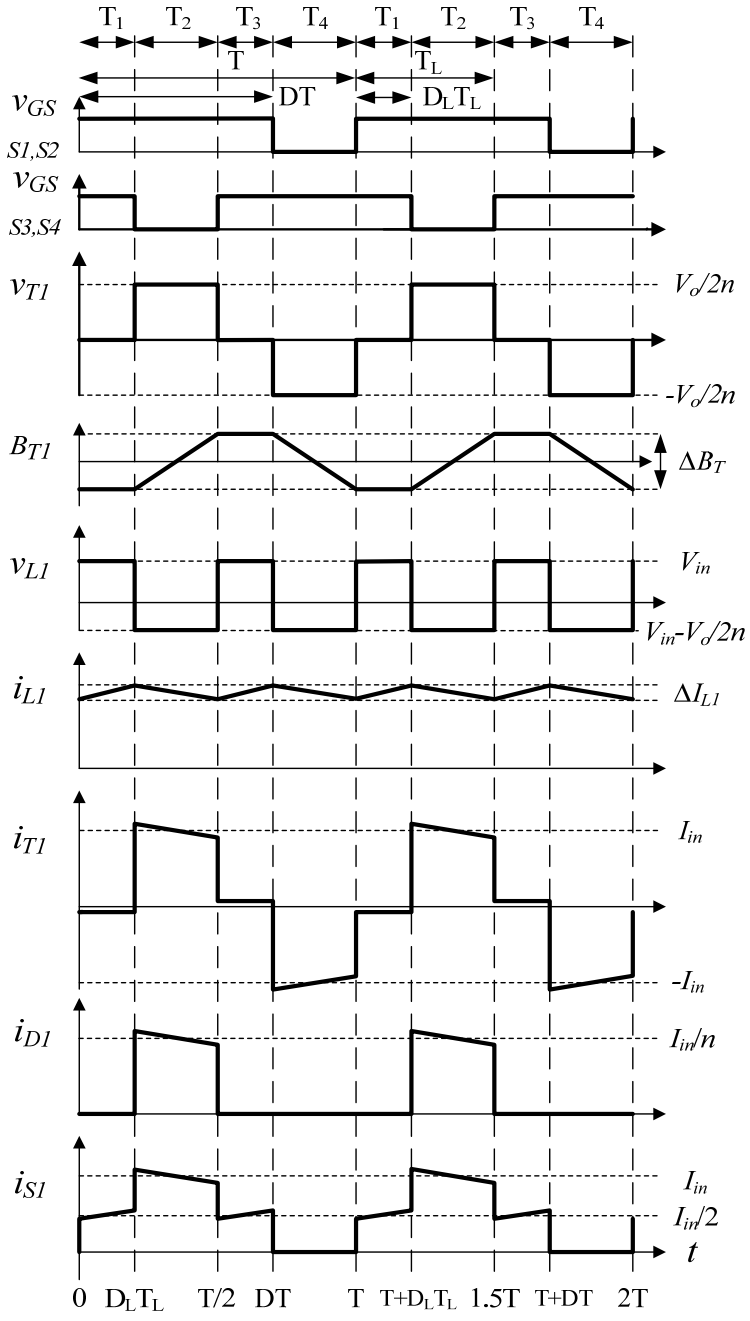

Fig. 7. Timing diagram and basic waveforms for isolated full-bridge boost converter.

State 1, First inductor charging period, T_1:
A first inductor charging period, T_1, starts when switches, S1-S2, are turned on. All switches, S1-S4, are on and the inductor current, i_{L1}, is increasing. The inductor current is shared between the two parallel branches, S1-S4 and S3-S2. Both rectifier diodes, D1-D2, are off and current in the transformer secondary winding is zero. The small transformer magnetizing current circulates in the transformer primary winding through switches, S2-S4 and/or S1-S3. Output capacitors, C1 and C2, supply the load current. The period ends when primary switches, S3 and S4, are turned off. The duration of the inductor charging period is

$$T_1 = D_L T_L = \left(D - \frac{1}{2}\right) T \tag{2}$$

Where the inductor duty cycle, D_L, and inductor period time, T_L, is defined as

$$D_L \equiv 2D - 1 \tag{3}$$

And

$$T_L \equiv \frac{T}{2} \tag{4}$$

State 2, First energy transfer period, T_2:
A first energy transfer period, T_2, starts when switches, S3 and S4, are turned off. Inductor current, i_{L1}, flows through primary switch, S1, transformer, T1, rectifier diode, D1, and output capacitor, C1, and returns to input through primary switch S2. Inductor current, i_{L1}, discharges. The period ends when primary switches, S3 and S4, are turned on again. The duration of the energy transfer period is

$$T_2 = (1 - D)T. \tag{5}$$

State 3, Second inductor charging period, T_3:
A second inductor charging period, T_3, similar to the first is initiated when switches, S3 and S4 are turned on. Only minor difference from the first inductor charging period is that transformer magnetizing current is flowing in the opposite direction in the transformer primary winding. The period ends when switches, S1 and S2, are turned off. Period time is equal to the first inductor charging period, $T_3 = T_1$.

State 4, Second energy transfer period, T_4:
Finally, a second energy transfer cycle, T_4, starts when switches, S1 and S2, are turned off. Inductor current i_{L1}, flows through switch, S3, transformer, T1 (in opposite direction compared with first energy transfer period), rectifier diode, D2, and output capacitor,, C2, and returns to input through primary switch, S4. The period ends when switches, S1 and S2, are turned on again. Period is equal to the first energy transfer period time, $T_4 = T_2$.

Total converter period time is the sum of the four state period times, T_1-T_4.

$$T = T_1 + T_2 + T_3 + T_4 \tag{6}$$

The ideal lossless converter transfer function in continuous steady state is:

$$\frac{V_o}{V_{in}} = \frac{n}{1 - D} \tag{7}$$

Where transformer turns ratio is defined as the ratio of secondary winding turn number to primary winding turn number.

$$n \equiv \frac{N_S}{N_P} \tag{8}$$

3.2.2 Isolated Full-Bridge Buck Converter

A schematic of the isolated full-bridge buck converter is presented in fig. 8. (Same as fig. 5, but repeated here for convenience). Timing diagram with basic operating waveforms are presented in fig. 9.

To minimize the voltage on output rectifiers as much as possible, a full-wave full-bridge rectifier consisting of D1-D4 is used. Since buck type converters have large discontinuous input currents, a large input ripple filter, represented by C1, is required to reduce input ripple current to acceptable levels.

3.2.2.1 Basic isolated buck converter operation

Primary switches, S1-S4, are hard switched and operated in pairs, S1-S2 and S3-S4 respectively. Drive signals are 180 degree phase shifted. Switch transistor duty cycle, D, is below 50 percent to avoid switch overlap and thus short circuit of input.

Basic converter operation can be divided into four main states.

State 1, First on-period, T_1:
A first converter on-period, T_1, starts when switches, S1-S2, are turned on. Switches, S3-S4, and diodes, D3-D4, are off. Reflected inductor current flows from input capacitor, C1, through switch, S1, transformer, T1, diode, D1, and inductor, L1 to the output, and returns to input through diode, D2, and switch, S2. The period ends when switches, S1 and S2, are turned off again. Duration of the on-period is

$$T_1 = DT. \tag{9}$$

State 2, First off-period, T_2:
A first converter off-period, T_2, starts when switches, S1 and S2, are turned off. All primary switches are off. Inductor current, i_{L1}, is free-wheeling through the two parallel branches, D1-D4 and D3-D2, to output. Inductor current is discharging. Transformer magnetizing current circulates in the transformer secondary winding and the diodes, D1-D3 and/or D2-D4. The period ends when switches, S3 and S4 are turned on.

State 3, Second on-period, T_3:
A second on-period similar to the first is initiated when switches, S3 and S4,, are turned on. Reflected inductor current flows from input capacitor, C1, through switch,, S3, transformer, T1, (in opposite direction compared to first on-period) diode, D3, and inductor, L1, to the output. Current returns to input through diode, D4, and switch, S4. The period ends when switches, S3 and S4, are turned off again. Period time is equal to the first on-period, $T_3 = T_1$.

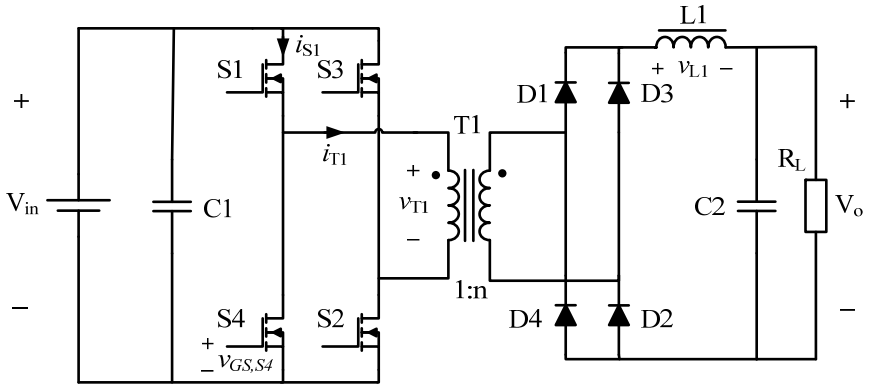

Fig. 8. Isolated full-bridge buck converter.

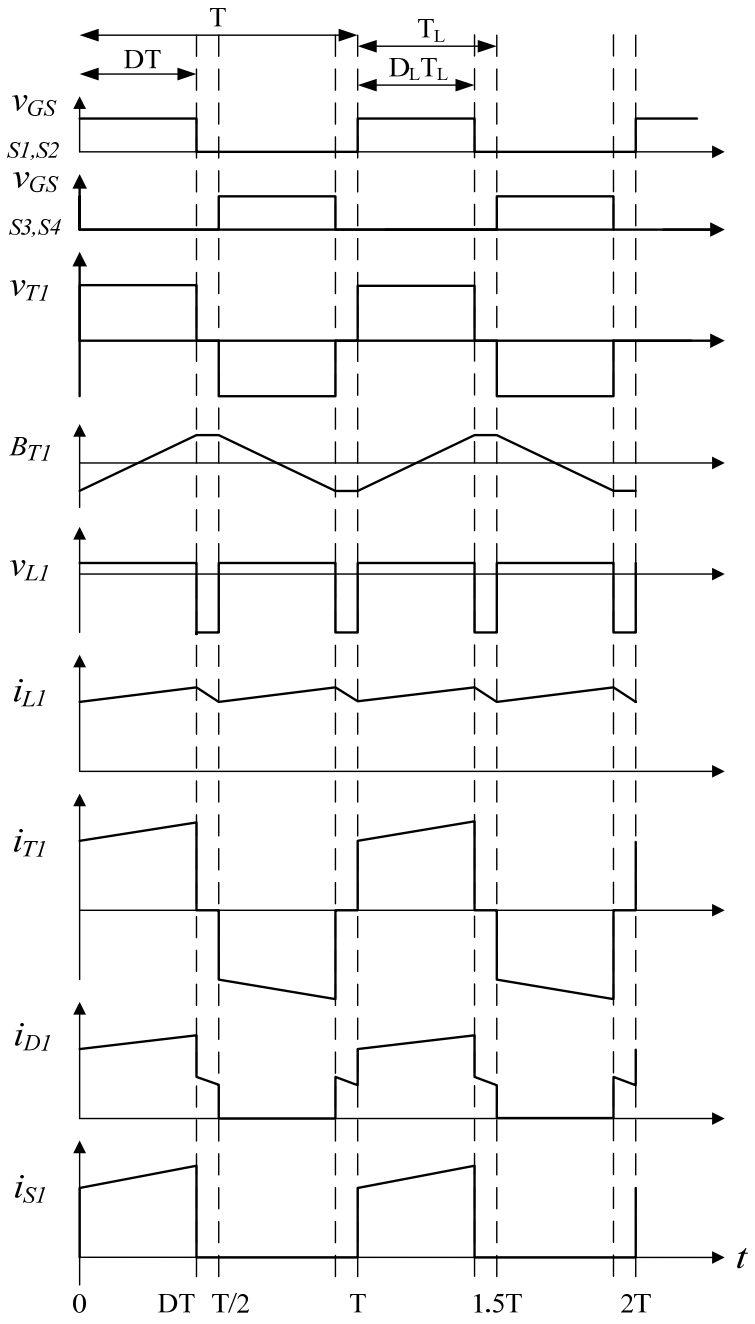

Fig. 9. Timing diagram and basic waveforms for isolated full-bridge buck converter.

State 4, Second off-period, T_4:
Finally, a second off-period starts when switches, S3 and S4, are turned off. All primary switches are off. Inductor current, i_{L1}, is free-wheeling through the two parallel branches, D1-D4 and D3-D2, to output. Inductor current is discharging. Transformer magnetizing current circulates in the transformer secondary winding (in opposite direction to first off-period) and the diodes, D1-D3 and/or D2-D4. The period ends when switches, S1 and S2, are turned on. Period time is equal to the first off-period time, $T_4 = T_2$. Duration of the off-period is

$$T_2 = \left(\frac{1}{2} - D\right)T. \tag{10}$$

Total converter period time is the sum of the four state period times T_1-T_4, and given by (6).

The ideal lossless converter transfer function in continuous steady state is:

$$\frac{V_o}{V_{in}} = 2nD \tag{11}$$

3.3 Transformer Design for High-Power Low-Voltage Converters

Transformer design for high power converters with high voltage gain is basically not different from designing any other high frequency power transformers. However, there seems to be a widespread misconception that high transformer turns ratio, as required in high gain applications, will result in large transformer leakage inductance [24], [33], [35], [42].

This assumption of large transformer leakage inductance due to high turns ratio has led to the proposal of numerous new topologies and techniques to deal with the supposedly high transformer leakage inductance. Proposed techniques include regenerative voltage clamp circuits [14], [15] and active clamp and transformer reset circuits [5], [9], [10], [12], [15], [22]-[24], [26], [27] as well as new topologies with lower transformer turns ratio such as the three phase V6 topology [33]-[37], [42].

However, as will be explained in section 3.3.1 below, the real issue in designing high frequency power transformers with high current windings is to avoid high winding ac-resistance due to severe proximity effect.

An analysis of transformer leakage inductance, in section 3.3.2, shows that not only does transformer leakage inductance not depend on transformer turns ratio, but that the extensive interleaving of primary and secondary windings needed to reduce proximity effect will dramatically reduce transformer leakage energy.

Finally, as the leakage inductance referenced to a particular winding is proportional to the number of turns squared, the very few primary turns needed on the low voltage primary winding will yield extremely small primary side leakage inductance.

The widespread acceptance that a high power transformer for low input voltage, having high turns ratio, will have high leakage inductance, is simply not correct.

3.3.1 Proximity Effect in Low-Voltage High-Power Transformers

High input current in high power fuel cell converters requires large wire copper cross section area in transformer primary windings.

Foil windings are very efficient in providing large copper cross section areas with a minimum conductor thickness. However, as power levels increase, even foil winding thicknesses quickly approach or exceed penetration depths in copper. Proximity effect can thereby cause very significant increases in winding ac-resistances thus leading to significantly increased power losses [43], [44].

In principle, Litz wire could be used. However, the very large copper cross section and few turns required on transformer primary side, make use of Litz wire difficult and impractical. Furthermore, due to the large number of individually insulated strands in Litz wires, copper space-factor is much lower than in solid copper foil windings leading to increased dc-resistance.

Using the work of Dowel [43] and Hurley [45], the increase in winding ac-resistance, R_{ac}, relative to winding dc-resistance, R_{dc}, at a specific frequency i.e. with sinusoidal excitation, due to eddy current effect is

$$F_R = \frac{R_{ac}}{R_{dc}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi - \cos 2\varphi} . \tag{12}$$

For single layer windings $\varphi = h/\delta$, and for half layer windings $\varphi = h/2\delta$.

In multi layer windings *(m > 1)* an additional term covering the proximity effect is added, thus the resistance factor becomes

$$F_R = \frac{R_{ac}}{R_{dc}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi - \cos 2\varphi} + \frac{2(m^2 - 1)}{3} \varphi \frac{\sinh \varphi - \sin \varphi}{\cosh \varphi + cos\varphi}. \tag{13}$$

Where $\varphi = h/\delta$.

Since number of turns and winding thickness are different on primary and secondary windings ($n \neq 1$), ac-resistance factors have to be calculated separately for primary, $F_{R,P}$, and secondary, $F_{R,S}$, windings. The combined effective ac-resistance for the transformer can be found as the weighted sum of the primary and secondary factors. If primary and secondary windings occupy equal winding spaces, the weighting factor becomes 0.5.

$$F_{R,T} = \frac{F_{R,P} + F_{R,S}}{2} \tag{14}$$

3.3.2 Leakage Inductance in Low-Voltage High-Power Transformers

Again, using the work of Dowel [43] and Snelling [44], an analytical expression of the transformer low frequency leakage inductance can be derived. This analytical expression is very useful in fully understanding the impact of transformer turns ratio and winding technique on transformer leakage inductance.

Stored energy in a magnetic volume, $V_{e,}$ is

$$w = V_e \int_0^{\Delta B} H \, dB \tag{15}$$

Where flux density of free space is B = μ_0 H.

The transformer windings can be grouped into a number of winding portions and intersections according to their magnetomotive force (m.m.f.) diagram as presented in fig. 10. Winding intersections constituting small volumes, $V_{\Delta} = l_w b_w h_{\Delta}$, of constantly high magnetic field strength H. Portions being volumes, $V_P = l_w b_w h_P$, of winding space where magnetic field strength, H, is increasing linearly from zero to maximum.

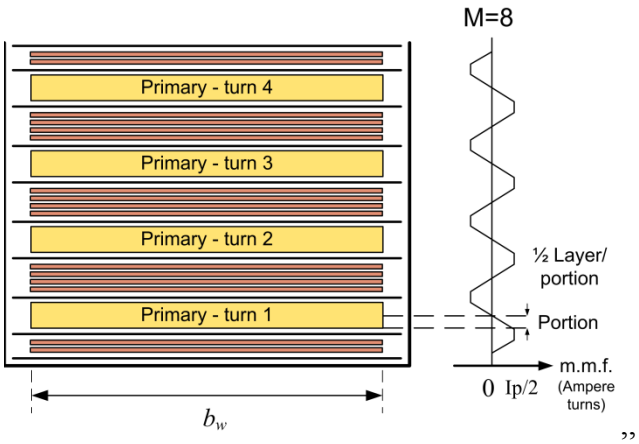

Fig. 10. Transformer winding configuration with 8 intersections, 16 portions and ½ layer primary winding.

To find the stored energy in each volume element, we integrate magnetic field strength squared, H^2, over the height of the volume element

$$w(V_P) = \frac{1}{2}\mu_0 l_w b_w \int_0^{h_P} H(x)^2 \, dx. \tag{16}$$

Where x, is the distance from the zero crossing of the magnetic field strength, H, (and m.m.f.) and is defined in the range $0 \leq x \leq h_P$.

Knowing the shape of the magnetic field strength as presented in each of the winding configuration drawings fig. 11, we can calculate the stored energy.

In each portion of the winding, the magnetic field strength H, will either be increasing or decreasing having the numerical magnitude

$$|H(x)| = \frac{NI}{Mb_w h_P} x. \tag{17}$$

The corresponding magnetic field strength in the intersection between primary and secondary windings is

$$|H(h_\Delta)| = \frac{NI}{Mb_w}. \tag{18}$$

Due to symmetry we only need to calculate the values for 1 portion and 1 intersection and then multiply by number of portions and intersections respectively.

$$w = \frac{1}{2}\mu_0 l_w b_w \left[\sum_{P=1}^{2M}\int_0^{h_P}\left(\frac{NIx}{Mb_w h_P}\right)^2 dx + \sum_{\Delta=1}^{M}\left(\frac{NI}{Mb_w}\right)^2 h_\Delta\right]$$

$$w = \frac{1}{2}\mu_0 l_w \frac{N^2 I^2}{M^2 b_w}\left(\frac{1}{3}\sum_{P=1}^{2M} h_P + \sum_{\Delta=1}^{M} h_\Delta\right) \tag{19}$$

By definition

$$w \equiv \frac{1}{2}LI^2. \tag{20}$$

Now we can find an analytical expression for the leakage inductance, L_{LK}

$$L_{LK} = \mu_0 \frac{N^2 l_w}{M^2 b_w}\left(\frac{1}{3}\sum_{P=1}^{2M} h_P + \sum_{\Delta=1}^{M} h_\Delta\right) \tag{21}$$

If $h_\Delta << h_P$ transformer leakage inductance is approximately

$$L_{LK} = \mu_0 \frac{l_w h_w}{3b_w}\frac{N^2}{M^2}. \tag{22}$$

From (21) and (22) it is clear that extensive interleaving of primary and secondary windings, as required in high-power low-voltage transformers, will lead to very small stored energy in transformer leakage inductance.

Further, it becomes evident that with leakage inductance being proportional to number of turns squared N^2, the few turns required on primary windings of low-voltage high-power transformers, will inherently have extremely small leakage inductance.

Finally, transformer leakage inductance for a given winding - as expressed in (21) and (22) - does not depend on number of turns on any other windings. Therefore leakage inductance in a transformer is not a function of transformer turns ratio but only depends on winding technique and number of turns on the specific winding in question.

3.3.3 Analysis of Four Alternative Winding Designs

To illustrate the importance of controlling eddy current and proximity effect losses in high frequency power transformers for low input voltage applications, we will use the analytical

expressions developed in section 3.3.1 and 3.3.2 to analyse winding ac-resistance and leakage inductance of the 4 alternative winding configurations shown in fig. 11 (a)-(d).

A power transformer for a 1.5 kW isolated boost converter operating down to 30 V input requires a transformer turns ratio of 1:4 [A1], [A2]. Switching at 45 kHz, an EE55/21 ferrite E-core with 4 primary turns can transfer the power. Thus, sixteen secondary turns are required.

At 45 kHz, penetration depth in copper is only 0.34 mm. A primary winding with 4 turns on an EE55/21 core, will allow each of the 4 primary turns to be up to 0.6 mm thick. The 16 turn secondary winding can be realized by using 0.15 mm copper foil.

Using (12)-(14), transformer winding ac resistance factors for the 4 alternative winding configurations of fig. 11 (a)-(d) are calculated and presented in table III. Notice, that primary winding ac resistance in the winding configuration of fig. 11 (a) is 13 times larger than in winding configuration fig. 11 (d).

This clearly illustrates that to achieve low ac-resistance in high frequency high-current transformer windings, extensive interleaving of primary and secondary windings is required.

Using (21), the leakage inductances for the 4 alternative winding configurations in fig. 11 (a)-(d) are calculated and presented in table III. Notice that leakage inductance in the winding configuration of fig. 11 (d) is approx. 35 times smaller than the corresponding leakage inductance in the winding configuration of fig. 11 (a).

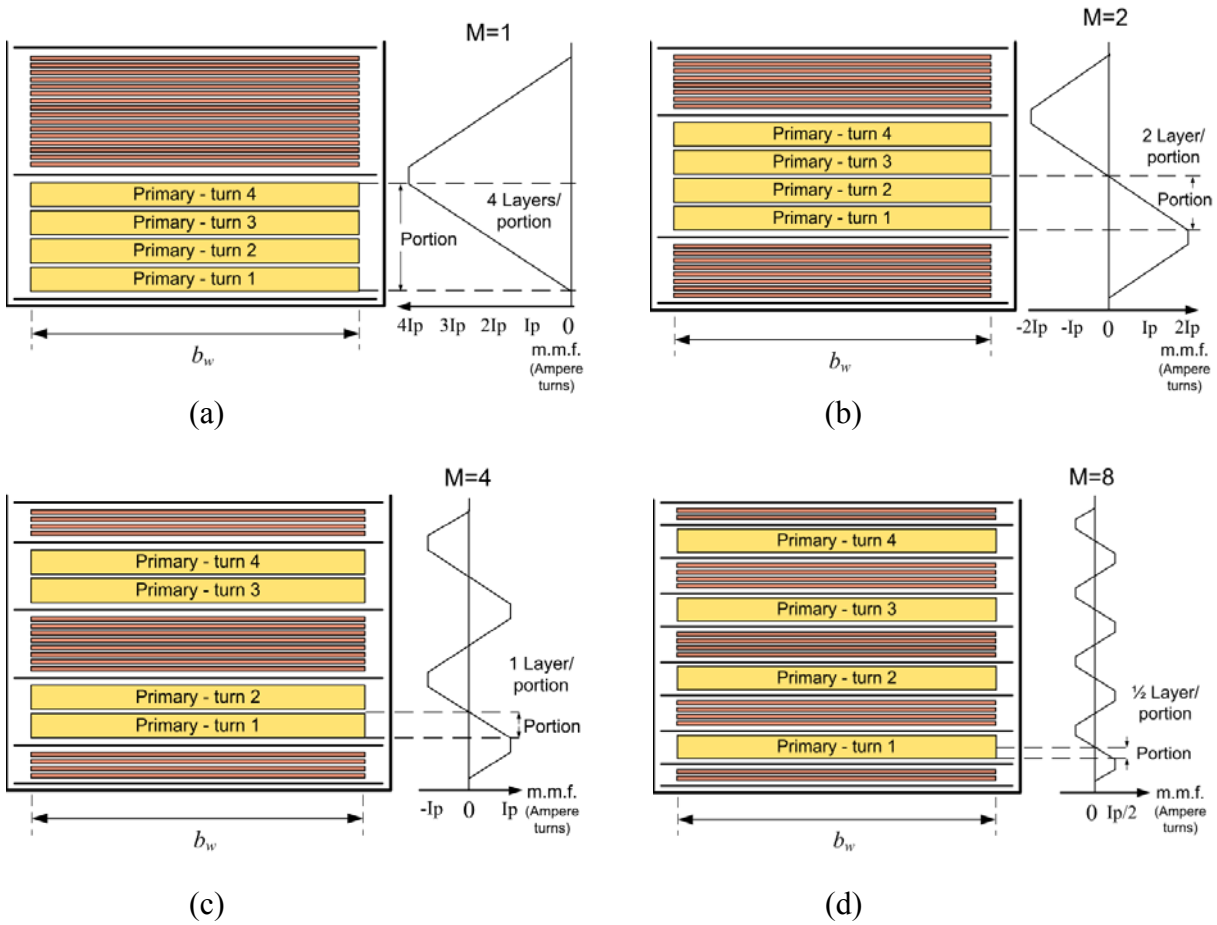

Fig. 11. Alternative transformer winding configurations. Without interleaving (a), single interleaving (b), double interleaving (c) and quadruple interleaving (d).

Also notice that this analysis does not include any stray inductance or ac-resistance effects caused by transformer terminal leads.

Summarizing, the need to reduce proximity effect in high-power low-voltage transformers requires extensive interleaving of windings. This extensive interleaving will dramatically reduce transformer leakage inductance, and thereby stored energy in transformer leakage inductance. Finally, the few primary turns required in transformers for low input voltage, will result in power transformers having exceptionally low leakage inductance.

TABLE III.
CALCULATED AC-RESISTANCE FACTOR AND TRANSFORMER LEAKAGE INDUCTANCE FOR 4 ALTERNATIVE WINDING DESIGNS

Winding design	A	B	C	D
Intersections M	1	2	4	8
$F_{R,P}$	13.3	3.96	1.63	1.05
$F_{R,S}$	2.07	1.27	1.07	1.02
$F_{R,T}$	7.7	2.6	1.35	1.04
$L_{LK,P}$ [nH]	249	70	21	7.2
$L_{LK,S}$ [nH]	3,976	1,114	339	115

3.3.4 Experimental Verification/Results

The transformer corresponding to the configuration in fig. 11 (d), was manufactured and leakage inductance and ac resistance were tested on an Agilent 4294A Precision Impedance Analyzer.

Leakage inductance and ac resistance are measured into secondary winding with primary winding shorted. Test result is shown in fig. 12.

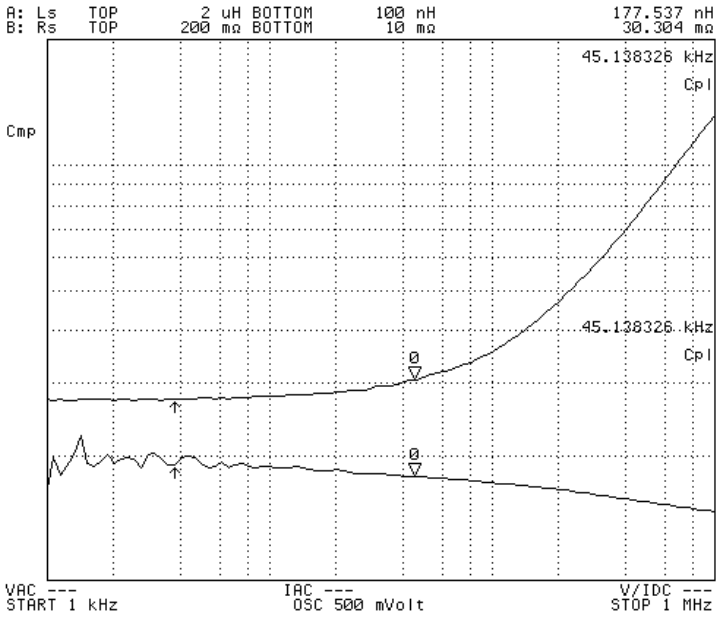

Fig. 12. Measured secondary side ac resistance (upper curve) and leakage inductance (lower curve) of 1.5 kW transformer.

Transferred to primary side, ac resistance at 45 kHz is 1.9 mΩ and leakage inductance is only 11 nH. Notice, the measured ac resistance and leakage inductance even include the parasitic resistance and stray inductance of the transformer terminal leads.

The leakage inductance in percentage of primary magnetizing inductance is only 0.01%.

The experimental test results therefore confirm the theoretical analysis and demonstrate the extremely low leakage inductances that are achieved in optimally designed high power transformers for low voltage applications.

The transformer is used in the 1.5 kW converter published in appendixes [A1], [A2], and also in the 3 kW converter published in appendix [A5].

3.4 Power MOSFET Losses

At present, power MOSFETs constitute the best available technology for low voltage switches. Alternative technologies such as IGBTs have much slower switching speed and in particular high saturation voltages which at a minimum voltage of only 30 V will result in very large power losses.

In the following, the significant loss factors involved when using power MOSFETs as primary switches in high-power low-voltage converters will be analyzed.

3.4.1 MOSFET Conduction Losses

Due to the very high input current, primary switch conduction losses are dominant loss factors in high-power low-voltage converters. Thus, optimum design and selection of primary switches are obviously very important in achieving high conversion efficiency.

In the on-state, power MOSFET conduction loss is purely resistive and switch conduction loss is given by

$$P_{DS,con} = R_{DS(on)} I_{DS,rms}^2. \tag{23}$$

For a constant power MOSFET chip area, two factors therefore determine the switch conduction losses – switch rms current, $I_{S,rms}$, and switch on-resistance, $R_{DS(on)}$. Switch rms current is a function of selected converter topology [A3].

For a constant chip area, power MOSFET on-resistance increases exponentially with rated drain-source breakdown voltage, $V_{(BR)DSS}$ [46].

$$R_{DS(on)} \propto V_{(BR)DSS}^{2.5\ to\ 2.7} \tag{24}$$

Due to terminal resistances from leads and bonding wires becoming significant at lower voltages, the exponential coefficient is closer to 2 in the power and voltage range (75-150 V) considered in this project. Comparing the two International Rectifier power MOSFETs, IRFB3077 and IRFP4321, rated for 75 V and 150 V respectively and having typical on-resistances of 2.8 mΩ and 12 mΩ [47], we get an exponential coefficient of 2.1. To be conservative, we will use an exponential coefficient of 2 in the following analysis.

For a given chip size and technology, power MOSFET conduction losses are thus proportional to

$$P_{DS,con} \propto V_{(BR)DSS}^2 I_{DS,rms}^2. \tag{25}$$

From (25), it is evident that any possibility of reducing device voltage stress and consequently rated device voltage will dramatically reduce conduction losses in the primary switches and thus significantly increase converter efficiency.

If the switch voltage rating can be reduced by a factor of 2, (from 150 V to 75 V) the total switch conduction losses would be reduced by minimum a factor of 4. Alternatively, the number of switches needed could be reduced by a factor of 4, thus dramatically saving component cost, size, drive power and switching losses.

The primary switch rms current in an isolated boost converter can be expressed as [A3]

$$I_{S,rms,Boost} = I_{in} \frac{\sqrt{3-2D}}{2} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{L1}}{2I_{in}}\right)^2} \tag{26}$$

If the inductor ripple current is much smaller than the dc input current, $\Delta i_{L1} << I_{in}$, then switch rms current becomes approximately

$$I_{S,rms,Boost} \approx I_{in} \frac{\sqrt{3-2D}}{2} = \frac{P_o}{\eta V_{in}} \frac{\sqrt{3-2D}}{2} \tag{27}$$

Total conduction losses in the primary switches of a full-bridge boost converter thus become

$$P_{FB,con,Boost} = R_{DS(on)}(3-2D)\left(\frac{P_o}{\eta V_{in}}\right)^2 \tag{28}$$

The corresponding equations for the full-bridge buck converter are [A3]

$$I_{S,rms,Buck} = I_o n \sqrt{D} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_S}{2nI_o}\right)^2} \tag{29}$$

If the switch ripple current is much smaller than the reflected input current, $\Delta i_S << nI_o$, then the switch rms current becomes approximately

$$I_{S,rms,Buck} \approx I_o n \sqrt{D} = \frac{P_o}{V_o} n \sqrt{D} \tag{30}$$

Total conduction losses in the primary switches of a full-bridge buck converter thus become

$$P_{FB,con,Buck} = 4R_{DS(on)} D \left(\frac{P_o}{V_o} n\right)^2 \tag{31}$$

If a buck and a boost converter are using the same primary switches, their relative switch conduction losses for the same operating point will be

$$\frac{P_{FB,con,Boost}}{P_{FB,con,Buck}} = \left(\frac{I_{S,rms,Boost}}{I_{S,rms,Buck}}\right)^2 = \frac{3-2D_{Boost}}{4D_{Buck}}\left(\frac{V_o}{n_{Buck}\eta_{Boost}V_{in}}\right)^2 \quad (32)$$

From the experimental comparison of the two converters published in [A3], we have the following comparable data for maximum output power and minimum input voltage:

V_o=400 V, $V_{in,min}$=30 V, n_{Buck}=16, η_{Boost}=0.967, D_{Boost}=0.7 and D_{Buck}=0.425.

Using (32), the ratio of the primary switch conduction losses at maximum output power and minimum input voltage become

$$\frac{P_{FB,con,Boost}}{P_{FB,con,Buck}} = 0.70 \quad (33)$$

Even if we base the comparison on the ideal lossless transfer functions for each of the two converter topologies given by (7) and (11) and further assuming that operating duty cycle of the buck converter can reach 50% i.e. not having any regulation headroom left, we will still see larger losses in the buck converter primary switches due to the inherently larger rms currents. The theoretical, however unrealistic, numbers would be:

V_o=400 V, $V_{in,min}$=30 V, n_{Buck}=13.33, n_{Boost}=3.33, η_{Boost}=1, D_{Boost}=0.75 and D_{Buck}=0.5.

Again using (32), we get a theoretical best case ratio between the squared primary switch rms currents - and thereby their conduction losses - of

$$\left(\frac{I_{S,rms,Boost}}{I_{S,rms,FB\ Buck}}\right)^2 = 0.75 \quad (34)$$

This means, that fundamentally the rms currents in the primary switches of the isolated boost converter are smaller than in the isolated full-bridge buck converter. If the same power MOSFETs can be used in buck and boost converters, the conduction losses in primary switches of the boost converter will be significantly lower than in comparable buck converters.

Theoretically, boost converters have at least 25% less conduction losses in primary switches. In practice this difference will be even higher since the buck converter cannot reach the full theoretical maximum duty cycle of 50%. In the comparative experimental study presented in [A3], the boost converter has 30% less conduction losses than a comparable buck converter.

To quantify the importance of conduction losses in the primary switches, we can use (28) to calculate the total primary switch conduction loss in the 1.5 kW boost converter in [A2]. Typical drain-source on-resistance of the IRFB3077 power MOSFET is 3.5 mΩ at 60°C [47]. At 30 V input and 1.5 kW output, converter duty cycle is D=0.7 and measured efficiency is η=0.968 [A2]. Total conduction losses in the 4 primary switches are

$$P_{FB,con,1.5\ kW} = R_{DS(on)}(3-2D)\left(\frac{P_o}{\eta V_{in}}\right)^2 = 14.9\ W. \quad (35)$$

Corresponding to a 1% loss of efficiency - or 30% of all converter losses - at maximum output power and minimum input voltage.

3.4.2 Power MOSFETs rated for repetitive avalanche

Modern power MOSFETs are rated for repetitive avalanche [47]. Failure mode is purely thermal, occurring at temperatures well in excess of rated device temperatures [47]. This effectively means that as long as device ratings are not exceeded, devises can operate under repetitive avalanche conditions. Thus, voltage clamping circuits traditionally used to avoid avalanche in these devices are no longer needed for device protection.

Special care has to be taken during device paralleling, since current sharing during avalanche cannot be guaranteed between paralleled devices. Avalanche voltage levels will differ between paralleled devices, thus the device having the lowest avalanche voltage will receive the full current from all parallel devices, potentially overstressing current rating and thermal rating of that device [48].

3.4.3 Power MOSFET Turn-off Losses

During a hard switched power MOSFET turn-off, drain-source voltage first has to commutate in order to open an alternative current path before drain current can start to decay. This first turn-off phase – the voltage switching phase - is well known from literature and described in many power electronic textbooks [46].

During power MOSFET turn-off, voltage rise time is controlled by the ability of the gate driver circuit to sink the current being delivered to the gate by the gate-drain Miller-capacitor as the drain voltage increases and thus charges the gate-drain capacitor. If the gate driver current exceeds the power MOSFET gate-drain feedback current during voltage switching, power MOSFET transistor will be off during the capacitive charging of the power MOSFET output capacitance, C_{OSS}. In boost converters (and many others), this charging is performed by an inductive element and charging is thus lossless.

During hard switched turn-on, the stored capacitive charge in the power MOSFET output capacitor, C_{OSS}, is however dissipated in the power MOSFET channel. At higher voltage levels and/or high switching frequencies such as in off-line applications, voltage switching losses can become a dominant loss factor. Consequently, many soft switching schemes have been developed to save voltage switching losses in high-input-voltage applications [49].

Since voltage switching losses have traditionally been the main concern with regard to switching losses in switch-mode power converters, the topic has been extensively treated in literature and in many power electronic textbooks [46] and will thus not be treated any further here.

In high input current applications however, power MOSFET current switching losses can become a very significant source of power losses. Furthermore, since efficiency critical high input current applications are relatively new, high-frequency high-current switching has not yet received a similar attention in literature.

The following sections will present a detailed analysis of power MOSFET current switching behavior and its impact on converter switching losses.

Power MOSFET common source inductance and gate driver voltage determine maximum power MOSFET current turn-off speed.

In boost converters, the ratio of commutation inductance to power MOSFET common source inductance will determine in which of two alternative current commutation modes the converter will operate.

In the following, the two current commutation modes will be analyzed in detail. Analytical expressions for converter commutation losses in each of the two modes are developed together with an expression for the boundary condition between the two modes.

These analytical expressions are therefore very useful in designing and optimizing high input current converters for high conversion efficiency.

Finally, the analytical results are verified by comparing measured current switching performance from two prototype converters - a 1.5 kW and a 10 kW isolated full-bridge boost converter.

3.4.3.1 Power MOSFET Current Switching Speed

Common source inductance sets a fundamental upper limit to the current switching speed in a power MOSFET during turn-off [50].

The equivalent circuit in fig. 13, represents the situation during power MOSFET current switch off.

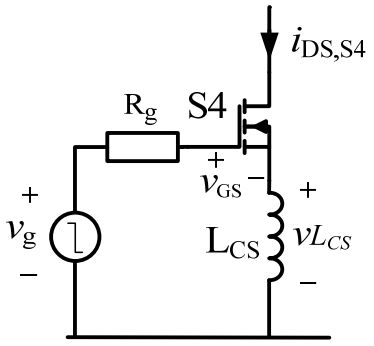

Fig. 13. Power MOSFET with parasitic common source inductance feedback to gate.

Total common source inductance is represented by a lumped parasitic inductance L_{CS}, common to the load current, represented by i_{DS}, and the gate driver loop. The lumped common source inductance is the sum of device internal parasitic bond wire inductance, device package common source parasitic lead inductance (determined by lead length) and any additional circuit layout related common stray inductance.

While the external common stray inductance can be controlled by proper circuit layout (Kelvin type layout), the device related internal bond wire inductance and parasitic lead inductance, is purely a function of device package design.

Using a fast gate drive circuit, gate drive output voltage, *vg*, will have reached its off-potential long before device drain current starts to decay.

During power MOSFET current turn-off, the negative current slope created by the decaying drain-source current, di_{DS}/dt, induces a negative voltage across the common source inductance. Since the common source inductance is also in series with the gate-source loop, the negative voltage induced across the common source inductance appears as a positive gate-source voltage on the power MOSFET.

When power MOSFET gate-source voltage reaches the voltage level required to conduct the drain-source current, $V_{GS}(i_{DS})$, the device will be operating in its active linear mode having high drain-source voltage. Due to the negative feedback, the power MOSFET will effectively limit rate-of-current-decay i.e. negative di_{DS}/dt to a fixed upper limit. Any tendencies to exceed this upper limit will increase power MOSFET gate-source voltage further, causing power MOSFET to reduce the slope of the negative di_{DS}/dt, thereby effectively controlling maximum current switch off speed.

Induced voltage across common source inductance is given by

$$v_{Lcs} = L_{CS}\frac{di_{DS}}{dt}. \tag{36}$$

Gate-source voltage is given by

$$v_{GS} = v_g - v_{Lcs} \tag{37}$$

The maximum power MOSFET current switch off speed can be found by combining (36) and (37).

$$\frac{di_{DS}}{dt} = \frac{v_g - V_{GS}(i_{DS})}{L_{CS}} \tag{38}$$

For a gate driver output voltage of zero, we have a maximum power MOSFET current turn-off speed of

$$\frac{di_{DS}}{dt} = -\frac{V_{GS}(i_{DS})}{L_{CS}} \tag{39}$$

From (38) we can also see that by applying negative gate driver output voltage during power MOSFET turn-off, current switching speed can be increased. This, however, comes at the expense of added gate driver complexity and increased gate drive losses.

3.4.3.2 Voltage Limited Current Commutation – Mode 1

In isolated boost converters having large commutation inductance, current commutation speed is limited by clamp voltage.

An isolated full-bridge boost converter is presented in fig. 14. A voltage clamp circuit represented by diode, D3, and voltage source, V_{CL}, limit primary switch overvoltage during

commutation of current to output. Commutation inductance, LX, is the sum of transformer leakage inductance, L_{LK}, primary stray inductance, L_{SP}, and reflected secondary stray inductance, L_{SS}/n^2.

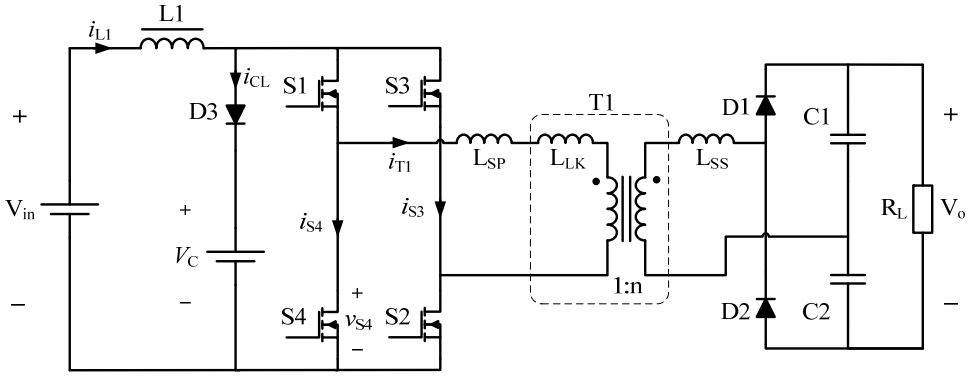

Fig. 14. Isolated full-bridge boost converter with voltage clamp circuit and commutation inductance.

A timing diagram showing waveforms for the voltage limited current commutation period is presented in fig. 15. Referring to fig. 14, and fig. 15, the basic current commutation process is explained.

Turn-off process starts when S3 and S4 gate driver output switches to its low state voltage at t_0=DT.

Voltage switching period ($T_1=t_1-t_0$)**:**
Drain-source voltage rises quickly, gate-source voltage is charged to $V_{GS}(i_D)$ by the gate-drain Miller capacitor. Current stays in switches since no alternative current path is yet open.

MOSFET current switch off period ($T_2=t_2-t_1$)**:**
When drain-source voltage reaches reflected output voltage, drain current starts to decay at its maximum current switching speed set by common source inductance. Transformer current increases linearly at a rate determined by the commutation inductance and the clamp voltage minus reflected output voltage. Remaining inductor current flows into clamp circuit. At the end of the period, current in switches, S3 and S4, reaches zero and transistors are turn-off. Duration of period is given by maximum power MOSFET di/dt and inductor current level.

Inductor current clamping period ($T_3=t_3-t_2$)**:**
Inductor current is now shared between clamp circuit and transformer. Transformer current continues to increase at the same rate, and clamp circuit current is reduced at the same rate. At the end of the period, all inductor current has commutated into the output.

Total power loss during current commutation is given by the integral of transformer current from t_1 to t_3 multiplied by the clamp voltage.

The current going into the clamp circuit can potentially be recovered by conversion to input or output.

$$\frac{L_X}{L_{CS}} > \left(V_C - \frac{V_o}{2n}\right)\left(\frac{1}{2V_{GS}(i_{S4})} + \frac{2n}{V_o}\right)$$

$$\frac{L_X}{L_{CS}} < \left(V_C - \frac{V_o}{2n}\right)\left(\frac{1}{2V_{GS}(i_{S4})} + \frac{2n}{V_o}\right)$$

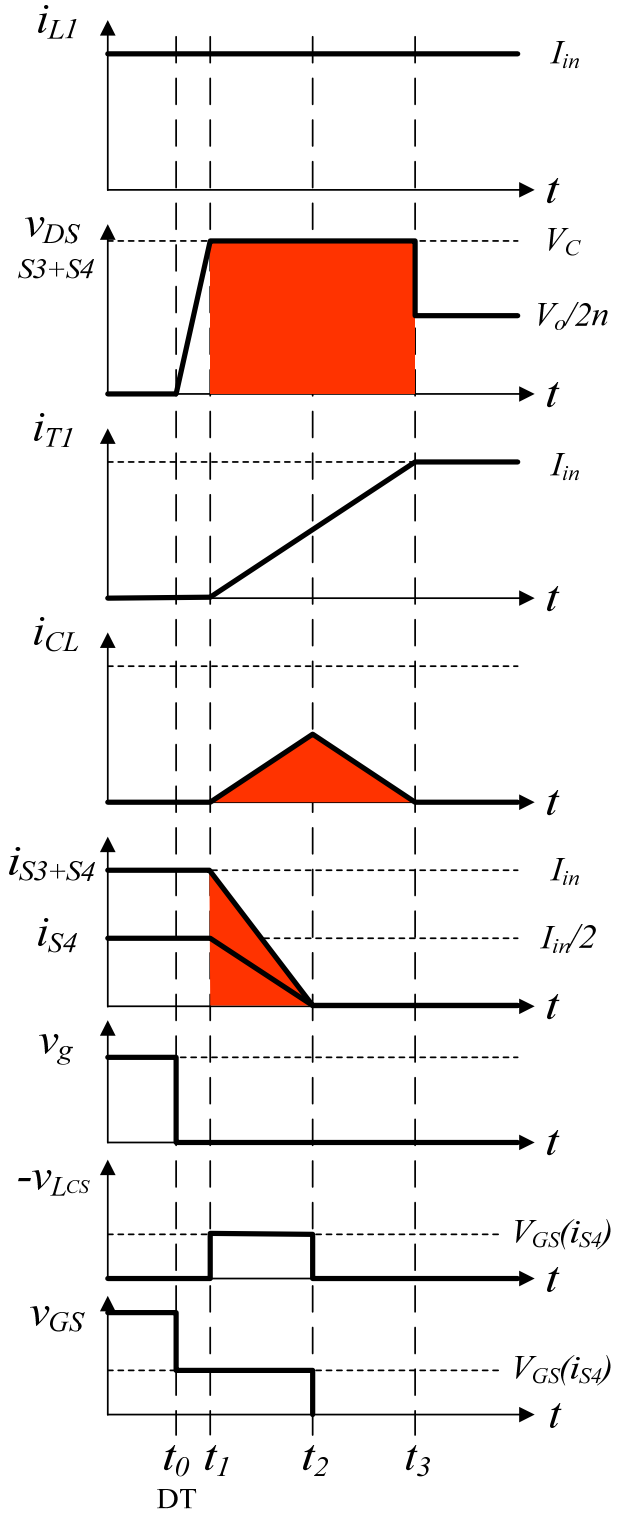

Fig. 15. Timing diagram for voltage limited current commutation – mode 1.

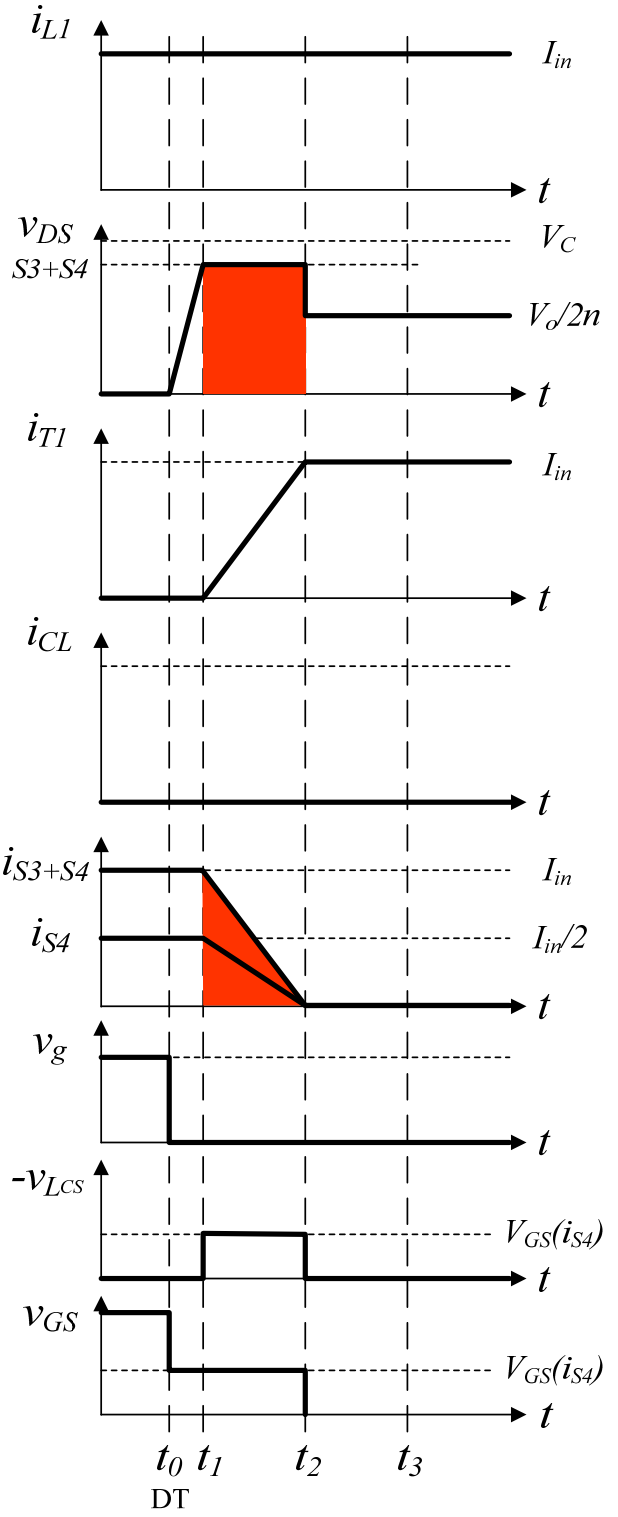

Fig. 16. Timing diagram for power MOSFET limited current commutation – mode 2.

The converter has two current commutation cycles in each switching period. Total commutation loss is the sum of clamp circuit power and power loss in switches and is given by

$$P_{CC-VL} = 2f_s \int_{t_1}^{t_3} V_C i_{T1}\, dt \tag{40}$$

Where

$$\frac{di_{T1}}{dt} = \frac{V_C - \frac{V_o}{2n}}{L_X} \tag{41}$$

Where the commutation inductance is defined as

$$L_X \equiv L_{SP} + L_{LK} + {}^{L_{SS}}/_{n^2}. \tag{42}$$

Since transformer current has to increase from zero to inductor, L1, current during total commutation time we have

$$t_3 - t_1 = \frac{I_{L1,peak}}{\frac{di_{T1}}{dt}} = \frac{L_X}{V_C - \frac{V_o}{2n}} I_{L1,peak} \tag{43}$$

Where peak inductor, L1, current is given by

$$I_{L1,peak} = \frac{P_o}{\eta V_{in}} + \frac{\Delta i_{L1}}{2}. \tag{44}$$

By combining (40) – (44), we get an expression for the total converter clamping power

$$P_{CC-VL} = \frac{f_s V_C}{V_C - \frac{V_o}{2n}} L_X I_{L1,peak}^2 \tag{45}$$

In the typical case where clamping voltage, V_C , is approximately 2 times the reflected output voltage i.e. $V_C \approx 2V_o/n$, and secondary stray inductance transferred to primary side can be ignored due to high transformer turns ratio, and finally that inductor ripple current is much lower than maximum input dc current, converter clamping power becomes

$$P_{CC-VL} \approx 2f_s(L_{SP} + L_{LK})I_{in}^2 \tag{46}$$

Where I_{in}, is the converter dc input current.

3.4.3.3 Power MOSFET Limited Current Commutation – Mode 2

If we reduce the commutation inductance (or increase the power MOSFET common source inductance) in the isolated boost converter of fig. 14, converter current commutation will change into being controlled by power MOSFET maximum turn-off current speed.

In this mode, switch voltage levels never reach clamp voltage levels and converter current commutation is therefore controlled by power MOSFET maximum current turn-off di/dt. In chapter 3.4.3.1, we found that maximum current turn-off speed in a power MOSFET is controlled by the common source inductance which minimum value is again given by package layout. This means that for a given device package design, the fastest converter current commutation achievable, and thus the lowest losses, is obtained when converter current commutation is limited only by the power MOSFET maximum turn-off di/dt.

Timing diagram with voltage and current waveforms for the current commutation period is presented in fig. 16. Referring to fig. 14 and fig. 16, the basic current commutation process is explained.

Turn-off process starts when S3 and S4 gate driver output switches to its low state voltage at t_0=DT.

Voltage switching period, ($T_1=t_1-t_0$)**:**
Drain-source voltage rises quickly, gate-source voltage is charged to $V_{GS}(i_D)$ by the gate-drain Miller capacitor. Current stays in switches since no alternative current path is yet open.

MOSFET current switch off period ($T_2=t_2-t_1$)**:**
When drain-source voltage reaches reflected output voltage, drain current starts to decay at its maximum current switching speed set by common source inductance. Due to low commutation inductance, drain-source voltage does not reach voltage clamping level. Thus, clamping circuit is not activated. Transformer current increases linearly at the same rate as the decaying switch current. Converter current commutation is completed when current in switches, S3 and S4, reaches zero, and transistors are turned off. Duration of current commutation is given by the maximum power MOSFET di/dt and inductor, L1, current level.

Total power loss during current commutation is given by the integral of transformer current from t_1 to t_3 multiplied by the switch drain-source voltage, v_{S4}.

The converter has two current commutation cycles in each switching period. Total converter commutation loss shared by the four switches is given by

$$P_{CC-CL} = 2f_s \int_{t_1}^{t_2} v_{S4} i_{T1}\, dt \tag{47}$$

Where

$$v_{S4} = \frac{V_o}{2n} + L_X \frac{di_{T1}}{dt} + V_{GS}(i_{S4}) \tag{48}$$

and

$$\frac{di_{T1}}{dt} = -2\frac{di_{S4}}{dt} = \frac{2V_{GS}(i_{S4})}{L_{CS}} \tag{49}$$

During current commutation, the transformer current changes from zero to peak inductor current

$$\Delta i_{T1} = \int_{t_1}^{t_2} \frac{di_{T1}}{dt}\, dt = I_{L1,peak} \tag{50}$$

Using (49) and (50), we can find the duration of the current commutation

$$t_2 - t_1 = \frac{L_{CS}}{2V_{GS}(i_{S4})} I_{L1,peak} \tag{51}$$

By combining (48) and (49), we can find an expression for the switch drain-source voltage

$$v_{S4} = \frac{V_o}{2n} + \frac{2L_X + L_{CS}}{L_{CS}} V_{GS}(i_{S4}) \tag{52}$$

Combining (47), (49), (52) and (55), we can now find an expression for the full-bridge boost converter total current commutation losses in the current limited case

$$P_{CC-CL} = 2f_s \int_{t_1}^{t_2} v_{S4} \frac{di_{T1}}{dt} t dt \tag{53}$$

$$P_{CC-CL} = 2f_s \int_{t_1}^{t_2} \left(\frac{V_o}{2n} + \frac{2L_X + L_{CS}}{L_{CS}} V_{GS}(i_{S4}) \right) \frac{2V_{GS}(i_{S4})}{L_{CS}} t dt \tag{54}$$

Total current commutation loss in mode 2 becomes

$$P_{CC-CL} = f_s \left[\left(1 + \frac{V_o}{4nV_{GS}(i_{S4})} \right) L_{CS} + L_X \right] I_{L1,peak}^2 \tag{55}$$

3.4.3.4 Mode 1 versus Mode 2 Current Commutation

By comparing the two power loss equations for current commutation mode 1 and mode 2 (45) and (55), we get an expression for the boundary condition between the two current commutation modes.

$$\frac{L_X}{L_{CS}} = \left(V_C - \frac{V_o}{2n} \right) \left(\frac{1}{2V_{GS}(i_{S4})} + \frac{2n}{V_o} \right) \tag{56}$$

If the ratio of commutation inductance, L_X, to common source inductance, L_{CS}, is larger than the right hand side expression in (56), converter current commutation operates in mode 1 and is controlled by commutation inductance and available clamp or avalanche voltage according to (45).

Condition for mode 1 operation is therefore:

$$\frac{L_X}{L_{CS}} > \left(V_C - \frac{V_o}{2n} \right) \left(\frac{1}{2V_{GS}(i_{S4})} + \frac{2n}{V_o} \right) \tag{57}$$

If, however, the commutation inductance can be reduced to a level lower than the critical ratio given by (56), the converter current commutation operates in mode 2, and we have the following condition for mode 2 current commutation:

$$\frac{L_X}{L_{CS}} < \left(V_C - \frac{V_o}{2n}\right)\left(\frac{1}{2V_{GS}(i_{S4})} + \frac{2n}{V_o}\right) \tag{58}$$

In mode 2, converter current commutation is only limited by the power MOSFET current turn-off speed which is determined by the common source inductance according to (55).

Comparing losses in the two modes, we can see that mode 2 operation will always be more efficient than mode 1 operation.

Since common source inductance, L_{CS}, is a function of power MOSFET package design and physical layout, then a given power MOSFET will have the same current turn-off waveform in mode 1 and mode 2 operation fig. 15, and fig. 16. Since switch voltage in mode 2 does not reach clamp voltage level – and is therefore lower than in mode 1 - current switching losses in mode 2 will be smaller than in mode 1.

In addition to these non-recoverable losses in the power MOSFETs, current commutation mode 1 will also have power losses associated with the clamping current, i_{CL}, in periods, T_2 and T_3. If voltage clamping is performed by an external circuit as shown in fig. 14, most of this clamp energy can be recovered to input or output by a dedicated converter [14], [20], [23], [25] or the use of active clamp circuits [9], [10], [12], [15], [21]-[24], [26], [27]. This will, however, require much higher voltage rating on primary switches and thereby lead to a dramatic increase in primary switch conduction losses as explained in chapter 3.4.1.

To conclude, if we can reduce commutation inductance to a level below the critical ratio given by (56), we can eliminate the voltage clamp circuit **and** at the same time reduce current commutation losses. Without the voltage clamp circuit, we can now reduce the primary switch voltage rating by approximately a factor of 2 [10], [20]-[25] thereby reducing conduction losses in primary switches by a factor of 4, thus achieving a very significant increase in converter conversion efficiency.

3.4.3.5 Experimental results

To illustrate the usefulness of the above analysis and the importance of achieving fast current switching, measured power MOSFET turn-off waveforms from the 1.5 kW isolated boost converter [A1], [A2] and the 10 kW isolated R4 boost converter [A6] are analyzed and compared in this subsection.

In fig. 17, measured power MOSFET switch-off waveforms on a 1.5 kW isolated boost converter [A2] at full load and minimum input voltage (1500 W & 30 V) are presented.

Straight-line approximations are superimposed on top of the measured oscilloscope traces in order to ease interpretation and measurement of waveform data. Red lines on top of light blue current trace and black lines on top of green voltage trace.

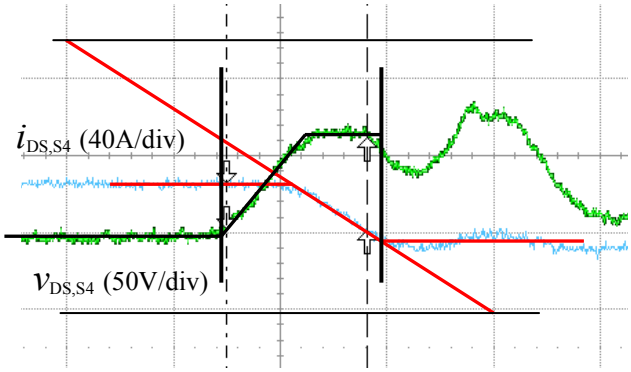

Fig. 17. Measured switch S4 turn-off sequence in 1.5 kW isolated boost converter. Time base is 20 ns/div.

By measuring the power MOSFET switch-off current di/dt and using (39), we can estimate the total power MOSFET common source inductance, L_{CS}, in the converter prototype. The power MOSFET is an IRFB3077 in a TO-220AB package from International rectifier. Typical gate-source voltage as function of drain current can be found in the product data sheet [47].

Measured turn-off di/dt in fig. 17, is

$$\frac{di_{S4}}{dt} = \frac{\Delta i_{DS,S4}}{\Delta t} \approx -1.8 \ {}^{A}/_{ns}. \tag{59}$$

Power MOSFET gate-source voltage at 28 A is typically: $V_{GS,IRFB3077}(28\ A) \approx 3.9\ V$ [47].

Using (39), we can then find an estimated value of the total power MOSFET common source inductance

$$L_{CS} \approx \frac{-V_{GS}(i_{S4})}{\frac{di_{S4}}{dt}} = 2.2\ nH \tag{60}$$

By evaluating the straight-line approximated curve forms in fig. 17, and using (47), the total converter turn-off losses can be estimated

$$P_{SW-1.5\ kW} = 2f_s \int_{t_1}^{t_2} v_{S4} i_{T1}\, dt \ \approx 2f_s \Delta v_{S4} \Delta i_{S4} \Delta t = 5.3\ W \tag{61}$$

Corresponding to only 0.35% loss of efficiency at 1500 W.

Similarly, measured power MOSFET switch-off waveforms from a 2.5 kW power stage in a 10 kW isolated boost converter [A6] is presented in fig. 18. The converter is operating at full power and minimum input voltage (10 kW & 30 V).

By measuring the power MOSFET switch-off current di/dt and using (39), we can estimate the total power MOSFET common source inductance, L_{CS}, in the converter prototype. The power MOSFET is an IRFP4368 in a TO-247AC package from International rectifier. Typical gate-source voltage as function of drain current can be found in the product data sheet [47].

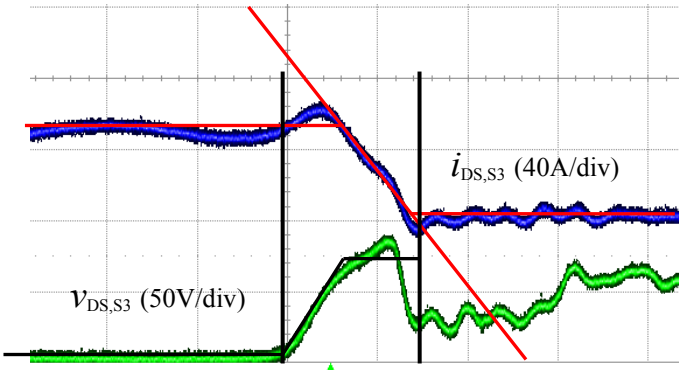

Fig. 18. Measured switch S3 turn-off sequence in 10 kW isolated boost converter. Time base is 100ns/div.

Measured turn-off di/dt in fig. 18, is

$$\frac{di_{S3}}{dt} = \frac{\Delta i_{DS,S3}}{\Delta t} \approx -0.67 \frac{A}{ns}. \tag{62}$$

Power MOSFET gate-source voltage at 48 A is typically: $V_{GS,IRFP4368}(48\ A) \approx 4.3\ V$ [47].

Using (39), we can then find an estimated value of the total power MOSFET common source inductance

$$L_{CS} \approx \frac{-V_{GS}(i_{S3})}{\frac{di_{S3}}{dt}} = 6.4\ nH \tag{63}$$

By using (47) and the straight-line approximated curve forms in fig. 18, the total commutation loss for all four parallel power stages is

$$P_{SW-10\,kW} = 8 f_s \int_{t_1}^{t_2} v_{S4} i_{T1}\, dt \approx 8 f_s \Delta v_{S4} \Delta i_{S4} \Delta t = 181\ W \tag{64}$$

Corresponding to a 1.8 % loss of efficiency at 10 kW output.

Note, since the commutation inductance will provide zero current turn-on (see chapter 3.4.4 below), the measured losses constitute the total converter switching losses.

Comparing the results from the two converters, there is a factor of 5 increase in relative losses between the two converters. The larger TO-247AC package utilized in the 10 kW converter has almost three times larger parasitic common source inductance. The much slower power MOSFET current turn-off speed in combination with the much higher current being switched, result in current commutation times - and thereby losses - that are five times larger in the 10 kW converter.

This comparative analysis of converter current switching performance clearly demonstrates the importance of achieving very fast current switching in high-power low-voltage applications. Further, it highlights a critical scaling problem, where larger parasitic inductances in larger power components, significantly contributes to deteriorating conversion efficiency as power levels are increased.

To reduce the effect of increasing parasitic common source inductance in high current power MOSFETs, semiconductor manufacturers could provide device packages with an additional source pin for gate drive purposes.

3.4.4 Switch Turn-on Losses

Zero voltage switching was developed in order to reduce capacitive losses during switch turn-on in high input voltage converters operating at high switching frequencies [49] and has since then been widely adopted in many such applications.

A repeated argument [2], [3], [27], [33], [35] is that high power converters for low input voltage also require zero voltage switching to achieve high conversion efficiency.

However, in [A2], [A6] we can see that even the exceptionally small commutation inductance realized in these converters is sufficient to delay current rise at switch turn-on such that zero current turn-on is created in the primary switches. The only remaining power loss during switch turn-on is therefore the capacitive discharge of the stored energy in the power MOSFET output capacitor.

To illustrate the insignificance of the capacitive turn-on losses, the capacitive turn-on losses of the 1.5 kW isolated boost converter presented in [A2] is calculated below.

Each of the 4 primary power MOSFETs (IRFB3077) are turned on once in each switching cycle of the fundamental switching frequency of 45 kHz. The drain-source voltage prior to turn-on is equal to the reflected output voltage seen on the transformer primary winding.

Total capacitive charge stored during switch turn-off and dissipated during device turn-on becomes:

$$P_{loss,turn-on} = 4 f_s E_C(V_{DS} = 50\ V) = 0.27\ W \tag{65}$$

Where the reflected output voltage is 50 V and the typical stored energy in the IRFB3077 power MOSFET output capacitor is $E_C(V_{DS}$=50 V$)$=1.5 µJ [47].

The total converter loss-of-efficiency due to primary switch turn-on is only 0.02% of maximum output power.

3.5 Circuit Design and Interconnections

Switch mode converters for high-power low-voltage applications, need to conduct very high dc- and ac currents while keeping conduction losses at a minimum. This requires components, circuits and interconnections that have extremely low resistances. Further, to be able to perform high frequency, high efficient switching of these high currents, we need to be able to change circuit currents very quickly.

Current switching speed of a circuit is fundamentally limited by the circuit parasitic inductance and given by

$$\frac{di}{dt} = \frac{v_L}{L_{Loop}} \tag{66}$$

Where v_L is the available circuit voltage i.e. the voltage driving the change of current, which in low voltage converters is naturally low and L_{Loop} is the total parasitic circuit inductance of that loop.

Since increasing the driving voltage will increase voltage stress on the switching semiconductors and thus dramatically increase their conduction losses, see chapter 3.4.1, it is apparent from (66) that the parasitic circuit inductance, L_{Loop}, is the only parameter by which we can increase the current switching speed.

In the following two chapters, we will analyze the impact of parasitic stray inductance and how to achieve low stray inductance in high current circuits.

3.5.1 Voltage Clamp Circuits

An isolated boost converter with a typical primary side clamp circuit to limit voltage spikes across primary switches during current commutation is presented in fig. 19. Diode, D3, capacitor, C_{CL}, and load, R_{CL}, act as a zener clamp across primary switches, S1-S4, during transistor switch-off.

In fig. 20, the equivalent circuit for the situation just after S4 has been switched off is presented. The intended operation being that parasitic stray inductance in clamp circuit, L_{CKT}, is much smaller than the transformer primary leakage inductance, $L_{LK,P}$, such that S4 drain-source voltage is essentially limited to clamp voltage, V_{CL}, while transformer current, i_{T1}, rises with the rate of

$$\frac{di_{T1}}{dt} = \frac{V_{CL} - {}^{V_o}/_{2n}}{L_{LK,P}}. \tag{67}$$

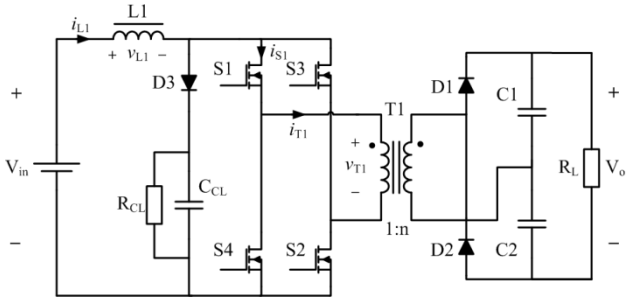

Fig. 19. Isolated full-bridge boost converter with primary side RCD clamp circuit.

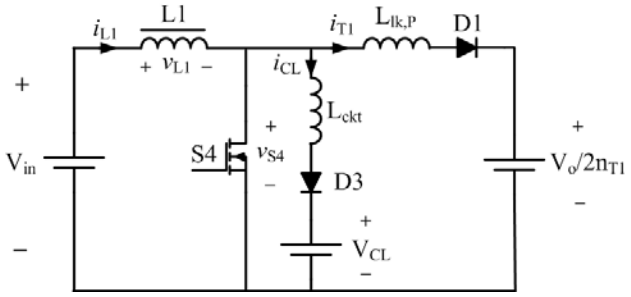

Fig. 20. Equivalent circuit of fig. 20, during switch S4 turn-off.

To limit rise time of transformer current, i_{T1}, and the associated clamp power, clamp voltage, V_{CL}, needs to be significantly larger than the reflected output voltage, $V_o/2n$. However, voltage rating of primary switches needs to be significantly higher than clamp voltage, V_{CL}, in order to allow clamp circuit to operate without reaching rated device voltage.

For primary clamp circuits to be effective, they must present significantly lower impedance at the clamping point than the circuit which is being clamped i.e. $L_{CKT} << L_{LK,P}$. This is easily achieved in high-voltage and/or low-power converters, where transformer leakage inductances are much higher.

In high-power low-voltage converters however, transformer leakage inductances are much smaller while clamp circuit stray inductances stay virtually unchanged as they depend on diode and capacitor terminal lead length and interconnecting wiring.

The result is clamp circuits that are only catching small fractions of the clamp energy. The major part being clamped by the converter output through the transformer. Furthermore, since the reflected output voltage on the transformer primary side is much lower than the clamp circuit voltage, V_{CL}, the transformer will present a lower voltage at the clamping point, leaving higher voltage across the transformer leakage inductance thus drawing the majority of the clamp current.

The extremely low transformer leakage inductance in high-power low-voltage converters thus renders primary side clamp circuits ineffective and superfluous.

Modern low voltage power MOSFETs are rated for repetitive avalanches and are very robust to unclamped inductive switching. Failure mechanisms are purely thermal and occurring at temperatures much in excess of rated junction temperature [47], [51]. Therefore, clamp circuits are not needed anymore for device protection.

3.5.2 Low Inductance and AC Resistance Interconnection

To achieve high conversion efficiency in ultra low impedance circuits, we need low ac resistive and low inductive interconnections capable of achieving fast current switching and conducting high ac currents without excessive losses.

Achieving low resistance levels obviously requires large copper cross sections, but the high ac frequency reduces current penetration depth, making copper thicknesses larger than one penetration depth useless. Thus, wide thin copper foil strips are the only way to achieve the required active copper cross sections.

The physical size of power components increases as a function of power level. Consequently, physical distance between these larger components will likewise increase, leading to increasing required wire length of the critical high-switching-current-interconnections. Thus, implementing low inductance layout is therefore vital in achieving fast and efficient high current switching.

To analyze ac resistance and stray inductance of interconnecting wiring, we can use the same methods and equations developed for the analysis of transformer ac resistance and leakage inductance in chapter 3.3.1 and 3.3.2.

The pair of foil strip interconnecting wires in fig. 21, can be seen as an uncoiled single-turn single-layer winding of a 1:1 turns ratio transformer with one intersection (M=1).

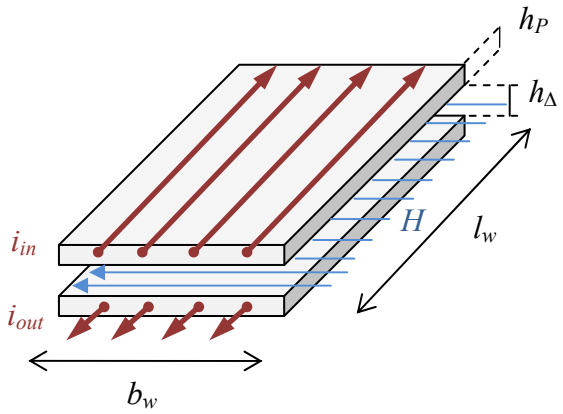

Fig. 21. Low inductance and low ac-resistance interconnection.

Ratio of ac to dc resistance due to eddy currents can be calculated using (12) from chapter 3.3.1.

$$F_R = \frac{R_{ac}}{R_{dc}} = \varphi \frac{sinh\, 2\varphi + sin\, 2\varphi}{cosh\, 2\varphi - cos\, 2\varphi}\,. \tag{12}$$

Where $\varphi = h/\delta$, since there is only penetration from one side corresponding to a single layer winding.

Similarly, we can use (21) from chapter 3.3.2 to estimate the stray inductance of the interconnection in fig. 22.

$$L_{LK} = \mu_0 \frac{N^2 l_w}{M^2 b_w}\left(\frac{1}{3}\sum_{P=1}^{2M} h_P + \sum_{\Delta=1}^{M} h_\Delta\right) \tag{21}$$

If *N=M=1,* and the conductor height represent the height of a transformer portion, $h = h_P$, the stray inductance of the interconnection wiring can be expressed by

$$L_S = \mu_0 \frac{l_w}{b_w}\left(\frac{2}{3}h + h_\Delta\right). \tag{68}$$

Where l_w, is the wire length, b_w is the wire width, h, is the copper foil thickness and h_Δ is the distance between the two conductors.

Since copper foil thickness exceeding the penetration depth will not contribute to the conduction of ac currents, we can only lower ac resistance by increasing the foil width, b_w, (which will also reduce the stray inductance). Also notice that stray inductance is proportional to distance between the two parallel foil conductors. The foil conductors should therefore be kept closely together in order to reduce parasitic inductance.

Similar to the principle of interleaving transformers windings to reduce ac resistance and leakage inductance, interleaved foil conductors could be used to achieve lower ac resistance and

stray inductance. The interconnection of the conductor layers at each end will, however, become quite complicated given the copper cross section needed.

A thin wire in free space will have an inductance of approximately 1.26 μH per meter. Alternatively, using (68), two copper foil strips of 30 mm width and 0.3 mm thickness which are spaced 0.1 mm apart, will have an inductance of only 12 nH pr. meter corresponding to a factor 100 decrease in stray inductance.

Wide copper foil conductors are therefore extremely efficient in achieving low ac resistance and low stray inductance in magnetic windings and interconnections as required to achieve high efficiency in high-power low-voltage converters.

3.6 High Voltage Silicon Carbide Schottky Diodes

High voltage rectifiers, as required in converters for high output voltage, are generally performing poorer in terms of switching speed and conduction losses than similar lower voltage devices.

In isolated boost converters, rectifying diodes are placed directly across output capacitors. Thus, output capacitors act as lossless voltage clamps, effectively limiting diode voltage stress to output voltage levels. In boost converters, rectifier diodes rated for 600 V will be sufficient for 400 V outputs.

In isolated buck type converters such as in the full-bridge converter fig. 8, required diode voltage rating is much higher. Even using full-bridge rectifiers, diodes in wide input voltage range converters (2:1) will be subjected to blocking voltages of at least twice the output voltage level. In addition to this, transient voltages caused by parasitic resonance will further increase voltage stress. Buck type converters therefore require rectifying diodes that are rated for at least 1200 V on a 400 V output. Alternatively, two outputs each using 600 V diodes can be series connected. In any case, rectifier cost and power loss will be substantially higher in buck type converters.

Silicon carbide (SiC) Schottky diodes are widely available in voltage rating up to 600 V and are also becoming available in 1200 V rating. Since SiC Schottky diodes do not suffer from reverse recovery, they can operate at much higher switching frequencies and be switched off much faster than traditional epitaxial PN diodes, while exhibiting much less switching losses.

The slightly higher forward voltage drop in SiC Schottky diodes compared to fast recovery PN junction diodes is more than compensated for by the fast and low loss turn-off behaviour resulting in overall lower converter losses.

3.6.1 Rectifier Conduction Losses

During conduction, diode voltage drop can be modelled by a fixed forward voltage drop, V_D, in series with a resistive element, R_D. Thus, diode conduction loss is given by

$$P_{D,con} = V_D I_{D,AV} + R_D I_{D,rms}^2 \tag{69}$$

In an isolated boost converter with voltage doubler output, the average diode current is

$$I_{D,AV} = I_o = \frac{P_o}{V_o} \tag{70}$$

And the corresponding diode rms current is

$$I_{D,rms} = \frac{I_{in}}{n}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L1}}{2I_{in}}\right)^2} \tag{71}$$

If $\Delta i_{L1} << I_{in}$, we have

$$I_{D,rms} \approx \frac{I_{in}}{n}\sqrt{1-D} \tag{72}$$

Total rectifier conduction loss in an isolated boost converter with voltage doubler (two diodes) thus becomes

$$P_{R,con} = 2\left[\frac{P_o}{V_o}V_D + R_D(1-D)\left(\frac{P_o}{\eta n V_{in}}\right)^2\right] \tag{73}$$

3.6.2 Rectifier Switching Losses

Switching losses in SiC Schottky diodes arise from the charging and discharging of the stored capacitive charge and is independent of the current slope [52].

In the 1.5 kW isolated boost converter presented in fig. 6, [A1]-[A2], the capacitive switching losses in the SiC output rectifiers can viewed as the charging and discharging of two (nonlinear) capacitors once every switching cycle. As the two diodes are in series and placed across the output, they share the same constant output voltage. Charging one diode thus automatically means discharging the other since the sum of their voltages is constant (=V_o). Charging and discharging these parasitic capacitors do not result in any power loss being dissipated in the diodes. Any switching losses associated with the charging and discharging of the capacitors are thus dissipated in the external circuits as a consequence of how this charging/discharging process is performed.

In the isolated boost converter (fig. 6), the charging and discharging of the parasitic output diode capacitors, are performed by the on/off switching action of the primary switches.

During the primary switch turn-off, the charging of parasitic capacitive elements such as MOSFET output capacitance and diode capacitance is performed inductively during the initial voltage switching part of the turn-off process. This charging process is a lossless transfer of charge to the parasitic capacitive elements.

Primary switch turn-on as described in chapter 3.4.4, is lossless apart from discharging of the stored energy in the internal parasitic MOSFET output capacitance. Current at turn-on is delayed due to the parasitic leakage and stray inductances such that MOSFET voltage can drop to zero before current increases thus creating zero current turn-on. However, the stored capacitive charge in the output diodes will be discharged in the form of a damped oscillating

current formed by the parasitic diode capacitance and the commutation inductance L_X. Thus the stored energy in the parasitic diode capacitance, will be dissipated as conduction losses in wiring, transformer windings and switch on-resistances.

Total capacitive switching losses in the rectifier output diodes (2 pcs.) are therefore

$$P_{D,sw} = 2f_s E_C(V_R) \tag{74}$$

Where $E_C(V_R)$, is the stored energy in the diode capacitance as a function of reverse voltage [52].

3.6.3 Analysis of Rectifier Losses in 1.5 kW Boost Converter

To illustrate the relative significance of these losses, the diode losses in the 1.5 kW isolated boost converter presented in [A1], [A2], is calculated.

The diodes used are 2 pcs. IDT10S60C, 600 V SiC Schottky diodes from Infineon.

Data for converter operating point is given in table IV.

TABLE IV.
1.5 KW BOOST CONVERTER WORST CASE OPERATING POINT DATA.

Parameter	Data
Switching frequency	45 kHz
Output power	1500 W
Output voltage	400 V
Input voltage	30 V
Transformer ratio	4
Duty cycle	70%
Converter efficiency	96.8%

The diode data obtained from the data sheet [52] are:

V_D=0.9V, R_D=0.065Ω and $E_C(400V)$=5.8 μJ

Using (73), total rectifier conduction losses are

$$P_{R,con} = 2\left[\frac{P_o}{V_o}V_D + R_D(1-D)\left(\frac{P_o}{\eta n V_{in}}\right)^2\right] = 13.3\ W \tag{75}$$

Using (74), total rectifier switching losses are

$$P_{R,sw} = 2f_s E_C(400\ V) = 0.52\ W \tag{76}$$

At maximum output power, the total rectifier switching losses constitute a loss of efficiency of only 0.03%.

Total calculated rectifier losses are

$$P_D = P_{D,con} + P_{D,sw} = 13.8\ W \tag{77}$$

Corresponding to a loss of efficiency of 0.92 % at maximum output power.

Measured diode switching waveforms can be seen in [A2].

3.7 Experimental results from 1.5 kW Boost Converter

To verify the theoretical results presented in this chapter and demonstrate the achievable conversion efficiency, a 1.5 kW isolated full-bridge boost converter was designed, built and tested. The results have been published in [A1] and in the invited journal paper [A2]. A very short summary of the achieved results is repeated here, but for full details please consult the attached appendix [A1]-[A3].

The converter is designed to fulfill the requirements in table I. The converter circuit is shown in fig. 6. The detailed design will not be repeated here, since data can be found in the published papers [A1]-[A3], and even further details have been given throughout chapter 3.

Measured converter waveforms are shown in fig. 22. Notice, although no snubber circuits have been used in the circuit, measured waveforms are very clean with only very limited spikes and ringings.

In fig. 23, measured converter efficiency is presented. To make sure that results are correct, very significant effort went into ensuring high precision of the efficiency measurement set-up. Measurement tolerances are less than +/- 0.1%. Measurements include gate driver losses. Maximum efficiency is 98% at 50 V input. In the worst case operating point at maximum power and minimum input voltage, efficiency is still 96.8%.

A photo of the prototype converter is presented in fig. 24.

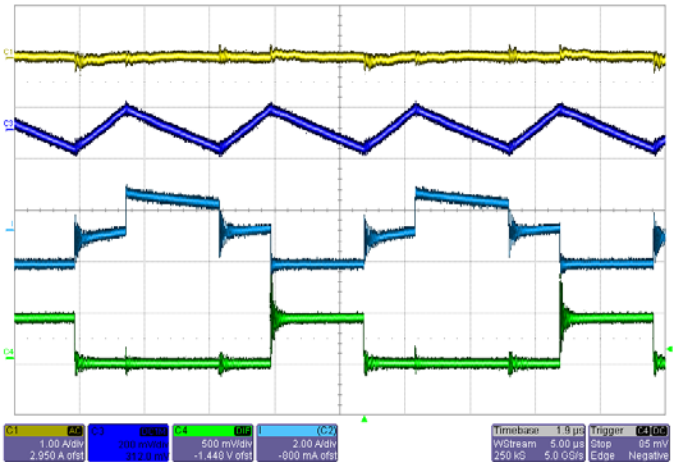

Fig. 22. Measured converter waveforms at 30V input and 1.5 kW output power. From top: Converter input ac-current $I_{in,ac}$ (1A/div), inductor L1, ac current (10A/div), switch S4 drain current (40A/div), and S4 drain-source voltage (50V/div). Time base is 5µs/div.

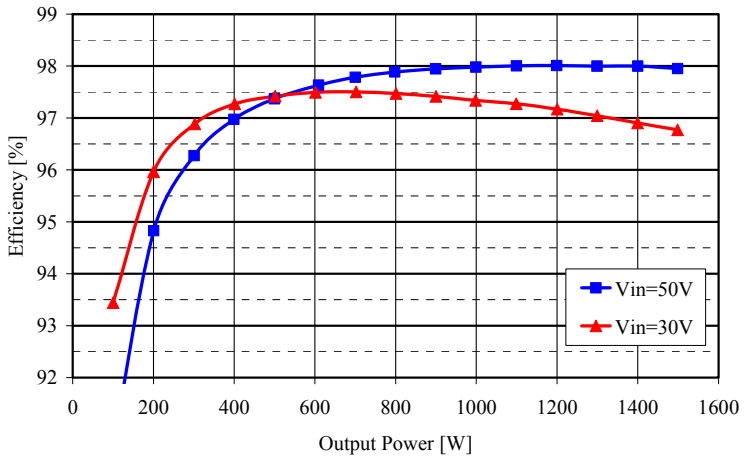

Fig. 23. Measured converter efficiency including drive power.

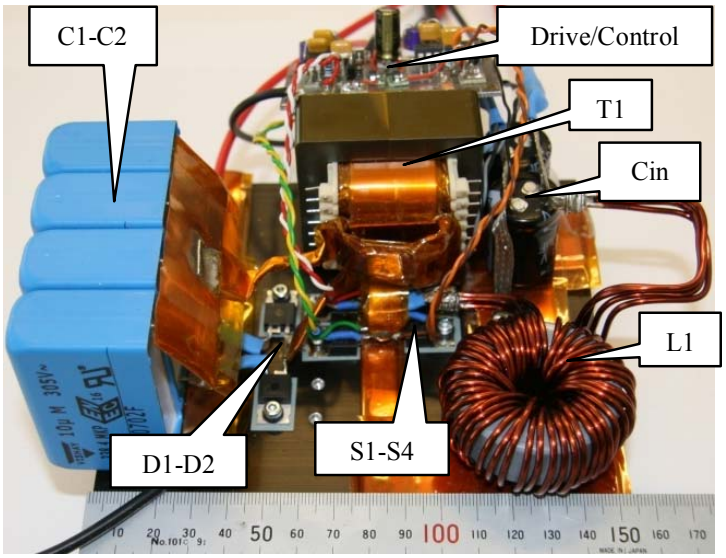

Fig. 24. Photo of 1.5 kW prototype isolated full-bridge boost converter.

3.8 Conclusion on Design of High-Current Converters

The following is a list of some of the conclusions that can be drawn from the analyses presented in this chapter.

- High-power low-voltage converters have extremely low input impedances, requiring extremely low impedance levels in circuits, components and interconnections to achieve high conversion efficiency.
- Extensive interleaving is needed to avoid proximity effect in transformer windings.
- Interleaving of windings and low number of primary turns provide extremely low transformer leakage inductance and stored leakage energy.
- Primary side switch voltage clamp circuits will be bypassed by the extremely low transformer leakage inductance and will thus not work.

- Power MOSFET losses are proportional to the product of device rms current squared and device voltage rating squared. To achieve high efficiency, this product must be minimized.
- Modern low voltage MOSFETs are rated for repetitive avalanche and do therefore no longer need voltage clamping circuits for device protection.
- Boost converters have lower switch rms currents than buck converters
- Minimum current switch-off losses in hard switched power MOSFETs are achieved when common source inductance are minimized to achieve fast current switching. If commutation inductance can be reduced to a level below the critical ratio for mode 2 current commutation, voltage clamp circuits cannot reduce switching losses any further.
- By eliminating voltage clamp circuits, power MOSFET voltage rating can be reduced by approximately a factor of 2, reducing primary switch conduction losses by more than a factor of 4. Thus, boost converter primary switches can achieve lower losses than buck converter switches.
- Voltage rating of boost converter rectifying diodes is less than half of the corresponding voltage rating of buck converter rectifying diodes. Furthermore, boost converters have inherently lossless clamping of rectifying diodes. Boost converters can therefore utilize lower voltage rating diodes and achieve higher rectification efficiency.
- Proper circuit layout is vital in achieving low circuit impedance and fast current switching. Thin wide foil type conductors in close proximity to return current path, will produce low stray inductive and low ac resistance interconnections.
- Boost converters can achieve both lower primary switch losses and lower rectifying losses and thus overall higher conversion efficiency in high power low voltage applications.
- Using these facts, very high conversion efficiency can be achieved. Test results from a 1.5 kW isolated full-bridge boost converter achieve maximum efficiency of 98%. In the worst case operating point at minimum input voltage and maximum output power, efficiency is still 96.8%.

The analysis and experimental verification presented in this chapter have therefore proved that the 4 widely accepted and adopted design hypothesis (or myths) identified in the state-of-the-art analysis are wrong.

4 Scalability of Converter

Following the analysis, design and demonstration of an ultra high efficiency single stage 1.5 kW converter in chapter 3, a second objective of this project is to analyze and suggest efficient and low cost methods to extend power level in the range of 1 to 10 kW.

With the aim of achieving the best possible scaling of the converter in terms of conversion efficiency per cost, this chapter will review alternative methods for extending power level of isolated boost converters.

A minimum paralleling approach is suggested in chapter 4.2. Fundamental limitations to converter scaling are reviewed in chapter 4.3.

4.1 Paralleling of Converters

One obvious method to scale power to higher levels is simply to parallel the required number of complete converter modules in order to reach the desired new power level. All input terminals and output terminals of all modules are directly paralleled. An additional control is required to balance power levels between paralleled modules (active current sharing, output voltage droop etc.).

This method, although being fairly simple, has the advantage of being very modular allowing reuse of existing designs, components, and will ideally mirror performance and relative cost of its basic modules. The method of paralleling complete modules has essentially unlimited power scaling potential in the sense that basically an unlimited number of power modules can be paralleled to reach an unlimited level of power.

The drawback of simple paralleling of power modules are, however, that potential benefits from scaling in terms of increased conversion efficiency, reduced size or cost per kilowatt etc. are lost, since these parameters are essentially fixed at the module level performance.

Other motivations for a direct paralleling of similar modules could, however, be to reduce development cost by reusing existing modules to satisfy lower quantity needs for higher power levels, achieving flexibility in power level (system growth potential) and/or achieving high reliability and maintainability by including extra spare modules.

4.1.1 Interleaving of Converters

Interleaving of converters is a special form of paralleling where clock phases of paralleled converters are phase shifted to achieve reduced input and/or output ripple [1]-[3], [11], [17], [30], [42].

The objective is to reduce the amount of ripple current or ripple voltage coming in- and/or out of paralleled converters. By de-phasing clock signals for each of the paralleled converter modules, fundamental frequency of input and output ripple are multiplied and absolute ripple magnitude is reduced rather than increased.

Significant ripple reduction can thus be achieved when paralleling converters already having high terminal ripple currents such as input ripple of buck type converters or output ripple of boost type converters. This saving can directly be translated into a reduction of input and/or output filter component size compared to non-interleaved converters.

4.1.2 Serial Connection of Inputs- and/or Outputs

Serial connection of either input- or outputs of paralleled converter modules is another special form of converter paralleling [1], [10], [17].

By series connecting multiple smaller voltage rated inputs (or outputs) on a high voltage input (or output), voltage stress on semiconductor devices can be reduced thereby allowing power electronic conversion at voltage levels much in excess of available semiconductor voltage ratings.

Series connecting full converters with internal voltage control will provide automatic current sharing since outputs (or inputs) are chained.

Series connecting at semiconductor level, however, requires careful attention to dynamic and steady state voltage sharing to avoid overstressing individual switches leading to catastrophic failures.

4.2 Minimum Paralleling Approach

In order to achieve the lowest cost and highest performance in terms of conversion efficiency, we will try to employ a minimum-paralleling-approach to scaling of high-power low-input-voltage converters.

The objective of the minimum-paralleling-approach is to obtain maximum economies-of-scale - in terms of improved ratio of conversion efficiency to cost - for a given output power. If inductors and diodes become more efficient and cheaper per watt of output power at higher output power, avoiding paralleling will create a more competitive product. Similarly, if a single control and protection circuit can control a larger converter, cost is saved.

The idea of the minimum-paralleling-approach is to limit paralleling to those few components or circuits where scaling of power level is either impossible due to lack of higher rated components, or scaling is fundamentally unfavorable, leading to lower conversion efficiency. The objective is thus to reach a minimum complexity by creating a partial paralleling solution where only critical high-stress-components are paralleled.

In chapter 3 and in [A3] it has been shown that isolated boost converters can achieve higher conversion efficiency than buck type topologies in high-power low-voltage applications. The starting point for the analysis is thus the 1.5 kW isolated full-bridge boost converter presented in [A1]-[A2]. Key parameters such as input voltage, output voltage, and switching frequency are kept constant in order to simplify comparison of results.

By sequentially analyzing each converter element for its ability to scale power level, the few critical high-stress-areas are identified. Once these components/areas and their limitation are

known, we can start to conceive solutions that exactly target this limitation without employing solutions/components to areas that are not yet scalability limited.

4.3 Scalability Limitations in Isolated Boost Converters

Each component of the isolated full-bridge boost converter in fig. 25, will be analyzed for its ability to be up-scaled without sacrificing conversion efficiency. The red marked area in fig. 25, symbolizes the high-ac-current-loop in the converter.

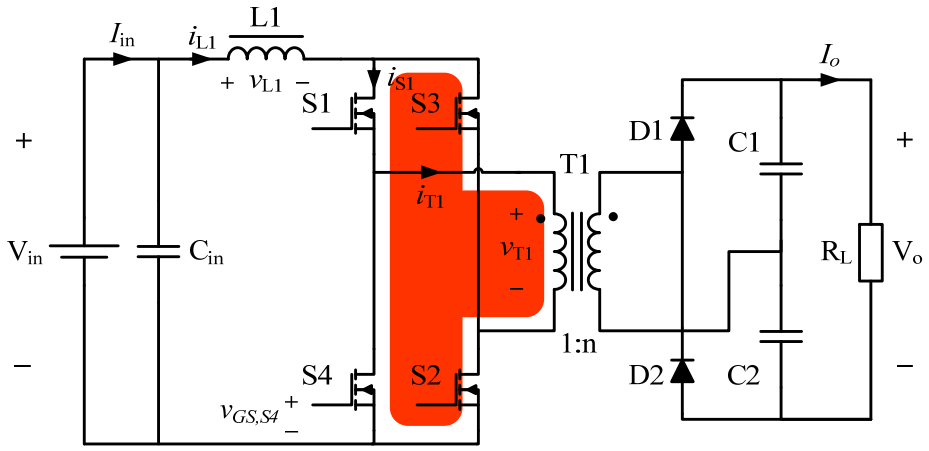

Fig. 25. Isolated full-bridge boost converter showing the critical high-ac-current-loop.

4.3.1 Input filter Scalability

The boost converter having the storage inductor, L1, in series with the input, inherently has very low input current ripple. Compared to buck converter topologies having large discontinuous input currents, the boost converter requires only very small additional input capacitance, C_{in}, for input ripple current attenuation. In terms of input capacitance, C_{in}, required, there is no converter scaling limitations in the power range of 1-10 kW.

The detailed consequences of scaling the storage inductor to a power level of 10 kW have been analyzed, tested, and presented in [A4]. Since the [A4] is already an integral part of this report, only a very brief summary of the conclusions will be included here.

At 10 kW output power and 30 V input, a storage inductor of 1.8 µH @ 345 A_{dc} will be needed at 45 kHz switching frequency. Inductor ripple frequency will be 90 kHz.

The 10 kW inductor is realized as 5 turns on a Magnetics Kool Mµ EE80 00K8020E40µ core. The winding window area allows each of the 5 turns to be 3.1 mm thick and 45 mm wide copper foil, providing a cross section of 140 mm^2, corresponding to a current density of 2.5 A/mm^2. Maximum dc winding loss will be 13.4 W.

Even though the ac current ripple is only approx. 67 A_{P-P}, and that flat foil windings are used, severe proximity effects will increase ac-resistance by a factor of 222 compared to winding dc-resistance. The large ac-resistance factor creates an ac winding loss of 9.3 W, thus almost doubling the winding losses. A larger inductor size will be required to allow this level of power dissipation.

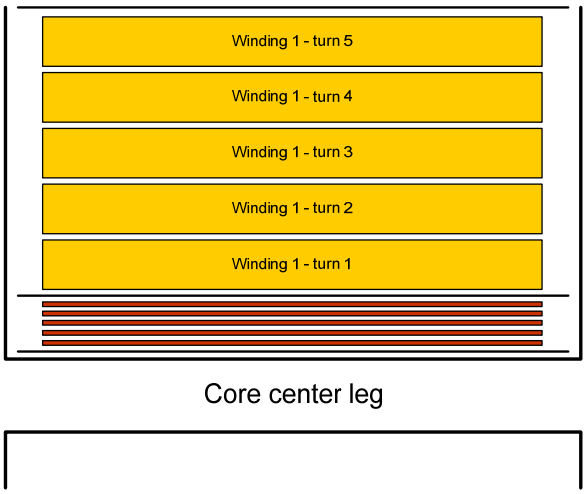

Fig. 26. Cross sectional view of 10 kW/345 A inductor winding.

A two winding solution is presented in fig. 26. A thin inner winding will mainly conduct ac ripple current, and a thick outer dc-winding will mainly conduct the large dc-current. Using this winding technique, ac-resistance is reduced by a factor of almost 7, whereas dc-resistance is not affected.

Worst case total winding loss in the two-winding 10 kW inductor is only 14.9 W corresponding to only 0.15 % loss of efficiency.

Using the proposed two-winding design for the converter storage inductor L1, even the storage inductor does not present any scalability limitations in the power range from 1-10 kW.

4.3.2 Scaling of Output Rectifiers

The output rectifier, consisting of the two SiC Schottky diodes D1-D2, and the voltage doubling capacitors C1-C2, is highly favoured by the high output voltage. However, as power levels increase, diode and capacitor currents in the simple voltage doubler configuration start to become a limiting factor.

At higher power level a full-bridge rectifier will be more appropriate. Transformer turns ratio will have to be doubled, reducing diode currents by a factor of two compared with the voltage doubler configuration. Four diodes of the same voltage and current rating (600 V, 10 A) will be able to handle twice the output power at the same efficiency. Also the ripple current in the output capacitor is greatly reduced and shifted to twice the switching frequency.

For grid tied systems beyond approximately 5 kW, it is likely that output voltage requirement would be increased to 7-800 V in order to allow interface to the three phase utility grid. Transformer turns ratio would have to be increased to 1:16 which would complicate transformer design and manufacturing. The rectifying diodes can still be scaled as 4 pcs. 1200 V/20 A SiC Schottky diodes will be able to handle 10 kW output power [A6].

In conclusion, by changing rectifier configuration to full-bridge rectifiers, current rating of diodes is reduced by a factor of two. Transformer turns ratio, however, has to be increased by a factor of two, slightly complicating transformer design and manufacturing. The high output

voltage and the change of rectifier configuration into full-bridge type allow the rectifier to be scaled in the power range from 1-10 kW.

4.3.3 Scaling of Primary Switches

The primary switches are definitively scalability limited in the power range of 1-10 kW. At a minimum input voltage of 30 V, maximum input current will reach 345 A at 10 kW output power. No single standard power MOSFET rated for 75 V can handle this current level today, so extensive paralleling of power MOSFETs is required to scale power level to 10 kW.

To determine the minimum number of parallel power MOSFETs required for a given application, we can use (28) to calculate the maximum allowable switch on-state resistance, $R_{S(on)}$, for a given acceptable primary switch loss-factor, κ.

$$R_{S(on)} = \frac{\kappa\left(\eta V_{in,min}\right)^2}{P_{o,max}(3-2D)} \tag{78}$$

The minimum number of parallel switches required is the integer number higher than

$$N_{SW,min} \geq \frac{R_{S(on)}}{R_{DS(on),max}} \tag{79}$$

Where $R_{DS(on),max}$, is the maximum operating on-state resistance of the power MOSFETs to be used i.e. on-resistance at maximum operating junction temperature.

Alternatively, we can use (78) to find the maximum power we can transfer in a full-bridge boost converter when using a specific power MOSFET and limiting switch conduction losses to a defined level.

For a 1% maximum conduction loss, 4 pcs. International Rectifier IRFB3077 power MOSFET with a typical on-state resistance of 3.5 mΩ at 60°C will be able to transfer

$$P_{o,max}(1\%) = \frac{0.01\left(\eta V_{in,min}\right)^2}{R_{DS(on),max}(3-2D)} = 1512\ W. \tag{80}$$

To scale a single power stage to 10 kW, each of the 4 primary switches would need at least 7 IRFB3077 power MOSFETs in parallel to keep conduction losses below 1% at maximum output power. To guarantee dynamic current sharing (also in avalanche) between 7 power MOSFETs in parallel and at the same time achieve fast current switching will be a very difficult task.

4.3.4 Transformer Scalability

From the analysis of the transformer winding ac-resistance in chapter 3.3.1, we can see that the height of any winding portion has to be limited to twice the penetration depth δ, that is

$$h_P \leq 2\delta \tag{81}$$

As presented in [A2], this limit has already lead to the need to interleave each primary winding between sections of secondary windings in the 1.5 kW isolated full-bridge boost converter presented in [A1]-[A2].

Increasing transformer power level further under the same operating conditions, will require proportionally higher level of winding interleaving in order to keep winding ac-resistance low.

Further, if core geometry is unchanged (but scaled with power), number of required primary turns will be reduced as power level is increased. One way to achieve the same maximum height of winding portions when having fewer primary turns and larger total winding height is to parallel multiple primary windings – each being interleaved between sections of secondary windings.

Although paralleling of multiple primary windings is possible, it will complicate transformer design even further.

4.3.5 Scaling of Interconnection Wiring

Power loss from ac-resistance as analyzed in chapter 3.3.1 is proportional to rms currents squared. Similarly, power losses from parasitic stray inductances as analyzed in chapter 3.4.3 is proportional to peak current squared. To keep the same relative losses and thus maintain efficiency, parasitic ac-resistances and stray inductances have to reduce inversely proportional to increases in power level.

$$R_{ac} \propto \frac{1}{P_o} \tag{82}$$

$$L_{stray} \propto \frac{1}{P_o} \tag{83}$$

However, as presented in chapter 3.5.2, useful thickness of single layer interconnections is limited by penetration depth of copper (0.34 mm @ 45 kHz). Larger copper cross section as required at higher current levels can only be achieved by using wider tracks or complicated interleaving of wiring.

Furthermore, since physical size of primary switches and power transformers increases as power level increases, the length and thus the ac-resistance and stray inductance of this critical interface increases even further.

Lowering ac-resistance and parasitic inductances of interfaces as power level increases therefore becomes increasingly difficult eventually leading to poor scaling and lower conversion efficiency.

High ac-current interfaces such as seen between primary switches and power transformers in high-power low-voltage converters thus constitute a critical area of poor scaling.

4.4 Summary/Conclusion on Scalability

To summarize, when trying to scale high input current converters to even higher power levels, we will be faced with increasing challenges in the following areas:

- Large numbers of Power MOSFETs have to be operated in parallel to scale power level to 10 kW. Dynamic current sharing between parallel power MOSFETs has to be guaranteed – also in avalanche mode – while still achieving very fast current switching.

- Transformer windings have to be paralleled in order to allow even higher levels of winding interleaving on fewer primary turns to keep ac-resistance low.

- Scaling of the critical high-ac-current-interface between primary switches and transformer windings is potentially very difficult to achieve. Parasitic ac resistances and stray inductances have to reduce inversely proportional to output power while size of components increases and conductor thickness is limited by penetration depth.

5 New Partial Paralleling Method

Inspired by the conclusions in chapter 4, a new converter concept for partial paralleling of multiple power stages in isolated boost converters is suggested [A5]-[A7].

Since the new converter concept has already been described in the patent application in appendix [A7], and in the two conference papers in appendix [A5] and [A6], only a short overview description will be included here. For further details readers are referred to the included publications.

The objective of the new concept is to achieve a minimum paralleling solution which exactly target and resolves the converter scalability limitations found in chapter 4. Added complexity is thus held at an absolute minimum while a simple, efficient and scalable solution is achieved.

The new partial parallel isolated boost converter is depicted in fig. 27.

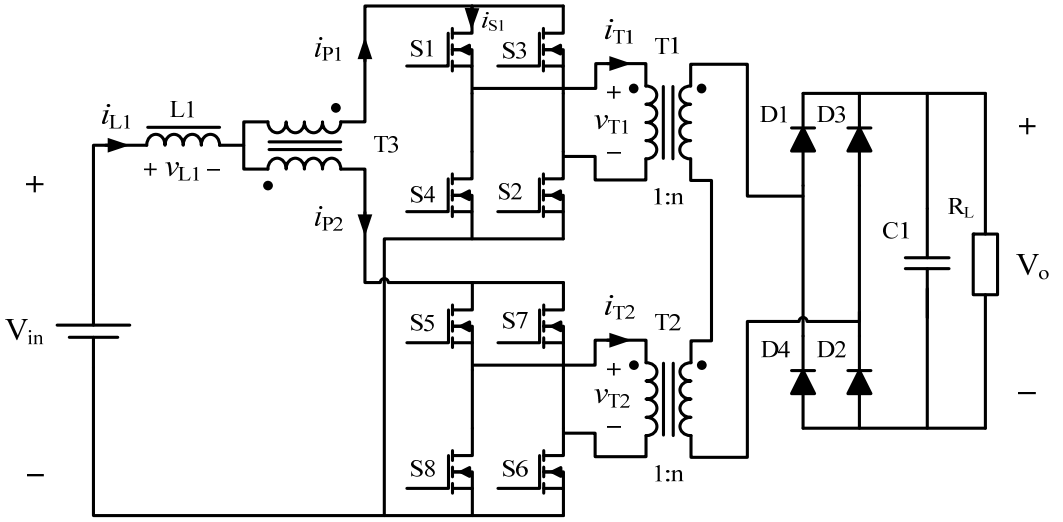

Fig. 27. Partial parallel isolated full-bridge boost converter.

Two primary side inverter bridges consisting of S1-S4 and S5-S8 respectively operate in-synchronism and in-phase utilizing the same control signals. Each inverter bridge supplies a power transformer.

Series connection of transformer secondary windings insures current sharing during energy transfer cycle when power is transferred to output. During inductor, L1, charging when all switches are turned on, a small current balancing transformer, T3, will maintain current sharing between the two parallel branches. Small volt-time product imbalances between the two power stages as caused by small differences in gate driver delays, power MOSFET switching speed, and/or parasitic circuit elements are absorbed by the current balancing transformer.

Balancing of the two primary currents, i_{P1} and i_{P2}, is required. Since any differences in currents developing during the inductor charging period will be clamped (and thus dissipated) in the primary switches having the highest primary current during the subsequent energy transfer period.

A single output rectifier with associated output capacitor is shared between the two power stages. Also the storage inductor on the input side can be shared. Since input ripple current is much smaller than in comparable buck type converters, a small input filter will be enough to completely attenuate input ripple current.

To achieve fast on/off switching and thus low switching losses, all power MOSFETs have individual gate-drivers circuits.

The new paralleling method splits the critical primary high-ac-current-loop into two smaller loops. Each of the new smaller loops only need to switch half of the input current thereby achieving much faster current switching and thus higher conversion efficiency.

Each of the two parallel power stages thus operates as if they were part of two individual single converters, each having a continuous feed of input current that exactly matches the current in the parallel branch such that no transient interaction between branches can occur. The circuit therefore has inherent current sharing and does not need any additional control to guarantee current balancing between power stages.

Since the two power transformers share input current and power level. Design and manufacturing of these transformers are significantly simplified. Furthermore, since transformer secondary windings are in series, required transformer turn ratio in each of the two transformers is reduced by a factor two, even further simplifying transformer design.

The ideal continuous steady state transfer function is

$$\frac{V_o}{V_{in}} = \frac{n}{1-D}. \tag{84}$$

The partial paralleling method can also be applied to all other isolated boost converters. As an example, the implementation of a partially paralleled two-inductor-boost converter is presented in fig. 28.

The two storage inductor currents i_{L1} and i_{L2}, are each split into two equal currents i_{L11}, i_{L12} and i_{L21}, i_{L22} for each of the two power stages consisting of switches S1, S2, T1 and S3, S4 and T2.

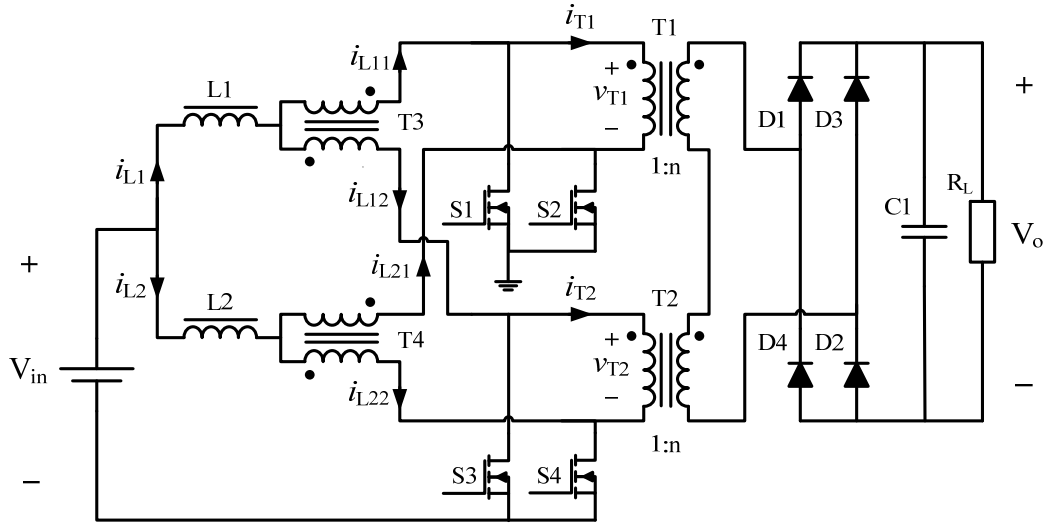

Fig. 28. Partial parallel isolated two-inductor boost converter.

Extension to higher number of paralleled converter stages is possible by adding an extra current balancing transformer for each extra paralleled power stage. For even numbers of paralleled power stages, the current transformer turns ratio should be 1:1. For odd numbers of paralleled power stages, one current transformer needs to have a turns ratio of 2:1, with the winding having the higher number of turns supplying the extra odd number power stage.

Inductor and current transformer configuration for a 3-paralleled power stage converter is shown in fig. 29. Fig. 30, show the configuration for a 4-paralleled power stage converter. In general, N-1 current balancing transformers are needed for paralleling N power stages.

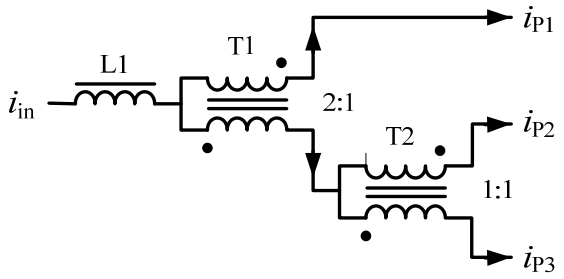

Fig. 29. Storage inductor and current balancing arrangement for a triple parallel isolated boost converter.

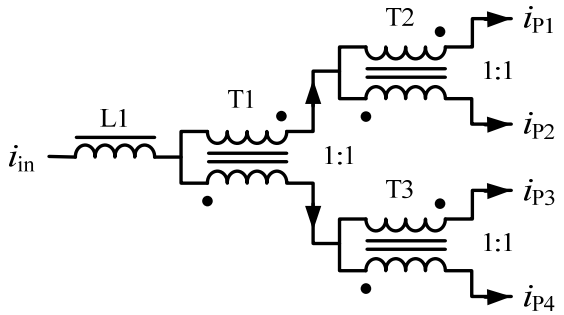

Fig. 30. Storage inductor and current balancing arrangement for a quad parallel isolated boost converter.

The advantages of the partial paralleling method are that

- A minimum amount of paralleling is utilized to achieve a very simple, low cost, safe and efficient parallel operation of multiple primary switching bridge-stages.
- Current switching losses are reduced by splitting primary side high-current ac-loops into multiple smaller loops with only fractional switching currents. Current switching losses are thereby significantly reduced.
- Small current balancing transformers in combination with serial connected transformer secondary windings, guarantee current sharing in all switch transistors. Selection and matching of switch transistors are therefore not required and avalanche operation can be utilized without risk of switch overstress.
- Transformer power level, primary current and turn ratios are reduced by the number of parallel power stages, thereby greatly simplifying transformer design and manufacturing.

5.1 New Partial Parallel 3 kW Isolated Boost Converter

To verify and demonstrate the feasibility and advantages of the new concept, a 3 kW isolated full-bridge boost converter with two parallel power stages was designed, built, tested, and published [A5]. Converter circuit is shown in fig. 27. The achieved results are briefly presented in the following.

To allow easy comparison with the single power stage 1.5 kW converter presented in [A1]-[A2], the exactly same type and design of the power components were used. The primary side power MOSFETs were same type from same batch, power transformer was exactly same design, and also the output rectifier SiC diodes were similar. All operating conditions such as input voltage range, output voltage, and switching frequency are also kept constant.

Measured waveforms of the two primary currents i_{P1} and i_{P2}, is presented in fig. 31. Notice that currents are completely alike. If the oscilloscope off-set between the two traces are removed, traces coincide completely.

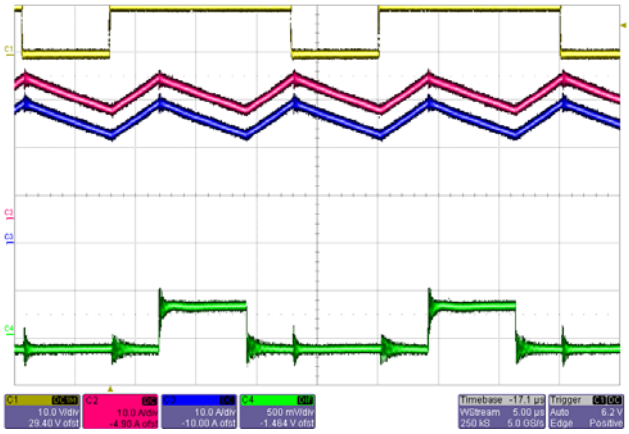

Fig. 31. Measured converter waveforms. From top: Drive signal for primary switches S1-S2 and S5-S6, primary current i_{P1} (10A/div), primary current i_{P2} (10A/div) and bottom trace is S4 drain-source voltage (50V/div). Time base is 5µs/div.

Measured converter efficiency is presented in fig. 32. Blue curve is measured at 50 V input and red curve is measured at 30 V input. Measurement tolerances are better than +/- 0.1%. Measurements include gate-driver losses.

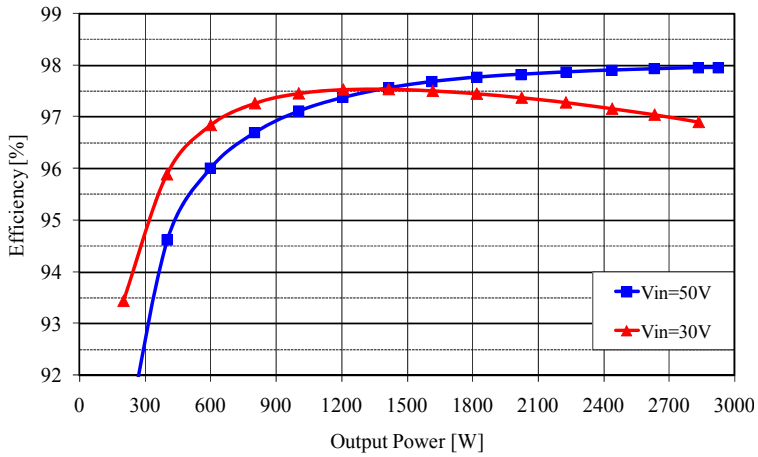

Fig. 32. Measured converter efficiency of 3 kW isolated boost converter with parallel power stages.

A photo of the current balancing transformer is presented in fig. 33, and fig. 34, is a photo of the 3 kW prototype converter. For further details, the reader is referred to appendix [A5].

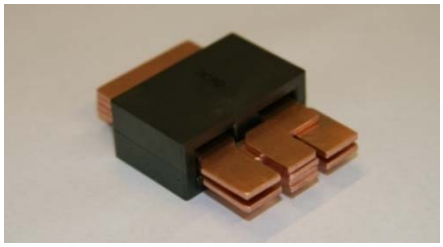

Fig. 33. Photo of current balancing transformer for 3 kW converter.

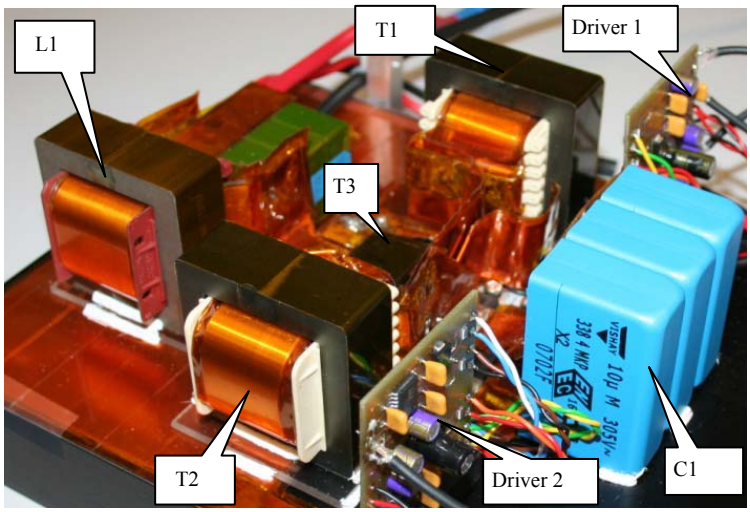

Fig. 34. Photo of 3 kW isolated boost converter with two parallel power stages.

5.2 New Partial Parallel 10 kW Isolated Boost Converter

The next step in the demonstration and verification of the new of concept was to design a quad partially parallel isolated boost converter for 10 kW [A6], thus achieving the maximum power range considered in the project. Fig. 35, is a diagram of the quad partially parallel isolated boost converter.

Considering the power level involved, it was decided to increase output voltage level to 7-800 V to allow interface to the three phase utility grid.

Four 2.5 kW power stages operate in parallel using the same control signals. Power MOSFETs are IRFP4368 from International Rectifier [47]. Rated on-resistance is 1.85 mΩ and transistor is packaged in a TO-247AC package.

For comparison, switching frequency is kept at 45 kHz. An EE65 ferrite core is used for each power transformer. Each transformer has two primary windings in parallel. Each primary winding is interleaved between sections of secondary windings. Due to the series connection of all secondary windings, the transformer turn ratio is only 1:4.

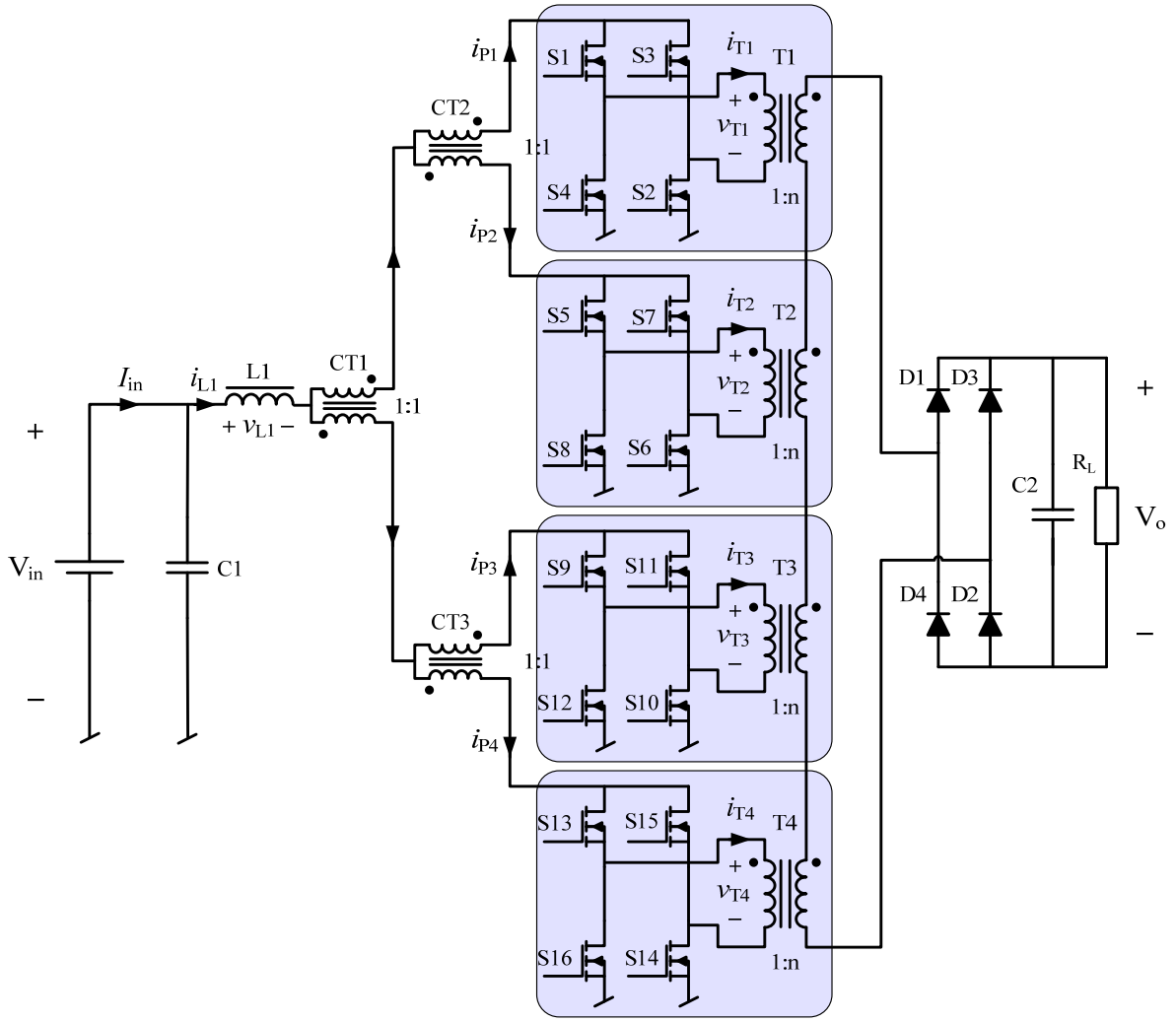

Fig. 35. Quad partial parallel isolated boost converter.

Detailed analysis and design of the common storage inductor, L1, is given in [A4].

The continuous steady state transfer function for the converter is

$$\frac{V_o}{V_{in}} = \frac{2n}{1-D}. \tag{85}$$

Measured converter curve forms are presented in fig. 36, and measured converter efficiency including gate drive losses are shown in fig. 37. Notice, that compared with the 3 kW converter in chapter 5.1, worst case efficiency at minimum input voltage and maximum output power is lower. The drop in efficiency is a consequence of slower current switching in the power MOSFETs as explained in chapter 3.4.3.5. Further, an effect of poor scaling of parasitic inductances in the critical primary side high-ac-current loop – as explained in chapter 3.5.2, is also seen. Regardless of these beginning signs of poor scalability, the converter achieves the highest measured efficiency at 50 V input.

A photo of the three integrated current balancing transformers is presented in fig. 38. The complete 10 kW prototype converter is shown in fig. 39. For further details, please consult the published papers in [A4] and [A6].

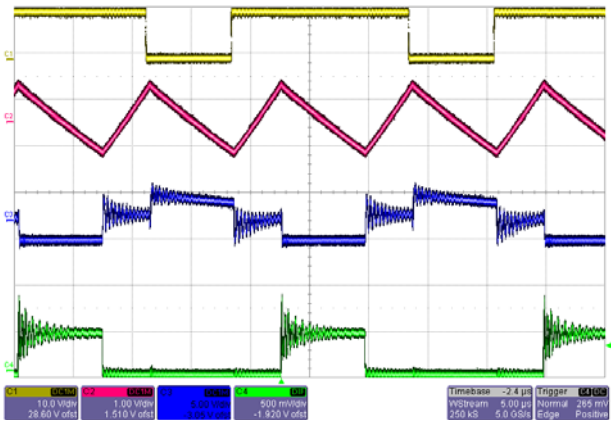

Fig. 36. Measured waveforms on a 10 kW quad partial parallel isolated boost converter. From top: switch drive signal, inductor L1 ac-current (50A/div), switch S3 current (100A/div) and switch S3 drain-source voltage (50V/div). Time base is 5 µs/div. Input voltage is 30 V and output power is 10 kW.

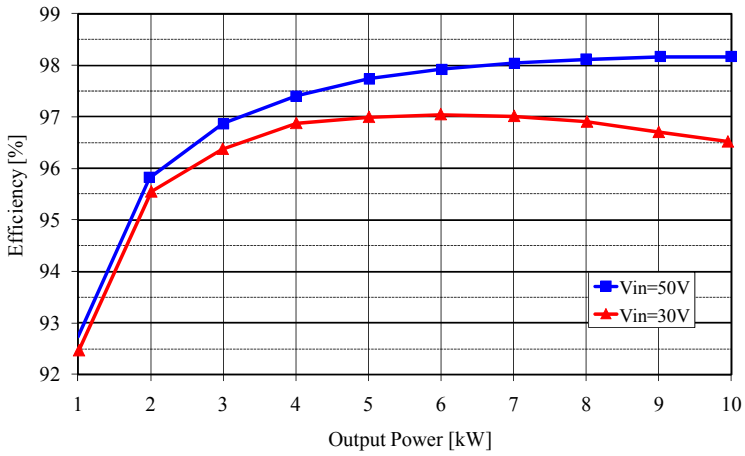

Fig. 37. Measured efficiency of 10 kW isolated boost converter.

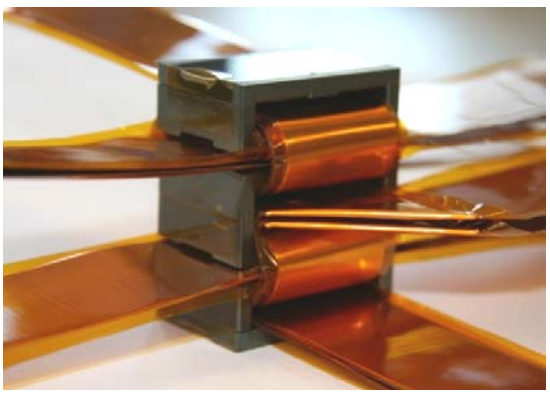

Fig. 38. Photo of 3 integrated current balancing transformers for 10 kW converter.

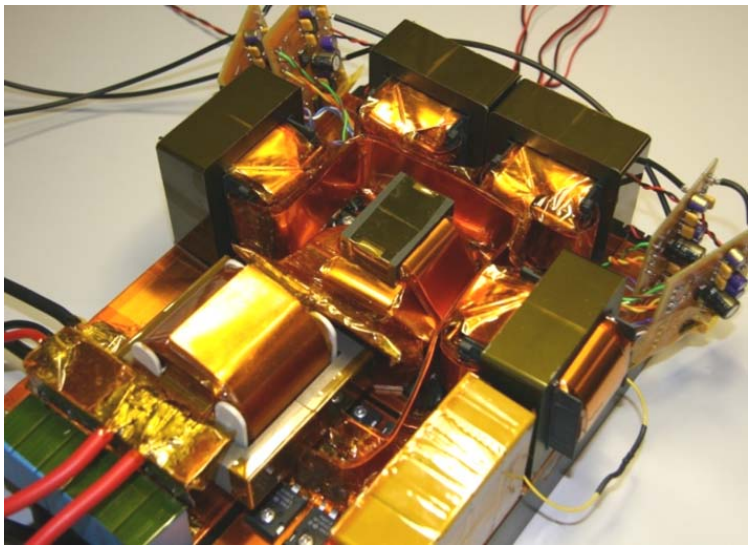

Fig. 39. Photo of 10 kW prototype converter.

5.3 Conclusion on Extending Power in 1-10 kW Range

A new method for extending power level of isolated boost converters has been presented.

- The critical high-ac-current-loop consisting of primary switches, power transformer, and interconnection, is effectively broken-up into several smaller loops with fractional currents. Much faster and thus more efficient current switching is obtained.

- Current sharing between all switches and stages is guaranteed by series connection of secondary windings and the use of small current balancing transformers on primary side.

- A simple common controller can control all power stages.

- Power transformer design is greatly simplified since power level, primary current, and turns ratio are reduced by the number of parallel power stages.

- Input filter, output filter, and rectifier are common to all power stages, thus achieving higher efficiency and lower cost.

- Test results from a dual parallel 3 kW converter and a quad 10 kW converter prototype have been presented. Very high conversion efficiency has been demonstrated.

A very simple and low cost yet very high performing converter topology is achieved.

6 Conclusion and Future Work

6.1 Summery and Conclusion

An extensive state-of-the-art analysis has been performed to create an overview of current results and techniques being used. The analysis revealed that:

- Many full-bridge buck and boost derived topologies have been proposed, but except for the V6 topology they all suffer from low conversion efficiency in the critical low input voltage maximum output power point. However, no published data for the V6 converter efficiency in regulated mode has been found.

- Boost type topologies and V6 topology are preferred due to their lower transformer turns ratio. As this was claimed to be a critical source of high transformer leakage inductance and thus low conversion efficiency.

- Boost type converters are generally designed using voltage clamp circuits or active clamp/reset circuits to limit primary switch over voltages during current commutation. Primary switch voltage rating is typically rated at three times the maximum input voltage when voltage clamp circuits are used. Active clamp circuits and reset circuits require additional switches and create high rms currents. In both cases leading to significantly increased conduction losses in primary switches.

In order to verify - or reject - these assumptions and to identify, if possible, the most efficient converter topology, a detailed analysis of power transformer design and power losses in low voltage high power applications was conducted. This analysis revealed that:

- High power and low input voltage create very low converter input impedance levels, requiring extraordinary low circuit impedances, in terms of ac resistance and parasitic stray inductances, to achieve high conversion efficiency.

- Large input current requires large conductor cross sectional areas in transformer primary windings. To avoid severe proximity effects, extensive interleaving of primary and secondary windings is needed.

- Contrary to the general understanding, very low transformer leakage inductances can be achieved. Due to the few primary turns, extremely low primary side leakage inductances can be achieved.

- Boost type topologies have inherently lower primary switch rms currents than comparable buck type topologies. For similar switch voltage rating, boost converters will thus have lower conduction losses in primary switches.

- Boost type converters have inherently lower peak reverse voltage on output rectifier diodes than comparable buck type converters. For similar input voltage range, buck converter rectifier diodes have twice as high peak reverse voltage as comparable boost type converters. Furthermore, boost rectifiers are naturally clamped to output voltage capacitors providing effective and lossless clamping of voltage spikes. Requiring much

lower voltage rating of rectifier diodes, boost converters have much lower rectification losses.

- The widely used voltage clamp circuits and techniques used to limit primary switch voltage spikes during current commutation in boost type converters require extensive (>2 times) over sizing of primary switch voltage rating to work. As power MOSFET conduction losses increase exponentially with device voltage rating, over sizing of switch voltage rating in boost converters leads to dramatically increased conduction losses and thus low conversion efficiency.

- If power transformers and circuit layout are optimized for high power low voltage applications, primary side voltage clamp circuits will be bypassed by the exceptionally low impedance and reflected voltage seen on power transformer primary side. Voltage clamp circuits will therefore not work in properly designed high power low voltage applications.

- Modern low voltage power MOSFETs are fully rated for operation under repetitive avalanche conditions. Failure modes are purely thermal and occurring at temperatures much in excess of maximum operating junction temperature. Voltage clamping circuits are therefore no longer needed for device protection.

- SiC Schottky diodes do not suffer from reverse recovery and thus allow very fast current turn-off without power losses being affected.

- Therefore, since stored leakage energy in power transformers for high power low voltage applications is exceptionally low, and over sizing of primary switch voltage rating leads to dramatically increased conduction losses, a very large efficiency improvement in isolated boost converters can be achieved by simply eliminating primary side clamping circuits and reducing voltage rating on primary switches.

- Even more, if the ratio of commutation inductance to common source inductance can be kept below a defined ratio, a minimum current commutation loss condition is reached where voltage clamp circuits no longer has any effect.

Having identified isolated full-bridge boost converters as being the most efficient converter topology for low voltage high power applications, the next objective of this study was to find the most efficient way - in terms of conversion efficiency and cost – to scale power level in the range of 1 kW to 10 kW.

Many suggestions for paralleling and interleaving of multiple converters have been proposed in literature. A significant drawback of paralleling is, however, that potential gains in efficiency and relative cost per watt are lost, since paralleling of complete power converters will fix cost and performance at module power level.

With the aim of suggesting a minimum paralleling solution in which only critical functions and circuits are paralleled, a study of potentially poor converter scalability was performed. The conclusions of this study are that:

- Boost converter input filter is not scalability limited in the power range 1-10 kW. Using a two winding technique to reduce inductor proximity effect, even the high current

storage inductor can be scaled and thus achieve even higher efficiency as power increases.

- Having high output voltage levels, ripple current levels on output can easily be managed in this power range.

- Also rectifier diodes can be scaled in this power range. In particular, since output voltage levels are likely to increase at higher power levels in order to interface to the three phase grid. In this aspect the boost converter has a huge advantage in the low rectifier voltage stress.

- However, the power MOSFETs in the primary switches quickly need to be paralleled. Although paralleling of multiple power MOSFETs in principle is possible, special precautions are required to ensure dynamic current sharing without loss of switching speed. Parameter screening and matching of power MOSFETs is one way of improving current sharing but at a higher cost. In avalanche mode, instantaneous power is high and current sharing becomes even more critical. Unfortunately, avalanche voltage levels can vary significantly between devices. Thus, current sharing cannot be guaranteed.

- Increasing power level in transformers for low voltage high power applications will require even more extensive interleaving of primary and secondary windings in order to control proximity effect. Although this is possible, winding complexity increases complicating design and manufacturing even more.

- Finally, scaling of the critical high ac-current interface between primary switches and transformer primary winding becomes very critical as current levels increases. To maintain efficiency, stray inductance and ac resistance of this interface have to scale inversely proportional to output power i.e. reduced by a factor of two for every doubling of output power. But as physical size of power components increases with power level, also distance between them invariably increases. Moreover, penetration depth in conductors effectively limits conductor thickness to one penetration depth requiring very complicated interleaved multilayer interconnections to maintain efficiency at higher power levels.

Based on the above results, the critical scalability limited area requiring duplication is identified as the high ac-current carrying loop from primary switches to power transformer primary winding.

A new method for partial paralleling isolated boost converters is proposed. Only the high ac-current carrying components i.e. primary switches and transformer are paralleled. Series connection of transformer secondary windings and small current balancing transformers ensure current sharing between parallel power stages. Parallel primary bridges operate in synchronism using the same control signal. The converter behaves and acts as if it was a single large converter, only requiring a single controller. Dynamic current sharing between all switches is guaranteed without sacrificing switching speed or requiring component screening, matching, or selection. The method can be applied to all isolated boost converter topologies.

Three isolated boost prototype converters covering the power range from 1.5 kW to 10 kW have been designed, built and tested to validate the theoretical analysis and demonstrate feasibility of the new paralleling method. All converters achieve maximum efficiencies of 98% or above and

worst case minimum efficiency at maximum output power and minimum input voltage are between 96.5 and 96.9 percent.

6.2 Future Work

Additional research and development effort is required to commercialize the suggested new paralleling principle.

A complete controller with start-up sequence, protection circuitry, voltage control, and/or current control as required by the specific application will need to be developed and demonstrated.

Since the power transformer requires extensive interleaving of primary and secondary windings, large capacitive coupling from input to output is inevitable. Study of common mode noise rejection and alternative approaches to achieve it will be a general need in high power low voltage converters.

Finally, bi-directional converters for high power low voltage applications are required in applications such as for recovering brake energy in electrical and hybrid electrical vehicles. The slow dynamics in fuel cell systems require large additional energy storage in order to isolate fuel cell from load transients and to supply output power during slow start-up and load transients.

One way to provide such extended low frequency filtering at converter output is to use a bi-directional dc-dc converter to charge and/or discharge energy from a storage energy bank realized by super capacitors. Developing a low cost high efficiency bi-directional converter, preferably utilizing the cost and efficiency advantages developed in this project will be a highly needed and attractive product.

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Appendix A

Appendix A is contains a list of publications made as part of this project i.e. conference papers, journal papers and patent applications.

A1. M. Nymand, M. A. E. Andersen, "A new approach to high efficiency in isolated boost converters for high-power low-voltage fuel cell applications," in *Proc. EPE-PEMC,* Poznan, Poland, 2008, pp. 127-131.

A2. M. Nymand, M. A. E. Andersen, "High-efficiency isolated boost dc-dc converter for high-power low-voltage fuel cell applications," *IEEE Trans. Ind. Electron.,* vol. 57, no. 2, pp. 505-514, Feb. 2010.

A3. M. Nymand, R. Tranberg, M. E. Madsen, U. K. Madawala, M. A. E. Andersen, "What is the best converter for low voltage fuel cell applications- A buck or boost?," in *Proc. IEEE IECON*, Porto, Portugal, 2009, pp. 959-964.

A4. M. Nymand, U. K. Madawala, M. A. E. Andersen, B. Carsten, O. S. Seiersen, "Reducing ac-winding losses in high-current high-power inductors," in *Proc. IEEE IECON*, Porto, Portugal, 2009, pp. 774-778.

A5. M. Nymand, M. A. E. Andersen, "New primary-parallel boost converter for high-power high-gain applications," in *Proc. IEEE APEC,* Washington, USA, 2009, pp. 35-39.

A6. M. Nymand, M. A. E. Andersen, "A new very-high-efficiency R4 converter for high-power fuel cell applications," in *Proc. PEDS*, Taipei, Taiwan, 2009*,* pp. 997-1001.

A7. M. Nymand, "Switch mode pulse width modulated dc-dc converter with multiple power transformers," WO/2009/012778, International Patent application PCT/DK2008/000274.

Appendix A1

M. Nymand, M. A. E. Andersen, "A new approach to high efficiency in isolated boost converters for high-power low-voltage fuel cell applications," in *Proc. EPE-PEMC,* Poznan, Poland, 2008, pp. 127-131.

A New Approach to High Efficiency in Isolated Boost Converters for High-Power Low-Voltage Fuel Cell Applications

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***Abstract*—A new low-leakage-inductance low-resistance design approach to low-voltage high-power isolated boost converters is presented. Very low levels of parasitic circuit inductances are achieved by optimizing transformer design and circuit lay-out. Primary side voltage clamp circuits can be eliminated by the use of power MOSFETs fully rated for repetitive avalanche. Voltage rating of primary switches can now be reduced, significantly reducing switch on-state losses. Finally, silicon carbide rectifying diodes allow fast diode turn-off, further reducing losses. Test results from a 1.5 kW full-bridge boost converter verify theoretical analysis and demonstrate very high efficiency. Worst case efficiency, at minimum input voltage maximum power, is 96.8 percent and maximum efficiency reaches 98 percent.**

***Keywords*—Switched-mode power supply, fuel cell system, efficiency, transformer, SiC-device.**

I. INTRODUCTION

High-power fuel cell or battery powered applications such as for transportation, forklift trucks or distributed generation, are often faced with the need for boosting the low input voltage (30-60V) to the much higher voltage (360-400V) required for interfacing to the utility grid fig. 1, [1].

For safety as well as for EMC reasons, galvanic isolation between source and utility grid is often desirable or required.

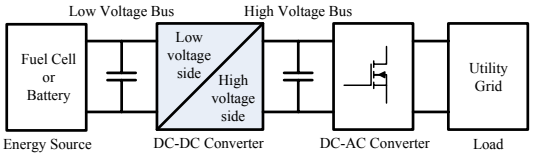

Fig.1. Fuel cell power system with isolated high gain DC-DC converter.

In particular fuel cells, exhibit significant output impedance reducing output voltage as output power is increased. System peak power is therefore reached at converter minimum input voltage. Drop in converter efficiency at minimum input voltage and maximum output power therefore directly reduces available system peak power. While the converter is required to operate over a wide input voltage range, typically up to a factor 1:2, high converter efficiency becomes particular important at minimum input voltage maximum power [1].

Isolated boost converters has some inherent advantages when used in fuel cell applications. With the storage inductor placed at the input side, ripple current is inherently low, only requiring limited extra filtering at the input side.

Output rectifying diodes are placed directly across output capacitors, ensuring minimum voltage stress and effective voltage clamping.

In a 400 V output application, 600 V rated diodes will be sufficient in boost type topologies, whereas buck type topologies would require 1200 V diodes or stacking of multiple outputs. Voltage stress on boost topology diodes are thus less than half of the corresponding voltage stress on a buck derived topology. Buck type topologies will therefore have significantly larger rectifying losses than boost type topologies.

The draw back of the boost type topologies is the need for clamping voltage spikes on primary switches caused by transformer leakage inductance and parasitic circuit inductances. Clamping is typically performed by some sort of voltage clamp circuit or by implementing active reset circuits [2-7]. This however requires significantly increased voltage rating on primary switches severely penalising conduction losses.

A large number of isolated boost converters for fuel cell applications have been presented, among these [2-7]. Ref. [2-4] have input voltage range and power level that are comparable to the converter presented in this paper. Ref. [5-7] are isolated bi-directional full-bridge boost converters intended for electrical vehicles. Input voltage is 12 V (8-15V), output voltage is typically 250-420 V and power range, in boost mode, is from 1.5 kW [5,6] to 3 kW [7].

Even though vastly different designs are represented (hard switched push-pull boost [2], actively clamped, two-inductor boost [3], bi-directional, actively clamped, two-inductor boost [4], and bi-directional soft switching full-bridge boost converters [5-7]), a general efficiency trend is clear. All converters achieve high efficiencies in the medium to high input voltage range, typically peaking at 94-96 percent at medium power. At low input voltage, high power, efficiency however reduces significantly to approx. 90 percent or below.

In this paper, the design of a simple, wide input voltage range, isolated full-bridge boost converter with very high efficiency at low input voltage is presented.

Test results from a 1.5 kW demonstration model achieve peak efficiency of 98 percent. Worst case

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efficiency at minimum input voltage and maximum power is 96.8 percent.

II. ISOLATED FULL-BRIDGE BOOST CONVERTER

The proposed full-bridge boost converter is presented in fig. 2. Timing diagrams and basic operating waveforms are presented in fig. 3.

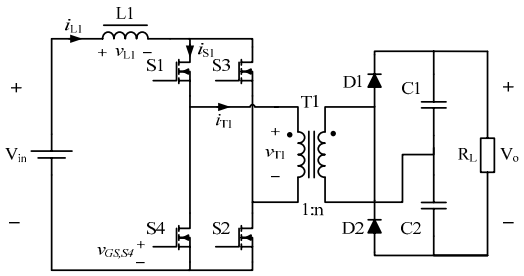

Fig.2. Isolated full-bridge boost converter with voltage doubling rectifier.

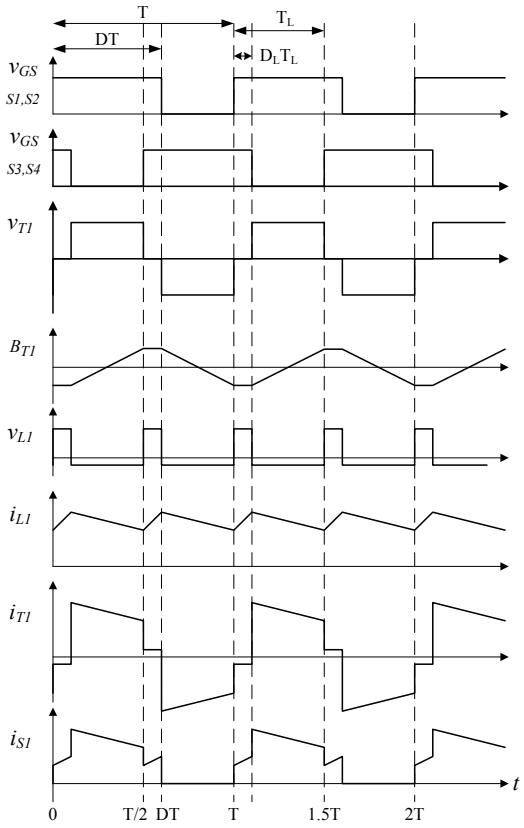

Fig.3. Basic operating waveforms of isolated full-bridge boost converter.

A. Basic converter operation

Primary switches S1-S4, are hard switched and operated in pairs S1-S2, and S3-S4, respectively. Drive signals are 180 degrees phase shifted. Switch transistor duty cycle D, is above 50 percent to ensure switch overlap and thus a continuous current path for the inductor L1, current.

Energy transfer to output starts when switches S3 and S4 are turned off. Inductor current i_{L1}, flows through primary switch S1, transformer T1, rectifier diode D1, output capacitor C1 and returns to input through primary switch S2. Inductor current i_{L1}, discharges. The period ends when primary switches S3 and S4 are turned on again.

During switch overlap, when all switches S1-S4, are turned on, inductor current $i_{L1,}$ is charged. Current in the transformer secondary winding is zero and diodes D1 & D2 are off. Transformer magnetizing current circulates in the transformer primary winding through switches S2-S4 and/or S1-S3. Capacitors C1, C2, supply the load current. The period ends when primary switches S1and S2 are turned off.

A second energy transfer cycle starts when switches S1 and S2, are turned off and ends when S1 and S2 are turned on again. Inductor current $i_{L1,}$ flows through switches S3, T1, D2, C2, and returns to input through S4.

Finally, a second inductor charging interval similar to the first follows.

The converter transfer function in continuous steady state is:

$$\frac{V_o}{V_{in}} = \frac{n}{1-D} \tag{1}$$

Where n=Ns/Np is the transformer turns ratio, and D is the switch duty cycle (0.5≤ D<1).

The corresponding inductor duty cycle D_L, and period time T_L, is defined as:

$$D_L \equiv 2D\text{-}1 \tag{2}$$

$$T_L \equiv {}^{T}/_{2} \tag{3}$$

Where $T=1/f_S$ is the period time for switches, diodes and the transformer.

III. CONVERTER DESIGN

The four primary switches S1-S4, are 75 V, 2.8 mΩ International Rectifier IRFB 3077 Power MOSFET which are fully repetitive avalanche rated [8]. The two rectifier diodes D1-D2, are 600 V Infineon IDT 10S60C SiC Schottky diodes. The inductor L1, core is a Magnetics Kool Mμ 77439. The transformer core is an EE55/21 ferrite core in 3F3 material. Switching frequency is 45 kHz.

Low current switching times increase efficiency since less charge is being diverted from output into primary side clamp circuits. Current switching times are limited by transformer leakage inductance and primary side stray inductances as well as MOSFET common source inductance whichever is worst case [9].

Transformer leakage inductance can be reduced by extensive interleaving of primary and secondary windings.

Careful primary side lay-out is required to reduce primary side stray inductances. MOSFET common source inductance is a function of package internal wiring (bonding wire length) as well as source external lead length [9].

B. Transformer design

The low input voltage, high power in fuel cell converters, causes high currents to flow in transformer primary windings requiring large copper cross sections in primary windings.

Foil windings are very efficient in providing large copper cross sections with a minimum conductor thickness. However, as power levels increases, even foil winding thicknesses quickly approach or exceed penetration depths in copper. Proximity effect can thereby cause very significant increases in winding AC resistances and thus lead to significantly increased power losses [10,11].

At 45 kHz, penetration depth in copper is only 0.34 mm. A primary winding with 4 turns on an EE55/21 core would allow up to approximately 0.6 mm cobber thickness for each of the 4 primary turns. Winding these 4 turns in a single 4 layer section, would increase AC resistance approximately 13 times compared to winding DC resistance ($F_R=R_{AC}/R_{DC}=13$) [10,11].

The more frequent case of a single interleaving (primary winding interleaved between two sections of secondary windings), increases AC resistance by a factor 3.5 compared to winding DC resistance.

To avoid severe proximity effect, penetration from both sides of each primary turn can be obtained by interleaving each primary turn between sections of secondary windings. The corresponding increase in AC resistance is now only 5 percent ($F_R=1.05$).

Keeping AC resistances low in high frequency high-current transformers therefore requires extensive interleaving of windings.

Since interleaving of windings also has the well known effect of reducing transformer leakage inductance [snelling], these transformers will not only have small AC resistances but also extremely low leakage inductances.

AC resistance and leakage inductance of the transformer used in a 1.5 kW isolated boost converter with a turn ratio of 4, are presented in fig. 4. Transferred to primary side, the AC resistance is only 1.9 mΩ and leakage inductance is only 11 nH. The leakage inductance in percent of primary inductance is only 0.01 percent.

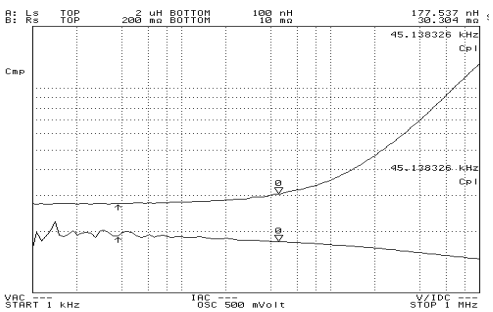

Fig.4. Measured secondary side AC resistance (upper curve) and leakage inductance (lower curve) of 1.5 kW transformer.

C. Primary switch voltage clamping

At low input voltage and high power levels, conduction losses in primary switches are a dominant loss factor. In the voltage range 60-200V, MOSFET on-resistance $R_{DS,ON,}$ typically increases quadratic with increasing drain-to-source breakdown voltage $V_{(BR)DSS}$. Voltage rating of primary switches therefore has very significant impact on converter conduction loss and thereby on converter efficiency.

To allow clamp circuits to clamp voltage spikes caused by transformer leakage inductance and circuit stray inductances, voltage rating of primary switches, in isolated boost converters, is typically rated at 2-3 times the maximum input voltage [6].

For primary clamp circuits to be effective, they need to present significantly lower impedance at the clamping point than the circuit which is being clamped. However, with the very low levels of transformer leakage inductances that are achieved in low voltage high power transformers, it becomes indeed very difficult for clamp circuits to present lower impedances than that of the transformer itself.

This result in clamp circuits only taking (small) fractions of the clamp energy, since the major part is being clamped by the transformer which even has lower reflected voltage and thus higher driving voltage across the leakage inductance.

Fortunately, due to the very low leakage inductance in the transformer, the leakage energy in the transformer is very small.

Some new low voltage power MOSFETs are rated for repetitive avalanche and are very robust to unclamped inductive switching [8,12].

With careful primary side lay-out and low leakage design of transformers, converter leakage energy is very small. Using avalanche rated MOSFETs, primary side clamp circuits can be eliminated and switch voltage rating reduced, significantly reducing MOSFET conduction losses.

Since silicon carbide Schottky diodes do not suffer from reverse recovery, they can work at much higher switching frequencies and in particular at much faster current switching speed (turn-off di/dt) without excessive losses.

IV. EXPERIMENTAL RESULTS

Experimental results from 1.5 kW demonstration model are presented in the following.

Fig. 4, is a plot of transformer leakage inductance and AC-resistance measured on secondary side. Transferred to primary side (dividing by transformer turns-ratio squared), the transformer leakage inductance is only 11 nH and the AC-resistance at 45 kHz is only 1.9 mΩ.

Fig. 5, is a plot of voltages and currents in the converter. Transformer current is measured on secondary side in order to avoid adding extensive stray inductance to the primary circuit.

Fig. 6, is an expanded view of fig. 5, showing that at turn off output current rise is only delayed approximately 30 ns from transistor voltage rise. Total avalanche loss, shared between 4 primary switches, can be estimated to:

$$P_{Aval,S1-S4} \approx i_{L1,peak} v_{S1,av} \Delta t f_s = 3.75\ W \qquad (4)$$

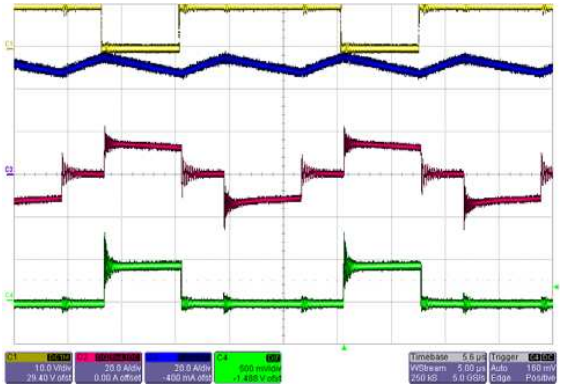

Fig.5. Measured converter waveforms at 30V input and 1.5 kW output power. From top: control signal for transistor S4, inductor L1 current (20A/div), transformer secondary current (20A/div) and bottom trace is transistor S4 drain-source voltage (50V/div). Time base is 5µs/div.

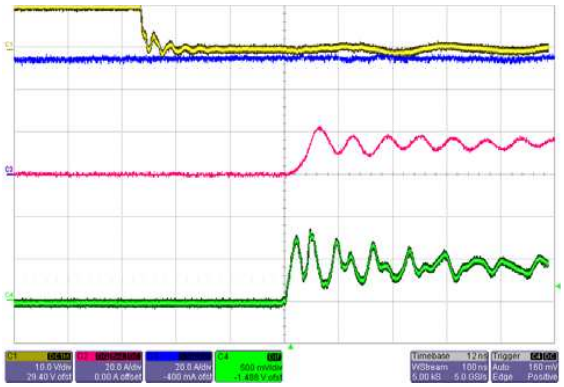

Fig. 6. Expanded view of fig. 5. Time base is 100ns/div.

D. Efficiency measurement

Measuring efficiencies in the 97-98 percent range are particularly critical and extensive care has been taken to ensure very high precision and stability of the efficiency test set-up.

In particular the current measurements are very critical. Measurements were made using 0.1 percent sense resistors with very high temperature stability (<10 ppm) mounted on heat sinks. Sense cables were shielded and supplied with common mode attenuating coils. Agilent 34410A high precision multimeters were used.

Since efficiency of single-input, single-output DC-DC converters is equal to the product of voltage ratio and current ratio (2), the critical current measurement ratio can be checked by simply passing the same current through both current sensors in series and verify that the measured voltage ratios correspond to the ratio of the sense resistor resistances.

$$\eta = \frac{V_o}{V_{in}} \frac{I_o}{I_{in}} \qquad (5)$$

Stability of test set-up was furthermore ensured by using high stability power sources and electronic loads. Converter heat sink temperature was measured and limited to 40 degree Celsius for repeatability of test.

The measured deviation of the sense resistor voltage ratio compared with the specified ratio (measured at 10 amperes) was less than 0.01 percent.

According to the specification of the Agilent 34410A, the output/input voltage ratio can be measured with a precision of better than +/- 0.012 percent.

The combined precision of the efficiency measurements are better than +/- 0.1 percent.

Measured converter efficiency, including transistor drive losses, is presented in fig. 7.

Maximum efficiency at low input voltage is 97.5 percent. Efficiency at full load is between 96.8 and 97.9 percent. Maximum efficiency is 98 percent.

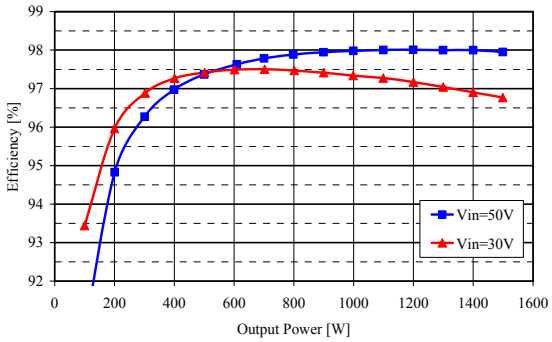

Fig. 7. Converter efficiency including drive power.

A detailed break down of converter power loss at minimum input voltage, maximum power (30 V/1.5 kW), is presented in table 1.

As would be expected, losses are dominated by conduction losses which constitute 83 percent of all calculated losses. Notice also that even though hard switching is used, switching losses are very small. Total inductive clamp losses are only 3.75 W corresponding to a quarter of a percent loss of efficiency.

Transformer efficiency is above 99.6 percent at maximum power.

TABLE I.
CONVERTER POWER LOSS BREAK DOWN AT 1.5 KW / 30 V

Component	Loss type	Loss [W]	Total [W]
MOSFET	Conductive	14.1	18.8
	Capacitive	0.27	
	Drive	0.72	
	Inductive clamp	3.75	
Diodes	Conductive	14.7	15.1
	Capacitive	0.41	
Transformer	Conductive	3.77	5.5
	Core	1.75	
Inductor	Conductive	5.2	6.2
	Core	1.0	
Other	Misc.		4.5
Converter	Measured efficiency		50.1

A photo of the 1.5 kW demonstration model is shown in fig. 8.

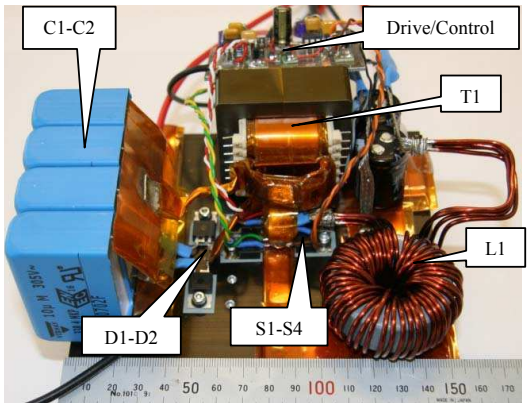

Fig. 7. Photo of 1.5 kW isolated full-bridge boost converter.

V. Conclusion

This paper, has presented a design approach to achieve very high efficiency in low-voltage, high-power, isolated boost converters. The design approach is demonstrated on an isolated full-bridge boost converter. Converter operation has been analysed and design details for a 1.5 kW converter has been presented.

Fast current switching is achieved by careful design of transformer and converter layout. Transformer proximity effect losses are reduced by extensive interleaving of primary and secondary windings. Test results on a 1.5 kW demonstration model confirm the achievement of fast current switching, low parasitic circuit inductance and very high efficiency.

Worst case efficiency, at maximum load and minimum input voltage, is 96.8 percent. Maximum efficiency is 98 percent.

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Appendix A2

M. Nymand, M. A. E. Andersen, "High-efficiency isolated boost dc-dc converter for high-power low-voltage fuel cell applications," *IEEE Trans. Ind. Electron.,* vol. 57, no. 2, pp. 505-514, Feb. 2010.

High-Efficiency Isolated Boost DC–DC Converter for High-Power Low-Voltage Fuel-Cell Applications

Morten Nymand, *Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—A new design approach achieving very high conversion efficiency in low-voltage high-power isolated boost dc–dc converters is presented. The transformer eddy-current and proximity effects are analyzed, demonstrating that an extensive interleaving of primary and secondary windings is needed to avoid high winding losses. The analysis of transformer leakage inductance reveals that extremely low leakage inductance can be achieved, allowing stored energy to be dissipated. Power MOSFETs fully rated for repetitive avalanches allow primary-side voltage clamp circuits to be eliminated. The oversizing of the primary-switch voltage rating can thus be avoided, significantly reducing switch-conduction losses. Finally, silicon carbide rectifying diodes allow fast diode turn-off, further reducing losses. Detailed test results from a 1.5-kW full-bridge boost dc–dc converter verify the theoretical analysis and demonstrate very high conversion efficiency. The efficiency at minimum input voltage and maximum power is 96.8%. The maximum efficiency of the proposed converter is 98%.**

***Index Terms*—DC–DC converter, fuel-cell system, high efficiency, switched-mode power supply, transformer.**

NOMENCLATURE

D	Switch duty cycle.
D_L	Inductor duty cycle.
f_S	Converter switching frequency.
T	Converter period time, $= 1/f_S$.
T_L	Inductor period time, $= T/2$.
n	Transformer turns ratio, $= N_S/N_P$.
F_R	AC resistance factor, $= R_{\rm ac}/R_{\rm dc}$.
$F_{R,P}$	AC resistance factor of primary winding.
$F_{R,S}$	AC resistance factor of secondary winding.
$F_{R,T}$	AC resistance factor of complete transformer.
h	Height of conductor.
h_P	Height of $P^{\rm th}$ winding portion.
h_Δ	Height of primary-secondary intersection.
h_w	Total height of transformer winding.
H	Magnetic field strength.
B	Flux density.
w	Stored energy in magnetic volume.
δ	Penetration depth in material.
p	Winding portion.
m	Number of layers in winding portion.
l_w	Mean turn length.
b_w	Breadth of winding.
M	Number of primary–secondary intersections.
N	Number of winding turns.
N_P	Number of primary turns.
N_S	Number of secondary turns.
μ_0	Permeability of free space.
$L_{\rm LK}$	Transformer leakage inductance.
$L_{\rm LK,P}$	Transformer leakage inductance referred to primary side.
$L_{\rm LK,S}$	Transformer leakage inductance referred to secondary side.

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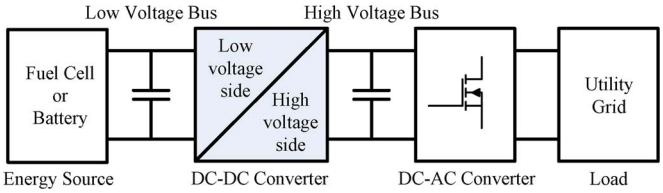

Fig. 1. Fuel-cell power system with isolated high-gain dc–dc converter.

I. INTRODUCTION

HIGH-POWER fuel-cell or battery-powered applications, such as for transportation, forklift trucks, or distributed generation, are often faced with the need for boosting the low input voltage (30–60 V) to the much higher link voltage (360–400 V) required for interfacing to the utility grid (Fig. 1), [1].

For safety and electromagnetic compatibility reasons, galvanic isolation between source and utility grid is often required.

High output impedance reduces fuel-cell output voltage at maximum output power. System peak power is therefore reached at converter minimum input voltage. A drop in converter efficiency at minimum input voltage and maximum output power therefore directly reduces the available system peak power. While the converter is required to operate over a wide input-voltage range, typically up to a factor of 1 : 2, high converter efficiency is particularly important at minimum input voltage and maximum power.

Isolated boost converters have some inherent advantages when used in fuel-cell applications. With the storage inductor placed at the input side, input ripple current is inherently low, requiring only limited additional decoupling at the input side.

Output rectifying diodes are placed directly across output capacitors, ensuring minimum voltage stress and effective voltage

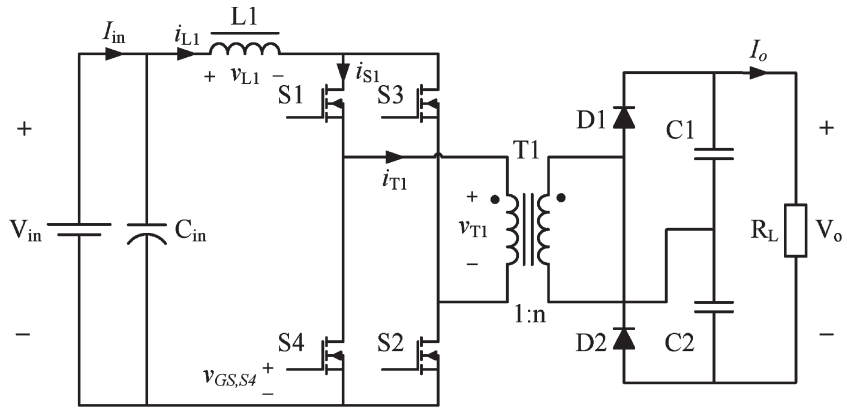

Fig. 2. Isolated full-bridge boost converter with voltage doubling rectifier.

clamping. In a 400-V output application, 600-V rated diodes will be sufficient in boost-type topologies.

As opposed to this, buck-derived topologies require 1200-V diodes or stacking of multiple outputs. Moreover, clamp circuits will be required across rectifier diodes in buck-derived topologies. Diode voltage stress in boost topologies are thus less than half of the corresponding voltage stress in buck-derived topologies. In high-voltage-output applications, buck-type topologies therefore have inherently larger rectifying losses than boost-type topologies.

The drawback of boost-type topologies is the need for the clamping of voltage spikes on primary switches caused by parasitic inductances, i.e., transformer leakage inductance and circuit stray inductances. Clamping is typically performed by voltage clamp circuits [2]–[4] requiring significantly increased primary-switch voltage rating (up to three times oversizing of voltage rating [5]), thus dramatically increasing switch-conduction losses. Alternatively, active clamping or reset circuits are used [4]–[10], requiring more switches and creating large triangular switch currents [4]–[7] with increased rms values. In [8]–[10], switch current is shaped by careful switch timing [8], [9] or resonance [10] in order to reduce switch-conduction losses.

A large number of isolated boost converters for fuel-cell applications have been presented, among these are [2]–[16]. References [2], [8], and [10]–[13] have voltage and power levels that are comparable with the converter presented in this paper. References [3]–[5], and [14] are isolated bidirectional full-bridge boost converters intended for electrical vehicles. Input voltage is 12 V (8–15 V), and output voltage is typically 250–420 V. Power range is from 1.5 kW [4], [5] to 3 kW [3] in boost mode. A 5-kW two-stage dc–dc converter solution is proposed in [15], and a current-fed converter with reduced output ripple current is presented in [16].

Although quite different designs are represented (hard-switched push–pull boost [2], bidirectional, actively clamped, two-inductor boost [8], actively clamped resonant push-pull [10], interleaved full-bridge boost [11], and resonant full-bridge boost [12]), there seems to be a general efficiency trend. Most converters achieve high efficiencies in the medium to high input-voltage range, typically peaking at 94%–96% at approximately half power. At minimum input voltage and maximum power, efficiency drops significantly to approximately 90% or below. The best performance is achieved by that in [10], which has an efficiency of 92.5% including dc–ac inverters.

In [17], the design of a simple wide-input-voltage-range isolated full-bridge boost converter with very high conversion efficiency was presented. This extended paper presents a detailed analysis of transformer ac resistance for four alternative transformer-winding designs. The analysis demonstrates that, to avoid severe proximity effect in high-power low-voltage transformers, an extensive interleaving of primary and secondary windings is required.

Furthermore, this paper presents a detailed analytical analysis of transformer leakage inductance. The analysis shows that stored energy in transformer leakage inductance does not depend on transformer turns ratio. Second, due to the few primary turns, primary-side leakage inductance is very small. Furthermore, the extensive interleaving of primary and secondary windings required to keep winding ac resistances low creates exceptionally low transformer leakage inductance.

Finally, analysis shows that the extremely low transformer primary-side leakage inductance and the low reflected output voltage will act as primary-switch voltage clamp circuit, effectively bypassing traditional clamp circuits.

Analytical results are verified by test results from a 1.5-kW prototype dc–dc converter. Transformer leakage inductance and ac resistance measurements confirm the extremely low leakage inductance. Detailed measurements of switch transistor, transformer, and diode voltage and current waveforms are presented. Finally, the measured prototype efficiency is presented. The worst case efficiency at minimum input voltage and maximum power is 96.8%. The maximum efficiency of the proposed converter is 98%.

II. Isolated Full-Bridge Boost Converter

The proposed full-bridge boost dc–dc converter is shown in Fig. 2. The timing diagrams and basic operating waveforms are shown in Fig. 3.

A. Basic Converter Operation

Primary switches $S1$–$S4$ are hard switched and operated in pairs, i.e., $S1$–$S2$ and $S3$–$S4$, respectively. The drive signals are 180° phase shifted. Switch-transistor duty cycle D is above

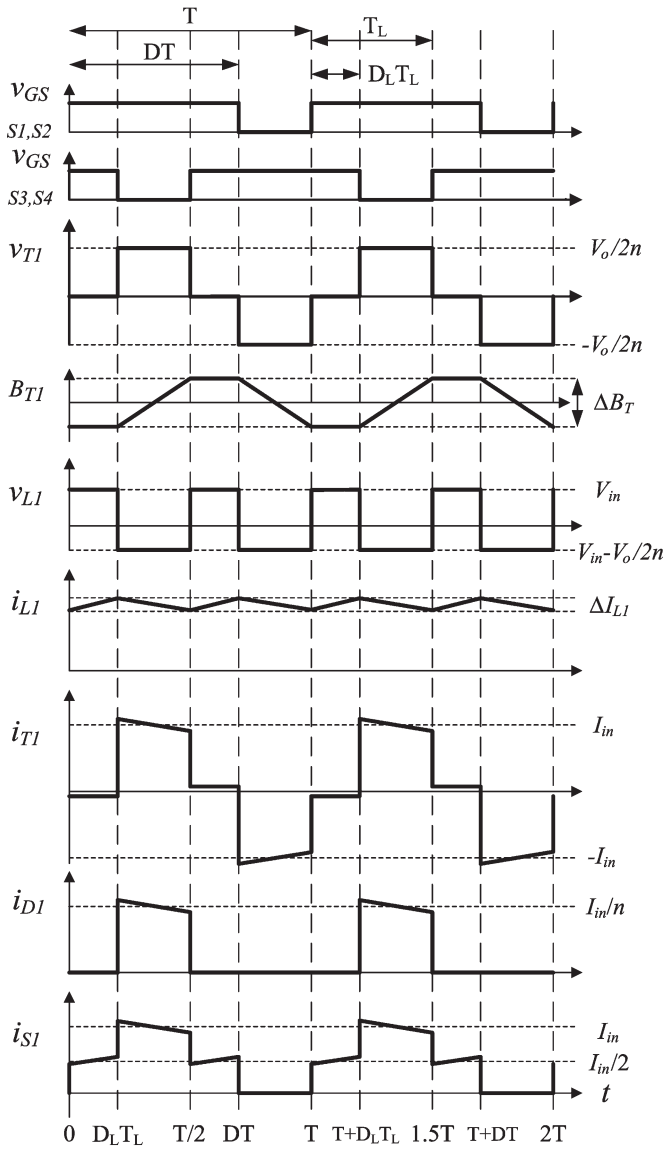

Fig. 3. Basic operating waveforms of isolated full-bridge boost converter.

50% to ensure switch overlap and, thus, a continuous current path for the inductor $L1$ current.

The energy transfer to output starts when switches $S3$ and $S4$ are turned off. Inductor current $i_{\rm L1}$ flows through primary switch $S1$, transformer $T1$, rectifier diode $D1$, and output capacitor $C1$ and returns to input through primary switch $S2$. Inductor current $i_{\rm L1}$ discharges. The period ends when primary switches $S3$ and $S4$ are turned on again.

During switch overlap, when all switches $S1$–$S4$ are turned on, the inductor current $i_{\rm L1}$ is charged. The current in the transformer secondary winding is zero, and diodes $D1$ and $D2$ are off. The transformer magnetizing current circulates in the transformer primary winding through switches $S2$–$S4$ and/or $S1$–$S3$. Capacitors $C1$ and $C2$ supply the load current. The period ends when primary switches $S1$ and $S2$ are turned off.

A second energy-transfer cycle starts when switches $S1$ and $S2$ are turned off and ends when $S1$ and $S2$ are turned on again. The inductor current $i_{\rm L1}$ flows through switches $S3$, $T1$, $D2$, and $C2$ and returns to input through $S4$.

TABLE I
CONVERTER SPECIFICATIONS

Parameter	Value	Comments
Output power $P_{\rm out}$	1500 W	
Input voltage range $V_{\rm in}$	30-50 VDC	Start-up voltage up to 60V
Output voltage $V_{\rm out}$	400 VDC	Galvanic isolation required
Efficiency target η	98 %	Converter efficiency to be optimized at low input voltage.
Output power regulation	0-100 %	For full control of input current transients
Input current ripple >10kHz	<15 %	For load range 15-100%
Input current slew rate	<3 A/s	Slow dynamics of fuel cell

Finally, a second inductor charging interval similar to the first follows.

The converter transfer function in continuous steady state is

$$\frac{V_o}{V_{\rm in}} = \frac{n}{1-D}. \tag{1}$$

The corresponding inductor duty cycle D_L and period time T_L is defined as

$$D_L \equiv 2D - 1 \tag{2}$$
$$T_L \equiv T/2. \tag{3}$$

III. CONVERTER DESIGN

The converter requirement specification is listed in Table I.

The four primary switches $S1$–$S4$ are 75-V 3.3-mΩ International Rectifier IRFB 3077 power MOSFETs which are fully rated for repetitive avalanches [18]. Rectifier diodes $D1$–$D2$ are 600-V Infineon IDT 10S60C SiC Schottky diodes. The inductor $L1$ core is a Magnetics Kool Mμ 77439. The transformer core is an EE55/21 ferrite core in 3F3 material. Switching frequency is 45 kHz.

Fast current-switching speed increases efficiency since less charge is being diverted from output into primary-side clamp circuits. Current-switching times are limited by transformer leakage inductance and primary-side stray inductances as well as MOSFET common source inductance whichever is worst case [19].

Transformer leakage inductance can be reduced by extensive interleaving of primary and secondary windings.

A careful primary-side layout is required to reduce primary-side stray inductances. MOSFET common source inductance is a function of package internal wiring (bonding wire length) as well as source external lead length [19].

A. Transformer AC Resistance

A transformer turns ratio of 1 : 4 is selected. At 45-kHz switching frequency, an EE55/21 ferrite E-core with four primary turns can transfer 1.5 kW at 30-V input. Sixteen secondary turns are thus required.

High input current in high-power fuel-cell converters requires a large copper cross-sectional area of transformer primary winding wires.

Foil windings are very efficient in providing large copper cross-sectional areas with a minimum conductor thickness. However, as power levels increase, even foil-winding thicknesses quickly approach or exceed penetration depths in copper. Proximity effect can thereby cause very significant increases in winding ac resistances, thus leading to significantly increased power losses [20], [21].

In principle, a Litz wire could be used. However, the very larger copper cross section and the few turns required on the transformer primary side make the use of a Litz wire difficult and impractical. Furthermore, due to the large number of individually insulated strands in Litz wires, the copper space factor is much lower than in solid copper foil windings, leading to increased dc resistance.

At 45 kHz, penetration depth in copper is only 0.34 mm. A primary winding with four turns on an EE55/21 core allows each of the four primary turns to be up to 0.6 mm thick. The 16-turn secondary winding can be realized by a 0.15-mm copper foil.

To illustrate the importance of controlling eddy-current- and proximity-effect losses, the works performed by Dowell [20] and Hurley *et al.* [22] are used to analyze the winding ac resistance of four alternative winding configurations, as shown in Fig. 4(a)–(d).

The increase in ac resistance $R_{\rm ac}$, compared with dc resistance $R_{\rm dc}$ at a specific frequency, i.e., with sinusoidal excitation, due to the eddy-current effect is

$$F_R = \frac{R_{\rm ac}}{R_{\rm dc}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi + \cos 2\varphi}. \tag{4}$$

For single-layer windings, $\varphi = h/\delta$, and for half-layer windings, $\varphi = h/2\delta$.

In multilayer windings $(m > 1)$, an additional term covering the proximity effect is added; thus, the resistance factor becomes

$$F_R = \frac{R_{\rm ac}}{R_{\rm dc}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi - \cos 2\varphi} + \frac{2(m^2-1)}{3} \varphi \frac{\sinh \varphi - \sin \varphi}{\cosh \varphi + cos\varphi} \tag{5}$$

where $\varphi = h/\delta$.

Since turn numbers and winding thickness are different on primary and secondary windings $(n \neq 1)$, ac resistance factors have to be calculated for both primary $F_{\rm R,P}$ and secondary $F_{\rm R,S}$ windings. The combined effective ac resistance for the transformer can be found as the weighted sum of the primary and secondary factors. If primary and secondary windings occupy equal winding spaces, the weighting factor becomes 0.5

$$F_{\rm R,T} = \frac{F_{\rm R,P} + F_{\rm R,S}}{2}. \tag{6}$$

Using (4)–(6), the transformer-winding ac resistance factors for the four alternative winding configurations in Fig. 4(a)–(d) are calculated and presented in Table II. Notice that the primary-winding ac resistance of the winding configuration in Fig. 4(a) is 13 times higher than that in the winding configuration in Fig. 4(d).

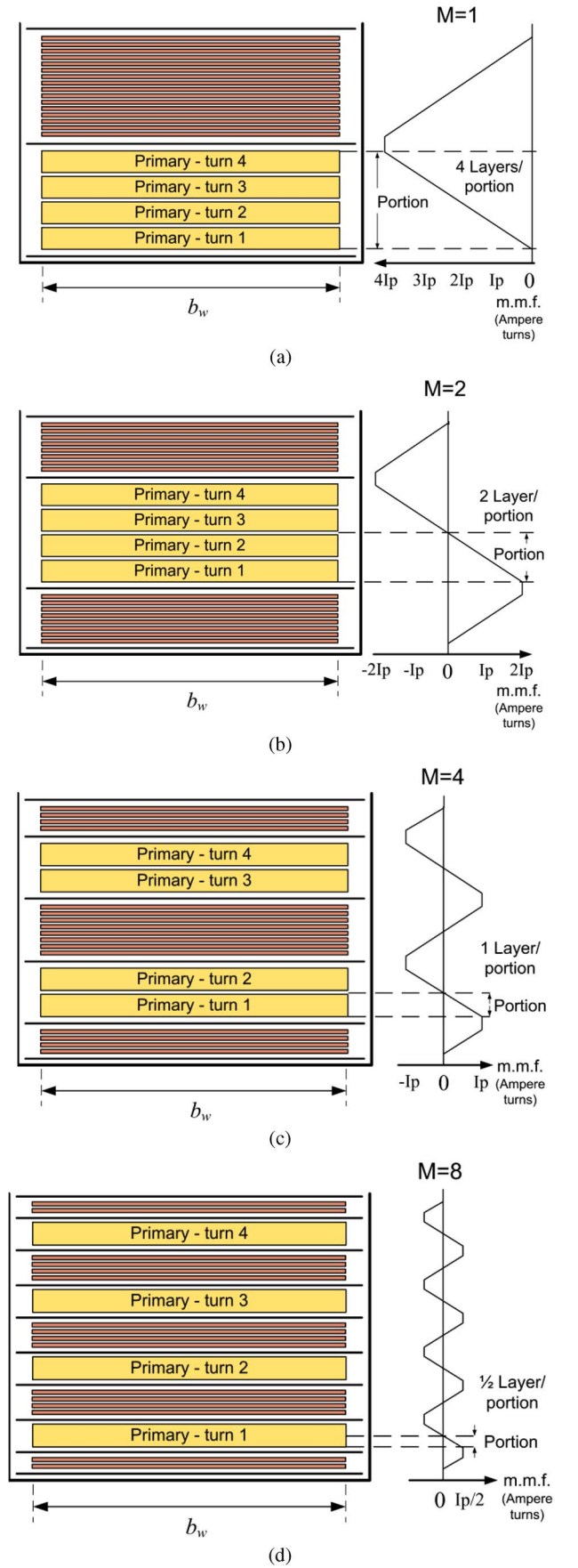

Fig. 4. Alternative transformer-winding configurations. (a) Without interleaving, (b) single interleaving, (c) double interleaving, and (d) quadruple interleaving.

TABLE II
CALCULATED AC RESISTANCE FACTOR AND TRANSFORMER LEAKAGE INDUCTANCE FOR FOUR ALTERNATIVE WINDING DESIGNS

Winding design	A	B	C	D
Intersections M	1	2	4	8
$F_{R,P}$	13.3	3.96	1.63	1.05
$F_{R,S}$	2.07	1.27	1.07	1.02
$F_{R,T}$	7.7	2.6	1.35	1.04
$L_{LK,P}$ [nH]	249	70	21	7.2
$L_{LK,S}$ [nH]	3,976	1,114	339	115

Keeping ac resistance low in high-frequency high-current transformers therefore requires an extensive interleaving of primary and secondary windings.

B. Transformer Leakage Inductance

Again, using the works of Dowell [20] and Snelling [21], an analytical expression of the transformer low-frequency leakage inductance can be derived. This analytical expression is very useful in fully understanding the impact of the transformer turns ratio and winding technique on transformer leakage inductance.

The stored energy in a magnetic volume V_e is

$$w = V_e \int_0^{\Delta B} H dB \tag{7}$$

where the flux density of free space is $B = \mu_0 H$.

The transformer winding can be grouped into a number of winding portions and intersections according to their magnetomotive-force diagram, as shown in Fig. 4(a)–(d). Winding intersections constitute small volumes $V_\Delta = l_w b_w h_\Delta$ of constantly high magnetic field strength H. Portions are volumes $V_P = l_w b_w h_P$ of winding space where magnetic field strength H is increasing linearly from zero to maximum.

To find the stored energy in each volume element, we integrate the squared magnetic field strength H^2 over the height of the volume element

$$w(V_P) = \frac{1}{2}\mu_0 l_w b_w \int_0^{h_P} H(x)^2 dx. \tag{8}$$

Knowing the shape of the magnetic field strength, as shown in each of the winding configuration drawings in Fig. 4, we can calculate the stored energy.

In each portion of the winding, the magnetic field strength H will either be increasing or decreasing, having the numerical magnitude

$$|H(x)| = \frac{NI}{Mb_w h_P} x. \tag{9}$$

Moreover, the corresponding magnetic field strength in the intersection between the primary and secondary windings is

$$|H(h_\Delta)| = \frac{NI}{Mb_w}. \tag{10}$$

Due to symmetry, we only need to calculate the values for one portion and one intersection and then multiply by the number of portions and intersections, respectively

$$w = \frac{1}{2}\mu_0 l_w b_w \left[\sum_{P=1}^{2M} \int_0^{h_P} \left(\frac{NIx}{Mb_w h_P} \right)^2 dx + \sum_{\Delta=1}^{M} \left(\frac{NI}{Mb_w} \right)^2 h_\Delta \right]$$

$$w = \frac{1}{2}\mu_0 l_w \frac{N^2 I^2}{M^2 b_w} \left(\frac{1}{3} \sum_{P=1}^{2M} h_P + \sum_{\Delta=1}^{M} h_\Delta \right). \tag{11}$$

By definition

$$w \equiv \frac{1}{2} L I^2. \tag{12}$$

Now, we can find an analytical expression for the leakage inductance L_{LK}

$$L_{\mathrm{LK}} = \mu_0 \frac{N^2 l_w}{M^2 b_w} \left(\frac{1}{3} \sum_{P=1}^{2M} h_P + \sum_{\Delta=1}^{M} h_\Delta \right). \tag{13}$$

If $h_\Delta \ll h_P$, transformer leakage inductance is approximately

$$L_{\mathrm{LK}} \approx \mu_0 \frac{l_w h_w}{3 b_w} \frac{N^2}{M^2}. \tag{14}$$

From (13) and (14), it is clear that the extensive interleaving of primary and secondary windings, as required in high-power low-voltage transformers, will lead to very small stored energy in transformer leakage inductance. Furthermore, it becomes clear that, with leakage inductance being proportional to the squared number of turns N^2, the few primary turns of low-voltage high-power transformers have inherently extremely small leakage inductance.

Using (13), the leakage inductances for the four alternative winding configurations in Fig. 4(a)–(d) are calculated and presented in Table II. Notice that the leakage inductance of the winding configuration in Fig. 4(d) is approximately 35 times smaller than that of the winding configuration in Fig. 4(a).

Furthermore, the analysis does not include any stray inductance effects of transformer termination leads.

In summary, the need to reduce the proximity effect in high-power low-voltage transformers requires an extensive interleaving of windings, which, at the same time, significantly reduces the transformer leakage inductance and, consequently, the stored energy in the transformer leakage inductance.

C. Primary-Switch Voltage Clamping

At low input voltage and high power levels, the conduction loss in primary switches is a dominant loss factor.

Slow current switching caused by high circuit inductances is another significant loss factor in high-power low-voltage applications. The slow current-switching speed creates extended voltage and current overlap time in primary switches during switching transitions, thus being responsible for increased switching losses.

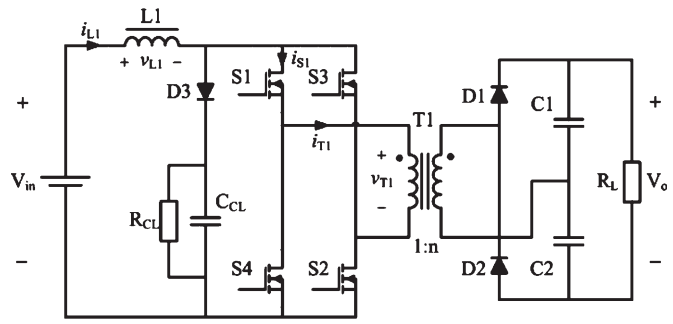

Fig. 5. Isolated full-bridge boost converter with primary-side voltage clamp circuit.

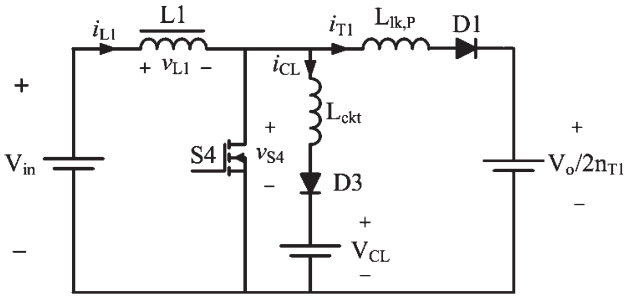

Fig. 6. Equivalent circuit of Fig. 5 during switch $S4$ turn-off.

In the voltage range of 60–200 V, the MOSFET on-resistance $R_{\mathrm{DS,ON}}$ typically increases proportional to the square of the rated drain-to-source breakdown voltage $V_{(\mathrm{BR})\mathrm{DSS}}$. The voltage rating of primary switches therefore has very significant impact on converter conduction loss and, thereby, on converter efficiency.

To allow clamp circuits to clamp voltage spikes caused by the transformer leakage inductance and circuit stray inductances, the voltage rating of primary switches, in isolated boost converters, is typically rated at two to three times the maximum input voltage [5].

An isolated boost converter with a typical voltage clamp circuit is shown in Fig. 5. Diode $D3$, capacitor C_{CL}, and load R_{CL} act as a Zener clamp across primary switches $S1$–$S4$, during transistor switch-off.

In Fig. 6, the equivalent circuit for the situation just after $S4$ has been switched off is shown. The intended operation is that the parasitic stray inductance in the clamp circuit L_{CKT} is much smaller than the transformer primary leakage inductance $L_{\mathrm{LK,P}}$, such that the $S4$ drain–source voltage is essentially limited to clamp voltage V_{CL} while the transformer current i_{T1} rises with the rate of

$$\frac{di_{T1}}{dt} = \frac{V_{\mathrm{CL}} - V_o/2n}{L_{\mathrm{LK,P}}}. \tag{15}$$

To limit the rise time of the transformer current i_{T1} and the associated clamp power, the clamp voltage V_{CL} needs to be significantly larger than the reflected output voltage $V_o/2n$. However, the voltage rating of primary switches needs to be significantly higher than the clamp voltage V_{CL} in order to allow the clamp circuit to operate without reaching the rated device voltage.

For primary clamp circuits to be effective, they must present a significantly lower impedance at the clamping point than the circuit which is being clamped, i.e., $L_{\mathrm{CKT}} \ll L_{\mathrm{LK,P}}$. This is easily achieved in high-voltage and/or low-power converters, where transformer leakage inductances are much higher.

In high-power low-voltage converters, however, transformer leakage inductances are much smaller while clamp-circuit stray inductances stay virtually unchanged as they depend on the diode and capacitor terminal lead length and interconnecting wiring.

The result is clamp circuits that are only catching (small) fractions of the clamp energy, with the major part being clamped by the converter output through the transformer. Furthermore, since the reflected output voltage on the transformer primary side is much lower than the clamp circuit voltage V_{CL}, the transformer will present a lower voltage at the clamping point, leaving a higher voltage across the circuit leakage inductance and thus drawing the majority of the clamp current. The extremely low transformer leakage inductance in high-power low-voltage converters thus renders primary-side clamp circuits ineffective and superfluous.

Modern low-voltage power MOSFETs are rated for repetitive avalanches and are very robust to unclamped inductive switching. The failure mechanism is purely thermal and occurring at temperatures much in excess of the rated junction temperature [18], [23]. Therefore, clamp circuits are no longer needed for device protection.

Silicon carbide Schottky diodes do not suffer from reverse recovery. Consequently, they can work at much higher switching frequencies and allow much faster current-switching speed (turn-off di/dt) without excessive losses.

D. Converter Start-Up

In boost converters, special considerations have to be given to the control of converter inrush current at start-up and handling of possible overload situations. It is well known that boost converters cannot control the output current when the output voltage drops below the input voltage. Similarly, isolated boost converters cannot control the current when the reflected output voltage drops below the converter input voltage. Unlike the nonisolated boost converters, isolated boost converters can be disconnected from an overload by simply turning all primary switches off.

Several techniques for limiting inrush current in isolated boost converters during start-up exist.

1) An active inrush limiter by means of a current limiter or a parallel combination of a charging resistor and a bypass switch can be placed in series with the input.
2) Similarly, an active current limiter can be placed at the output between the first small ripple filter and the main energy storage capacitor bank.
3) If overload protection is not required, the active current limiter can simply be placed in series with the main energy-storage capacitor bank on the output.
4) A small auxiliary start-up converter can be placed in parallel with the main converter for the charging of the output capacitors prior to main converter start-up.
5) An auxiliary flyback winding with the associated rectifier diode can be added on the boost-converter storage

inductor and connected to either output [24] [scheme 2)], [25] or input [26].

6) Finally, the output capacitor can also be charged by a series of narrow pulses in "buck mode," as described in [24] [scheme 1)].

The optimum solution heavily depends on specific application requirements, such as the amount of inrush current that can be accepted, whether output is loaded during start-up and whether output current limitation is required. For the fuel-cell applications envisaged in this paper, the dc–dc converter will be followed by a buck-type voltage-source dc–ac inverter, as in Fig. 1. The buck-type dc–ac inverter can thus protect the output from overload and disconnect the external load during start-up. During start-up, the converter is thus only loaded by a (large) intermediate bus capacitor bank.

Due to the high input current seen on the primary side, any series switches or active current-limiting circuits on the primary side are highly undesirable since they will dramatically reduce converter efficiency as well as increase the cost and size of the converter.

Current-limiter circuits on the output side are also an option but will add significant cost and complexity to the converter. Moreover, the separate start-up converter solution can be used and even potentially be combined with other desirable functions.

The use of an extra flyback winding on the input inductor is yet another option. However, the flyback winding will complicate the inductor manufacturing and reduce the available copper winding area for the main winding, thereby increasing inductor losses. More importantly, the voltage rating of primary switches will have to be increased substantially to allow clamping to input or output during start-up. As the on-resistance of power MOSFETs increases exponentially with the device voltage rating, the increased voltage rating of primary switches will dramatically increase conduction losses and thus significantly reduce converter efficiency.

Although, as explained previously, most of the solutions listed here can be used for reducing inrush current during start-up, the preferred solution is the method of "pumping" the converter during the charging of the output capacitors [24]. A series of short and low duty-cycle pulses $(D \ll 0.5)$ are fed alternately to a set of diagonal primary switches. A short and low-magnitude triangular current will be fed to the output during each switch-conduction cycle. When the switches are turned off, the (small) stored energy in the input inductor is clamped by the primary switches. This start-up method can charge the output voltage until it reaches the reflected input-voltage level $(V_o = 2nV_{\rm in})$, at which point, the converter will be started in normal operating mode $(D > 50\%)$. When the output capacitors are fully charged, the following dc–ac inverter will be allowed to start. The advantages of this method are the simplicity, requiring very little extra circuits, and the fact that converter efficiency is not affected.

E. Converter Control

As seen from the fuel-cell system having slow dynamics of hydrogen- and oxygen-supply systems, the ideal load profile will be that of a low-bandwidth controlled current sink. Converter control should therefore try to emulate a constant current-generator function. This function can be obtained by an input-current controller with a low-bandwidth outer feedback loop from the output voltage. Sufficient energy storage at the converter output will be needed to limit output-voltage transients during load changes and transients.

This control has several advantages. First of all, it will optimally allow the fuel-cell control system to control and track electrical load. Second, the traditional negative converter input impedance, caused by the constant power behavior of output controlled converters, is eliminated. Thus, any risk of negative impedance oscillations caused by high fuel-cell output impedance and/or high converter input filter impedances is effectively eliminated. In many ways, this control system will be analogous to the traditional control schemes used in active power-factor controllers.

F. Converter Input Ripple Current

The influence of converter ripple current on fuel-cell behavior has been presented in [27]. High-frequency ripple currents $(f > 10$ kHz$)$ are internally bypassed by the fuel-cell double-layer capacitance effectively short-circuiting the reactance impedance. The effective fuel-cell high-frequency impedance thus becomes the membrane resistance in series with a small inductance. While high-frequency ripple currents do not have any (measurable) effects on the electrochemical process as they are filtered by the double-layer capacitance, the long-term effects of ripple currents on fuel-cell aging, double-layer capacitance, and membrane are unknown.

Boost converters have inherently very low inductor ripple currents at the input, and in the case of the bridge converters, the fundamental frequency of this ripple current is at twice the switching frequency (Fig. 3). As a consequence of this, only very limited amount of capacitive decoupling is required at the converter input to completely suppress this ripple current.

The advantages of suppressing high-frequency ripple currents from the fuel-cell interface are, however, multiple. First, any potential degradation of the fuel cell due to ripple currents is eliminated. Second, power losses due to rms losses in the fuel-cell membrane resistance, as well as eddy-current losses in interface cables, are avoided. Finally, high-frequency ripple voltages and noise emission from interface cables are suppressed. Thus, small input decoupling capacitors $C_{\rm in}$ are placed across the converter input to effectively eliminate any of the aforementioned potential hazards.

G. Summary of Converter Design Approach

To avoid high ac resistance in high-power low-voltage transformer windings, an extensive interleaving of primary and secondary windings is required. This extensive interleaving of transformer windings leads to extremely low transformer leakage inductance. Stored energy in transformer leakage inductance can thus be dissipated with minimal impact on converter efficiency.

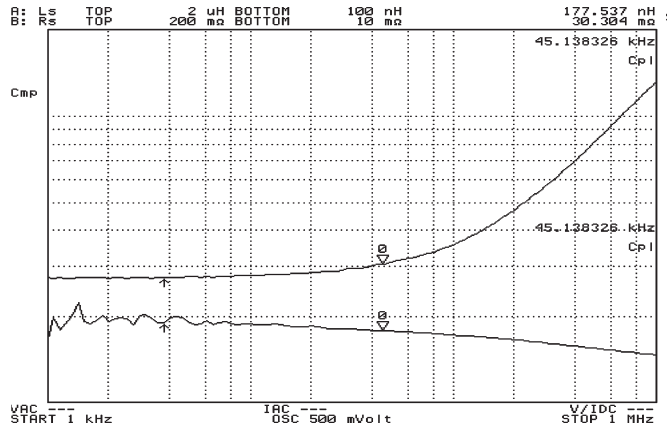

Fig. 7. Measured secondary-side (upper curve) ac resistance and (lower curve) leakage inductance of a 1.5-kW transformer.

Low-voltage MOSFETs are fully rated for repetitive avalanches, allowing MOSFETs to clamp stored energy in leakage inductances. With the careful primary-side layout and the low leakage inductance design of transformers, converter stored leakage inductance energy is very small. Using avalanche-rated MOSFETs, primary-side clamp circuits can be eliminated, and the switch voltage rating can be reduced. Very significant reduction in MOSFET conduction losses is thus achieved.

Finally, the use of silicon carbide Schottky diodes and a low-inductance layout provides very fast current-switching speed, significantly reducing switching losses. Combined, this design approach leads to very high conversion efficiency.

IV. Experimental Results

The experimental results from a 1.5-kW prototype converter are presented in the following.

Using an Agilent 4294A precision impedance analyzer, the ac resistance and leakage inductance of a 1.5-kW prototype transformer are measured (Fig. 7). The transformer design corresponds to the winding configuration in Fig. 4(d). Transferred to the primary side, the ac resistance at 45 kHz is 1.9 mΩ, and leakage inductance is only 11 nH. The leakage inductance in percentage of primary inductance is only 0.01%.

Fig. 8 shows the plots of transformer primary voltage, primary winding current, and secondary current. Figs. 9–11 show the plots of transistor $S4$ voltages and current waveforms. Notice that, except for internal capacitances, there are no turn-on losses. At turn-off, the voltage and current overlap time Δt is measured to 26 ns in Fig. 11. The total turn-off loss shared between all four switches is approximately

$$P_{\text{off,S1–S4}} \approx i_{\text{L1,peak}} v_{\text{S4,av}} \Delta t f_s = 4.6\ \text{W} \qquad (16)$$

corresponding to only 0.3% loss of efficiency.

Figs. 12–14 show plots of the rectifier diode $D2$ voltage and currents. Notice the well-clamped diode voltage, the fast current switching, and the absence of reverse recovery.

Measurement tolerances become very important when measuring efficiency in the range of 97%–98%. Extensive care has to be taken to ensure very high precision and stability of the efficiency test setup.

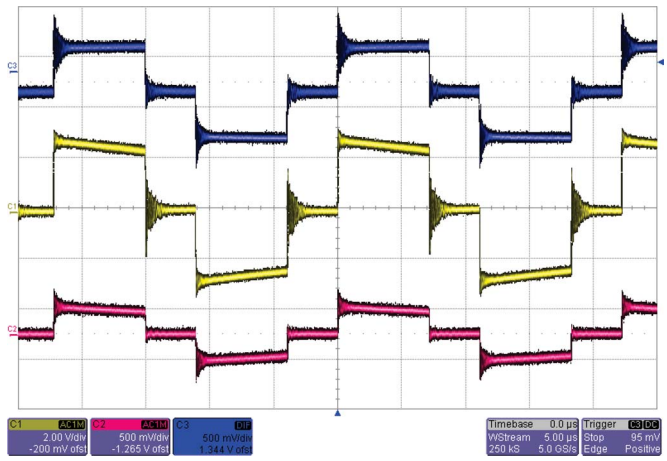

Fig. 8. Measured transformer waveforms at 30-V input and 1.5-kW output power. (From top) Transformer primary voltage (50 V/div), transformer primary current (40 A/div), and transformer secondary current (25 A/div). Time base is 5 μs/div.

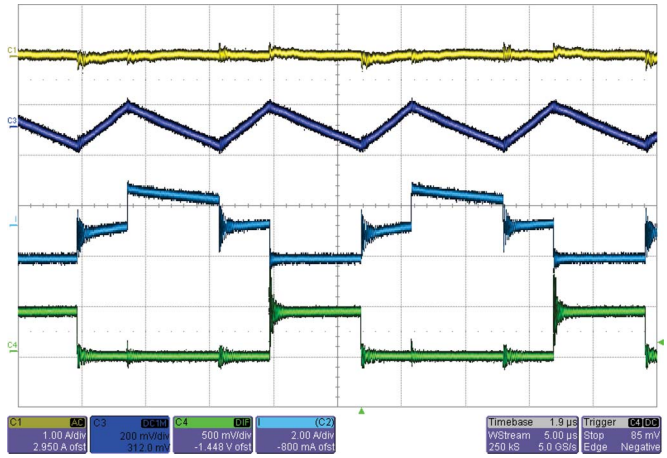

Fig. 9. Measured converter waveforms at 30-V input and 1.5-kW output power. (From top) Converter input ac current $I_{\text{in,ac}}$ (1 A/div), inductor $L1$, ac current (10 A/div), switch $S4$ drain current (40 A/div), and $S4$ drain–source voltage (50 V/div). Time base is 5 μs/div.

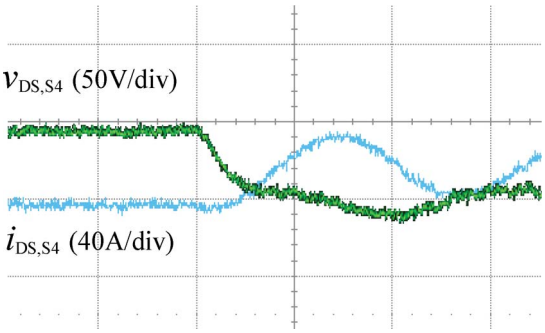

Fig. 10. Expanded view of Fig. 9, showing $S4$ turn-on sequence. Time base is 50 ns/div.

The measured converter efficiency, including transistor-drive losses, is shown in Fig. 15. The maximum efficiency at 30-V input is 97.5%. The efficiency at full load is between 96.8% and 97.9%. The maximum efficiency of the proposed converter is 98%. A photo of the 1.5-kW prototype converter is shown in Fig. 16.

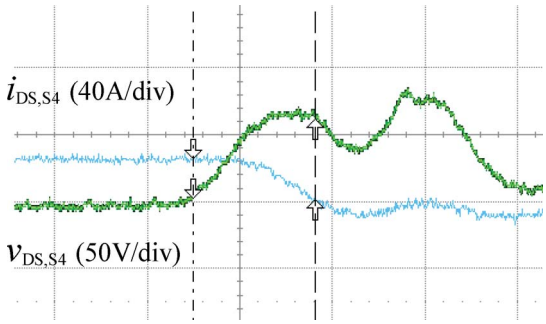

Fig. 11. Expanded view of Fig. 9, showing $S4$ turn-off sequence. Time base is 20 ns/div.

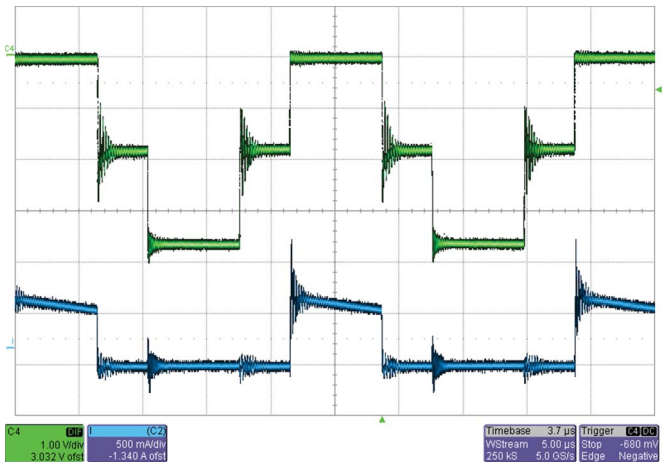

Fig. 12. Measured converter waveforms at 30-V input and 1.5-kW output power. (Top) Diode $D2$ voltage (100 V/div). (Bottom) Diode $D2$ current (10 A/div). Time base is 5 μs/div.

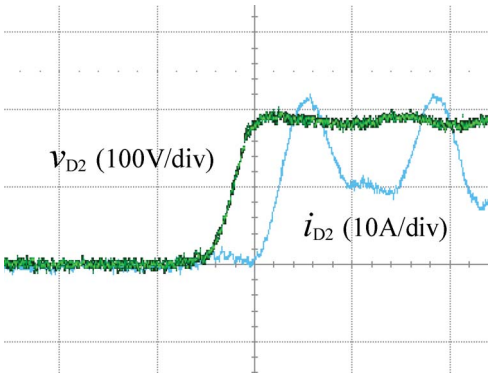

Fig. 13. Expanded view of Fig. 12, showing diode $D2$ turn-on sequence. Time base is 50 ns/div.

V. Conclusion

A new design approach to achieve very high efficiency in low-voltage high-power isolated boost dc–dc converters has been presented. High-power low-voltage transformers require an extensive interleaving of windings to keep ac resistances low. Extremely low primary leakage inductances are achieved, allowing the dissipation of stored leakage energy. Thus, the voltage rating of switches rated for unclamped inductive switching can be reduced, greatly improving converter efficiency. Silicon carbide Schottky diodes have no reverse recovery and allow very fast current switching, further increasing efficiency. Test results from a 1.5-kW prototype converter confirm the achievement of fast current switching, low parasitic circuit inductance, and very high efficiency. The worst case efficiency at maximum load and minimum input voltage is 96.8%. The maximum efficiency of the proposed converter is 98%.

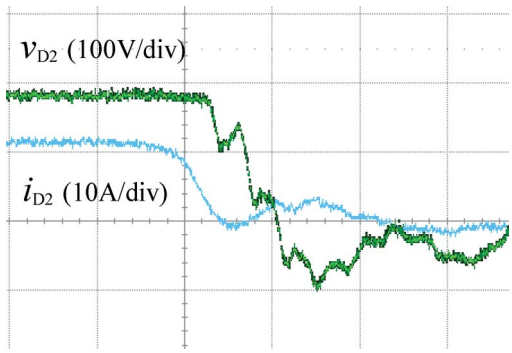

Fig. 14. Expanded view of Fig. 12, showing diode $D2$ turn-off sequence. Time base is 50 ns/div.

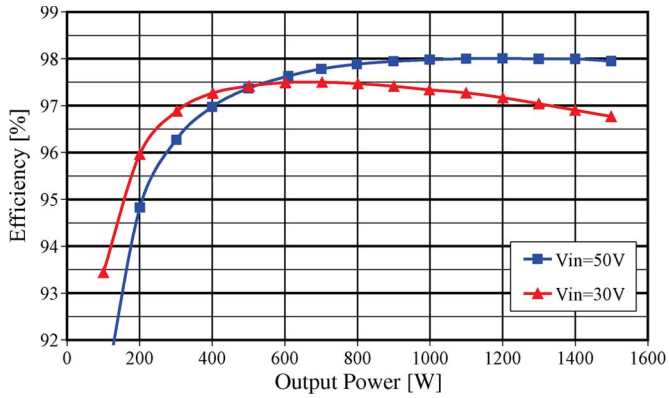

Fig. 15. Measured converter efficiency including drive power.

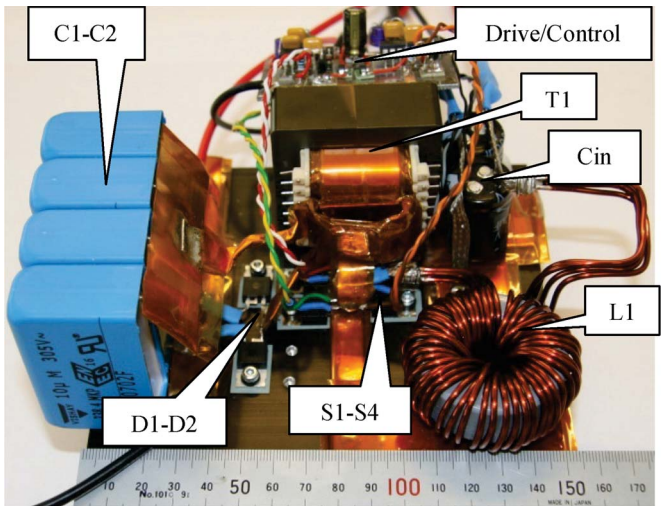

Fig. 16. Photo of 1.5-kW prototype isolated full-bridge boost converter.

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Appendix A3

M. Nymand, R. Tranberg, M. E. Madsen, U. K. Madawala, M. A. E. Andersen, “What is the best converter for low voltage fuel cell applications- A buck or boost?,” in *Proc. IEEE IECON*, Porto, Portugal, 2009, pp. 959-964.

What is the Best Converter for Low Voltage Fuel Cell Applications- A Buck or Boost?

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***Abstract*- Among many converter topologies that have been proposed and developed for low voltage fuel cell applications, isolated full-bridge Buck and Boost converters appear to be the most popular. Although the Buck topology is considered to be superior in performance, particularly for being more efficient, this claim has never been proved with a 'proper' comparison to the Boost topology. This paper presents a comprehensive comparison between Buck and Boost topologies, which are designed for the same specifications and tested under the same and stringent operating conditions using precision measuring equipment. Experimental results of two 1.5 kW prototype Buck and Boost converter units are presented with detailed discussions, and the paper explains why, in contrary to the popular belief, a properly designed Boost topology is superior in performance to Buck topology and more appropriate for low voltage fuel cell applications, as indicated by measured results.**

1. INTRODUCTION

Selection of an appropriate converter topology is an important and fundamental aspect of the design process of power converters used in fuel cell applications as the converter alone plays a major role in its overall performance. At present there are numerous converter topologies with different levels of sophistication, performance, cost, etc, and they may be suitable for a variety of applications. Selection of the best from these available topologies for a particular application, in this case a fuel-cell, would therefore be a challenging task as it invariably involves analysis of various parameters and aspects under various operating conditions. One approach is to design and implement a few selected topologies, and subsequently choose the best, based on results. However, such an approach may not always be economically viable owing to both time and resource constraints. Another approach is to use the information and analysis published in technical documents but this is also difficult as the information provided may be for designs, which have been optimized for different specifications and applications, using circuit components that may not necessarily be available in the current market. This difficulty is further compounded by the fact that important data such as efficiency measurements are not often provided or measured either under different or unknown conditions, negating any possible direct comparisons. Finally, even if all of the above difficulties could be overcome, still the results published would quickly become somewhat obsolete as previously made comparisons may not be valid with new components or technological discoveries.

In fuel cell applications, efficiency of the converter is a key parameter of the overall design process. This is because the size, cost, efficiency and reliability of the overall system largely depend on the losses of the converter at minimum input voltage, where input current is maximum when delivering maximum power. A power converter with very high efficiency is thus an essential requirement for fuel-cell applications. However, as discussed above, selection of a converter topology, which is efficient over the entire operating range and appropriate for fuel-cell applications, is not an easy task,

According to literature, isolated full-bridge Buck converter and isolated full-bridge Boost converter are the two topologies that have been identified as most appropriate for fuel-cell applications [1-14]. Traditionally, for a given input voltage range, Boost converters are most efficient at high input voltage whereas Buck converters are more efficient at low input voltage. This implies that Buck converters are the preferred topologies for fuel cell applications, since the efficiency at low input voltages has a major impact on the overall design and subsequent performance. Prime example is the V6 topology reported in [1-3], which demonstrated a very high efficiency at low input voltage and maximum power. However, Boost topologies have characteristics, such as continuous input current, low input ripple current, good clamping of output diodes requiring less than half of the voltage rating of rectifier diodes, etc, which are ideal for fuel cell applications, and therefore despite the inclination towards the Buck topology at low input voltage, many attempts have also been made to improve the efficiency of Boost topology at low input voltage, making it the ideal choice for fuel-cell applications [6-13]. These attempts include optimizing the transformer design to achieve very low leakage inductances, taking advantage of modern power MOSFETs repetitive avalanche ratings and Silicon Carbide (SiC) Schottky diode's very fast di/dt ability during turn off and eliminating the need for a voltage clamp circuit [13]. Consequently, Boost converters now appear to offer comparable performance even at low input voltages. Unfortunately, these superior claims on performance have only been made using converters that have been designed, analyzed and tested on individual basis and under different operating conditions.

A comprehensive comparison between these two topologies, which are designed for the same specifications and tested under the very same operating conditions, is yet to

be reported, and would be of significant benefit to both the research and industry community. The purpose of this paper is therefore to fulfill this long overdue need by providing a comprehensive comparison between these two topologies, including methodical design and experimental testing. The paper details the design aspects of each converter topology, highlighting the importance of optimizing the high frequency inductor and transformer windings, which has greater impact on the efficiency. Implementation and prototyping issues of a 1.5 kW unit of each type, using most recent technological advances such as SiC Schottky diodes and very low impedance power MOSFETs, are then discussed. Finally, a comprehensive comparison between the two prototype units, tested under same and stringent operating conditions, is provided with experimental analysis to show that the Boost topology is indeed superior in performance over the entire operating range of a typical fuel-cell application.

2. DESIGN CONSIDERATIONS

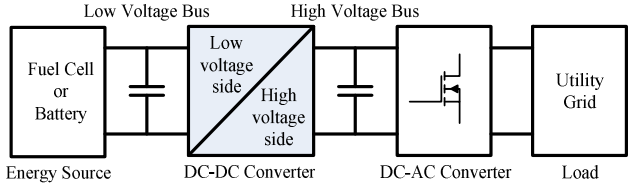

Fig. 1 A typical fuel-cell system

Fig. 1 shows the system configuration of a typical fuel cell application, where the DC-DC converter is powered by low voltage DC bus to produce a high voltage DC bus. The two possible Buck and Boost topologies that may be used for this DC-DC converter are designed in accordance with the specifications given in Table I. Theoretical voltage and current waveforms of the two converter topologies are illustrated in Fig. 3, and Fig. 6, respectively. The following common design practices are adhered to during the design of both converters.

Having very high input currents, both converters are hard switched in order to keep conduction losses at a minimum while avoiding circulating currents.

Transformer design is based on careful multiple interleaving of primary and secondary windings to avoid severe proximity effect due to high current in the primary winding.

SiC Schottky diodes are used as high voltage rectifiers, since they do not suffer from reverse recovery. Consequently, very fast diode turn-off can be achieved without sacrificing efficiency.

To reduce stray leakage inductances and ac resistances, all high current conductors are made as short as possible, using wide copper foil conductors in close proximity to the return current path.

Low impedance foil type capacitors are used for filter capacitors to ensure low ac losses.

Both converters are designed to operate at 45 kHz switching frequency with input and out ripple frequency at 90 kHz.

Each design is individually optimized for the same specifications, given in Table I, using similar components and technologies where relevant. State-of-the art components are used in each converter to achieve the best possible efficiency.

TABLE I.
CONVERTER SPECIFICATIONS

Parameter	Value	Comments
Output power P_{out}	1500 W	
Input voltage range V_{in}	30-50 VDC	Start-up voltage up to 60V
Output voltage V_{out}	400 VDC	Galvanic isolation required
Efficiency target η	98 %	Converter efficiency to be optimized at low input voltage.
Output power regulation	0-100 %	For full control of input current transients
Input current ripple >10kHz	<15 %	For load range 15-100%
Input current slew rate	<3 A/s	Slow dynamics of fuel cell

3. ISOLATED FULL-BRIDGE BUCK CONVERTER DESIGN

An isolated Buck converter topology is shown in Fig. 2 and its typical waveforms are illustrated in Fig. 3. Steady state voltage transfer function for the converter, shown in Fig. 2, is given by (1).

$$\frac{V_0}{V_{in}} = 2nD \qquad (1)$$

Where D is the primary switch duty cycle (D<0.5) and n = Ns/Np, is the transformer turns ratio. A transformer turns ratio of n=16 is chosen to allow for a sufficient voltage margin to compensate for internal voltage drops, control dynamics and overlap protection at the minimum input voltage. If the voltage spikes are ignored, the rectifier diodes D1-D4, can be regarded as subjected to a reverse voltage of

$$V_{D,RRM} = nV_{in,max} \qquad (2)$$

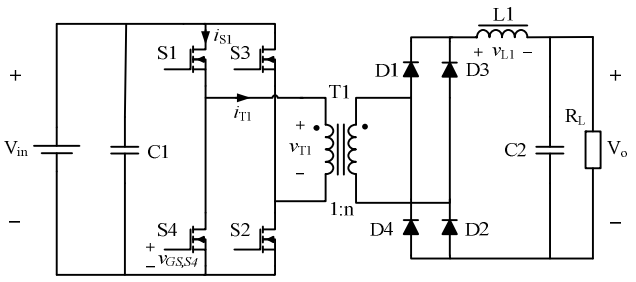

Fig. 2 Isolated full-bridge Buck converter

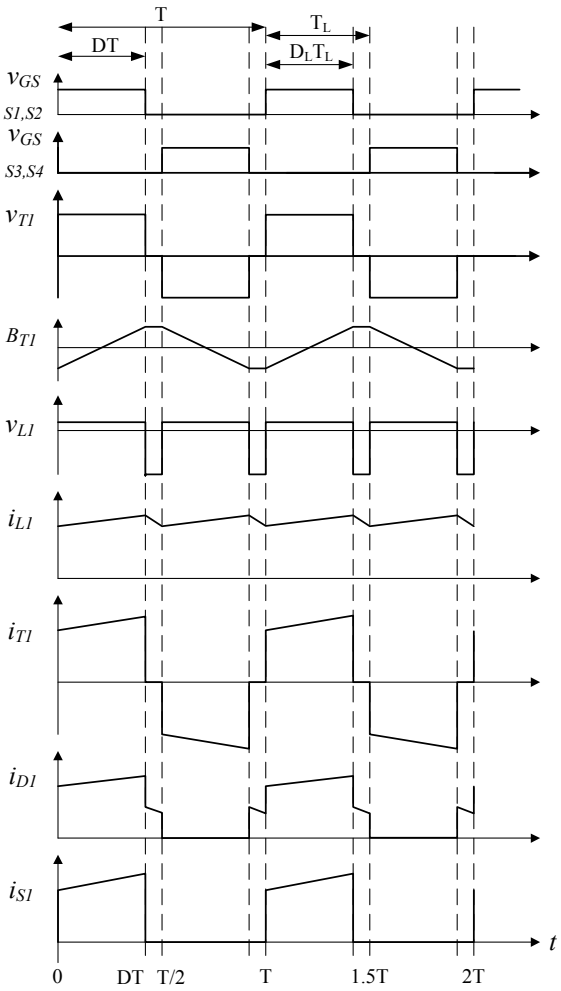

Fig. 3 Typical waveforms of isolated Buck converter

At 60 V input, the diode reverse voltage will thus be in excess of 960 V. When using normal silicon based epitaxial diodes, reverse recovery losses become excessive at voltage rating above approximately 600 V. Thus, the traditional solution is to use two series connected secondary's, each using 600 V diodes. While this solution reduces reverse recovery losses, it doubles the forward voltage drop. In contrast, SiC Schottky diodes, being relatively more expensive, do not suffer from reverse recovery, and are becoming available at ratings up to 1200 V. Therefore in this design, to achieve maximum efficiency, a single rectifier stage, using four 1200 V SiC Schottky (C2D05120) diodes from Cree, is used.

Power MOSFETs of 3.3 mΩ/75 V in standard TO-220 packages are used for the primary switches. The RMS current flowing in the switches is given by

$$I_{Sl,RMS} = I_o n\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{[\Delta i_{s1}/2]}{nI_o}\right)^2} \qquad (3)$$

For situations, where $\Delta I_{s1} << nI_o$,

$$I_{Sl,RMS} \approx I_o n\sqrt{D} = \frac{P_o}{V_o} n\sqrt{D} \qquad (4)$$

The components used in the design are given in Table II.

TABLE II.
FULL-BRIDGE BUCK CONVERTER COMPONENTS

Component	Type	Specification
S1-S4	IRFB 3077	3.3 mΩ/75 V
D1-D2	C2D05120	5 A/1200 V
L1	Magnetics Kool Mu 77439	1.6mH @ 3.8 A
T1	EE55/21 3F3	$n=N_S/N_P=16$
C1	MWR1105330 - MKT	6x 33µF/100 V
C2	MKP	4 x 1µF/630 V

TABLE III.
TRANSFORMER DESIGN OF FULL-BRIDGE BUCK CONVERTER

Transformer data:	
Core	E55/28/21 – N87
Primary	4 turns 25x0.6 mm Cu foil
Secondary	64 turns. 48 turns 2x0.78 + 16 turns 6x0.48 mm
Turns ratio	16
Insulation	3 layer 50 µm Kapton
Intersections	8
Primary leakage	14 nH @45 kHz (measured)
Primary DC-resistance	1.4 mΩ (measured)
Primary AC-resistance	1.8 mΩ @45 kHz (measured)
Core loss	1.2 W @ 60 °C
Winding loss	6.4 W @ (Vin=30 V, Pout=1.5 kW)
Total loss	7.6 W
Efficiency	99.5 % @1.5 kW

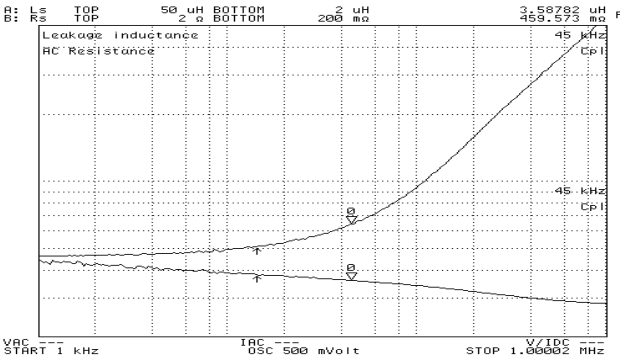

Fig. 4 Measured ac resistance (upper curve) and leakage inductance (lower curve) of Buck transformer

The detailed transformer design is presented in table III. To avoid excessive proximity effect, each of the 4 primary windings has to be interleaved between sections of secondary windings. The high transformer turns ratio required, further complicates the transformer design and manufacturing.

Fig. 4 shows measured ac resistance and leakage inductance of the transformer referenced to secondary side.

As can be seen from the presented loss data and the measured impedances, even though the transformer design has been challenging, the final performance was outstanding, having an efficiency of approximately 99.5 % at minimum input voltage and maximum power.

4. ISOLATED FULL-BRIDGE BOOST CONVERTER DESIGN

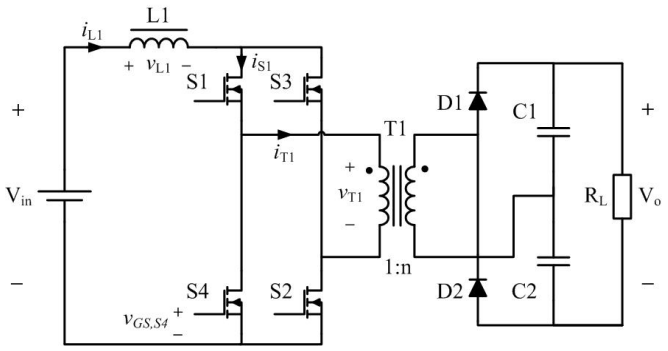

Fig. 5 Isolated full-bridge Boost converter

An isolated Boost converter and its typical waveforms are shown in Fig. 5 and Fig. 6, respectively. A voltage doubler is employed at the output, effectively reducing the transformer turns ratio by a factor two, and saving two rectifier diodes at the expense of a larger output capacitor.

Steady state voltage transfer function of the isolated full-bridge boost converter is given by (5).

$$\frac{V_0}{V_{in}} = \frac{n}{1-D} \tag{5}$$

Where D (> 0.5) is primary switch duty cycle and $n=N_S/N_P$ is transformer turns ratio. For the prototype, a transformer turns ratio of 4 is used.

As evident from Fig. 5, since the rectifier diodes are placed directly across the output capacitors, diode reverse voltage is effectively limited to output voltage. Both 600 V silicon diodes and SiC Schottky diodes can therefore be used. However, SiC Schottky diodes, which facilitate much faster turn-offs, are used to reduce switching losses. As in the case of the Buck design, the same power MOSFETs of 3.3 mΩ/75 V are used for the active switches of the Boost converter. The RMS current flowing in the switches is given by

$$I_{Sl,RMS} = I_{in}\frac{\sqrt{3-2D}}{2}\sqrt{1+\frac{1}{3}\left(\frac{[\Delta i_{L1}/2]}{I_{in}}\right)^2} \tag{6}$$

For situations, where $\Delta I_{L1} << I_{in}$,

$$I_{Sl,RMS} = I_{in}\frac{\sqrt{3-2D}}{2} = \frac{P_o}{\eta V_{in}}\frac{\sqrt{3-2D}}{2} \tag{7}$$

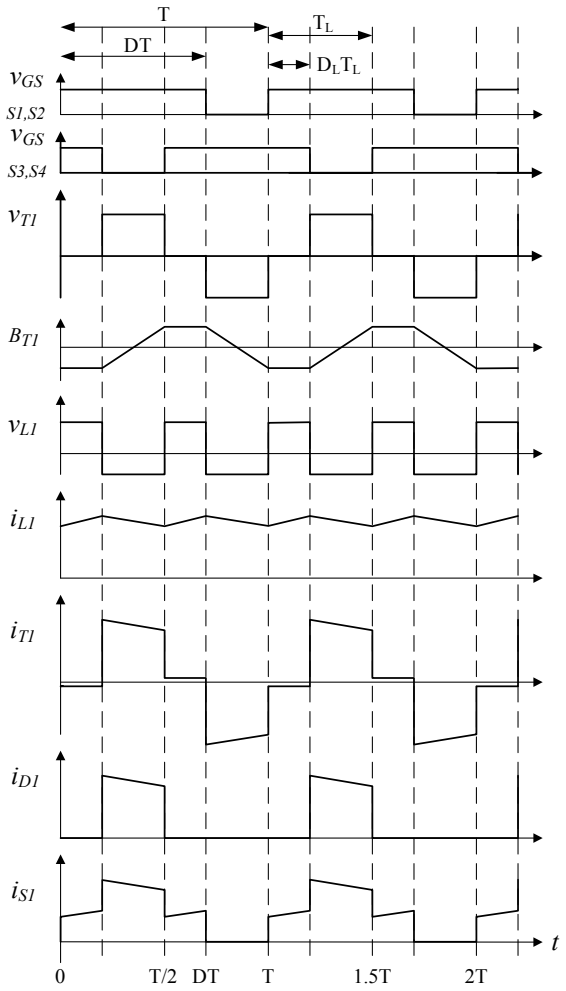

Fig. 6 Typical waveforms of isolated Boost converter

TABLE IV.
FULL-BRIDGE BOOST CONVERTER COMPONENTS

Component	Type	Specification
S1-S4	IRFB 3077	3.3 mΩ/75 V
D1-D2	IDT 10S60C	10 A/600 V
L1	Magnetics Kool Mu 77439	10μH @ 51 A
T1	EE55/21 3F3	$n=N_S/N_P=4$
C1	MKP	2x 10μF/630 V

Component selection of the prototype Boost converter design is shown in Table IV while the detailed transformer design is presented in Table V. The primary winding is similar to that of the Buck converter transformer thus requiring the same level of interleaving. The secondary winding is however much simpler since the turns ratio is only 1:4.

Fig. 7 shows the measured ac resistance and leakage inductance of the transformer referenced to secondary side. Notice that the leakage inductance referred to the secondary side is only 178 nH in contrast to 3.6 μH in the full-bridge Buck transformer. As can be seen from the test results in the

subsequent section, this lower leakage inductance will greatly reduce characteristic impedance of parasitic resonance circuits. The transformer efficiency at minimum input voltage and maximum power is 99.6 %, and is similar to the full-bridge Buck transformer.

TABLE V.
TRANSFORMER DESIGN FULL-BRIDGE BOOST CONVERTER

Transformer data:	
Core	E55/28/21 – N87
Primary	4 turns 25x0.6 mm Cu foil
Secondary	16 turns 25x0.15 mm Cu foil
Turns ratio	4
Insulation	3 layer 50 µm Kapton
Intersections	8
Primary leakage	11 nH @45 kHz (measured)
Primary DC-resistance	1.6 mΩ (measured)
Primary AC-resistance	1.9 mΩ @45 kHz (measured)
Core loss	1.7 W @ 60 °C
Winding loss	3.8 W @ (Vin=30 V, Pout=1.5 kW)
Total loss	5.5 W
Efficiency	99.6 % @ 1.5 kW

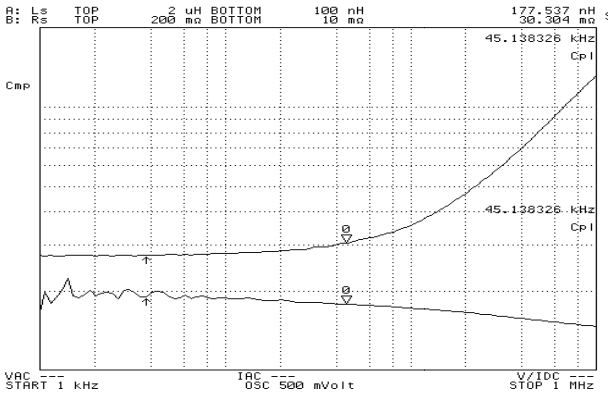

Fig. 7 Measured ac resistance (upper curve) and leakage inductance (lower curve) of Boost transformer

5. EXPERIMENTAL VERIFICATION

To make a fair comparison, a Buck and a Boost converter were built, carefully optimizing the design for minimum losses. The two 1.5 kW prototype Buck and Boost converters built for the study, are shown in Fig. 8 and Fig. 9, respectively.

Fig. 10, shows the measured voltages and currents of the prototype 1.5 kW full-bridge Buck converter, operated at 30 V input and full load with a duty cycle of 42.5 %. Fig. 11 shows the measured voltages and currents of the prototype 1.5 kW full-bridge Boost converter, operated at 30 V input and full load with a duty cycle of 70 %. Having much higher voltage and a larger leakage inductance at the output, the Buck converter ringing appears to be more significant.

Efficiency of both converters are measured, using high precision equipment. At maximum input voltage and maximum power, the Buck converter efficiency is 95.3 % whereas the Boost converter efficiency is 97.9 %, as demonstrated in Fig. 12. At high input voltage, power losses in the Buck converter are thus more than twice in comparison to those in the Boost converter.

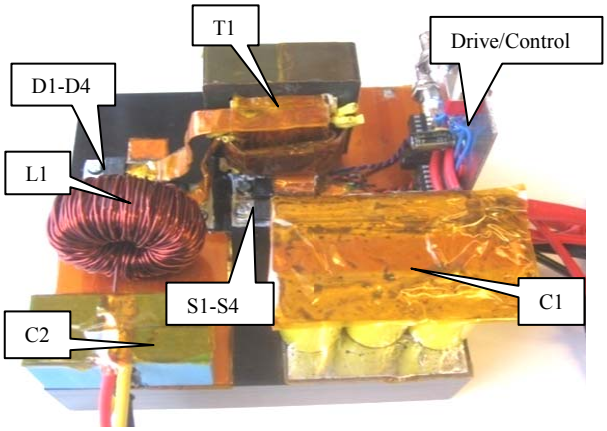

Fig. 8 A prototype 1.5 kW Full-Bridge Buck converter.

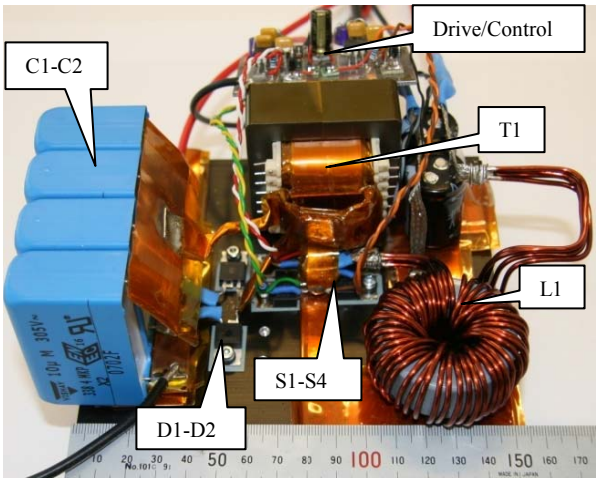

Fig. 9 A prototype 1.5 kW Full-Bridge Boost converter.

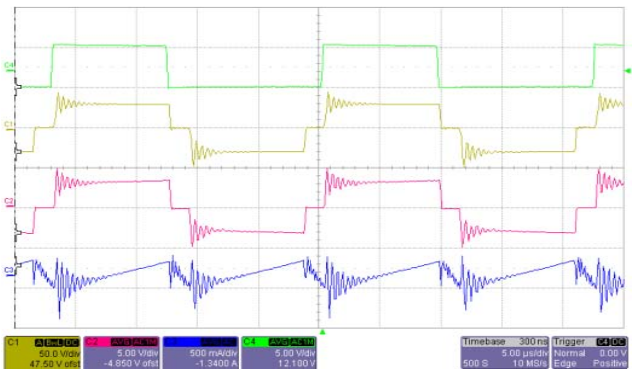

Fig. 10 Measured Buck converter waveforms at 30 V input and 1.5 kW output. From top: control signal, transformer primary voltage (50V/div), transformer primary current (100A/div), inductor L1, ac current (o.5A/div). Time base is 5µs/div.

Measured efficiency at low input voltage is shown in Fig. 13. At maximum power, Buck converter efficiency is 95.4 %, whereas Boost converter efficiency is still 96.7 %. Worst case power dissipation in the Buck converter is thus 74 W while Boost converter maximum power dissipation is only 51 W.

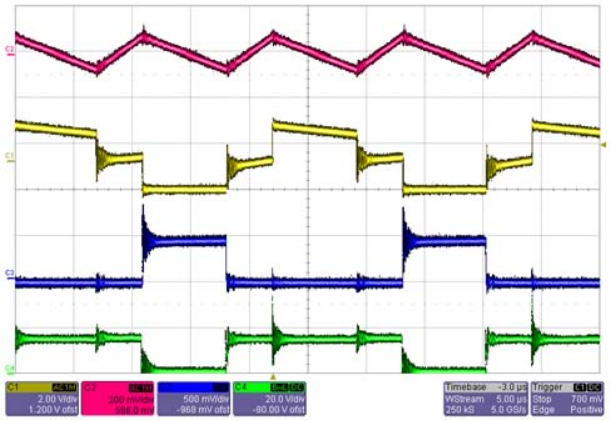

Fig. 11 Measured Boost converter waveforms at 30 V input and 1.5 kW output. From top: inductor L1, ac current (10A/div), primary switch current (40A/div), Primary switch drain-source voltage (50V/div), gate drive signal (20V/div). Time base is 5µs/div.

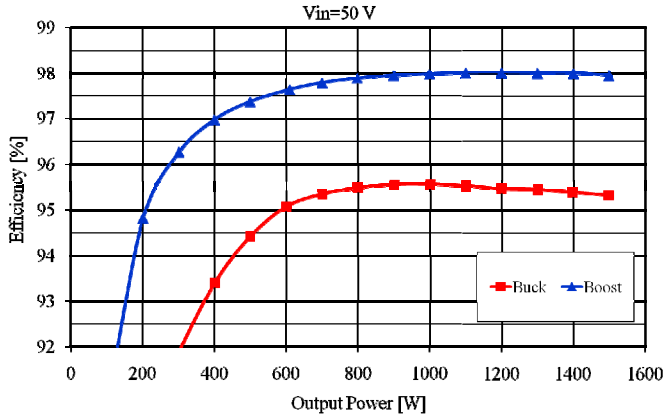

Fig. 12 Measured converter efficiency for Buck and Boost converters at 50V input.

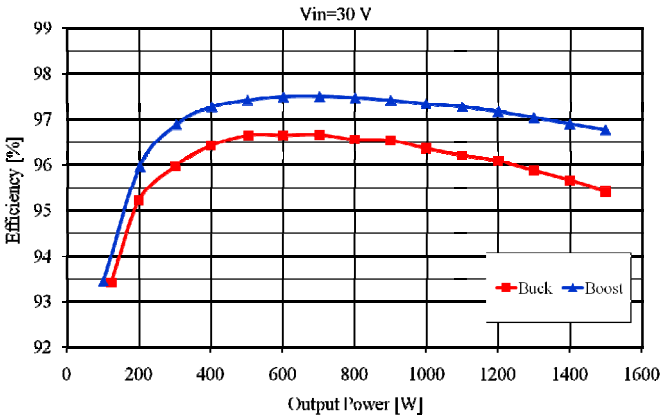

Fig. 13 Measured converter efficiency for Buck and Boost converters at 30V input.

5. Conclusion

A comprehensive comparative study on both design and performance between isolated full-bridge Buck and Boost converter topologies has been presented. Both converters have been designed for the same specifications and tested under the same and stringent operating conditions using precision equipment. Issues in relation to design and measurement have been discussed in detail. In contrary to popular belief, the measured results suggest that the Boost topology is more appropriate for low voltage fuel-cell applications, being superior in performance in comparison to the Buck topology. The relatively low RMS current in the primary switches of the Boost topology has been identified as the key for the superior performance.

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Appendix A4

M. Nymand, U. K. Madawala, M. A. E. Andersen, B. Carsten, O. S. Seiersen, “Reducing ac-winding losses in high-current high-power inductors,” in *Proc. IEEE IECON*, Porto, Portugal, 2009, pp. 774-778.

Reducing AC-Winding Losses in High-Current High-Power Inductors

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***Abstract*- Foil windings are preferable in high-current high-power inductors to realize compact designs and to reduce dc-current losses. At high frequency, however, proximity effect will cause very significant increase in ac resistance in multi-layer windings, and lead to high ac winding losses. This paper presents design, analysis and experimental verification of a two winding technique, which significantly reduces ac winding losses without compromising dc losses. The technique uses an inner auxiliary winding, which is connected in parallel with an outer main winding. The auxiliary winding is optimally designed with low ac resistance and leakage inductance to carry the ac current while the outer winding is designed for the large dc current. Detailed analysis and design of a 350 A, 10 kW inductor with the proposed technique are presented with discussions. Experimental results of a prototype 350 A inductor, used in a 10 kW fuel cell dc-dc converter, are also presented to demonstrate the validity of the proposed technique and its superior performance.**

I. INTRODUCTION

Storage inductors, such as those used in PWM controlled dc/dc converters, are generally designed to operate under high dc bias current conditions with a limited ac current ripple. To minimize inductor size and maximize efficiency, it is therefore preferable to use core materials with saturation flux density as high as possible while keeping the dc-resistance of the winding at a minimum. Since ac currents, and thus ac flux, are much smaller, core hysteresis losses and winding ac-resistances can be somewhat higher as a compromise to a inductor with smaller size and higher efficiency. Usually, for low to medium power levels, torroid cores in powdered iron material, such as Magnetics Kool Mu and others, with single layer round wire windings are very efficient solutions for storage inductors [1].

However, as the current level increases, the required copper cross section also invariably increases. As a consequence, ac-resistances in the winding will increase to a point, due to eddy current effects, beyond which the ac loss in the winding becomes significant and cannot be further ignored. This effect could be alleviated to a certain extent by paralleling multitude of smaller diameter wires [1], but would eventually become impractical and impossible as the required copper cross section becomes simply too large to handle with single layer windings made with discrete wires.

Many techniques to reduce eddy current losses in inductor windings have been proposed with their own merits and limitations [2-7]. A planar Litz winding is proposed for high ac current applications in [2], while [3] utilizes braided and transposed individually isolated wires for a similar application. However, Litz wires are expensive and invariably have very poor fill factors. Consequently, in both cases the reduction in eddy current losses was achieved at the expense of high dc losses, caused by the significant increase in the dc resistance.

Another solution for this problem is to use E cores with copper foil windings. Copper foil windings offer very high fill factors, and are relatively easy to wind with large copper cross sections. However, as discussed in this paper, even copper foil windings will exhibit very large ac resistances due to proximity effects, unless the winding is optimally designed. In [4], a comparison of foil and helical windings in a 150 kW Boost converter application is presented. At 15 kW, inductor losses are higher than 175 W and correspond to a 1.2 % loss of efficiency.

Use of foils with uneven foil thickness is suggested in [6]. This is because inner turns of a winding have the worst proximity effect and the shortest turn length, and hence the smallest resistance per turn. Therefore according to this technique, winding losses can be reduced by 13 % by reducing the foil thickness of the inner turns of a winding. However, manufacturing foil windings with variable thicknesses is very complex and expensive.

In contrast to the above reported technique, this paper proposes a methodical and yet simple technique, whereby the ac loss of a winding can be minimized by using multilayer foil windings. Generally, a thin multilayer winding will have a much lower ac-resistance, due to lower proximity effect, than that of a thick main winding. But it invariably has a higher dc resistance due to lower copper cross section. However, with proper and careful design of both main and auxiliary windings, the smaller ripple ac current can be guided into the thin auxiliary winding, significantly reducing ac losses. The dc losses are kept low as the dc current is split between the two windings according to their dc-resistances. Both applicability and effectiveness of the proposed technique are verified using measured results of a prototype 350 A inductor in a 10 kW converter.

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II. MULTILAYER SINGLE WINDING INDUCTORS

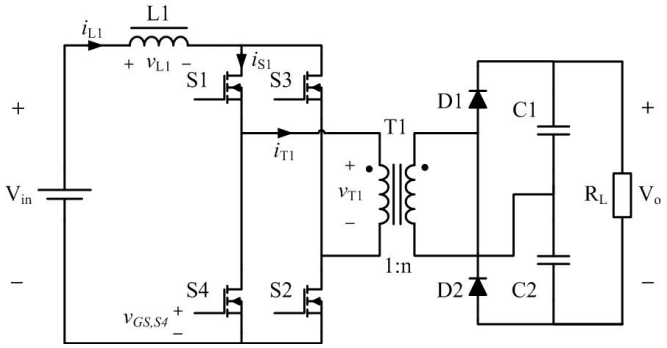

Fig. 1 High-power high-current dc-dc converter for low voltage fuel cell applications.

Inductors of typical high power converters, used in typical fuel-cell applications as shown in Fig. 1, operate under high level of dc bias currents with relatively small ac ripple. The winding loss of such a multilayer single winding inductor, which carries both dc, I_{dc}, and ac, i_{ac}, currents, can be represented by the sum of dc power loss, $P_{W,dc}$, and the ac power loss, $P_{W,ac}$, as defined by the following equations.

$$P_{W,dc} = R_{dc} I_{dc}^2 = \frac{\rho_c l_w}{A} I_{dc}^2 \quad (1)$$

$$P_{W,ac} = K_r R_w^* I_{ac,rms}^2 \quad (2)$$

Where ρ_c (Ωm) is the specific resistivity of copper, l_w (m) is the length of the winding and A (m^2) is the cross section of the wire, R^*_w is the dc resistance of a winding with the thickness of one penetration depth, δ (m), at the fundamental ripple frequency, and K_r is the normalized effective ac resistance factor as defined in [8].

Fig. 2 shows the normalized effective ac resistance factor K_r of a winding carrying a triangular ac current, plotted as a function of relative conductor height, *h/δ,* and number of layers, m [8]. As evident, inductors with multiple layers and large conductor cross sections, where the ratio between conductor height and penetration is invariably large, suffer from severe proximity effect. Consequently, K_r of such windings is substantially large, and hence the ac winding resistance is several orders of magnitude of its dc winding resistance. In some situations, K_r is too large to the extent that the ac loss cannot be simply ignored even though the ac current is only a small fraction of the dc current.

One solution to this problem is to use individually isolated thin wires or Litz wires or braided wires in bundles as reported in [2], [3]. This will effectively reduce the ac-resistance, but the dc-resistance will also be dramatically increased as the copper fill factor becomes much lower and the wire length is increased. Usually, the dc current in storage inductors is much higher than the ac ripple current, and therefore any increase in dc resistance is highly undesirable.

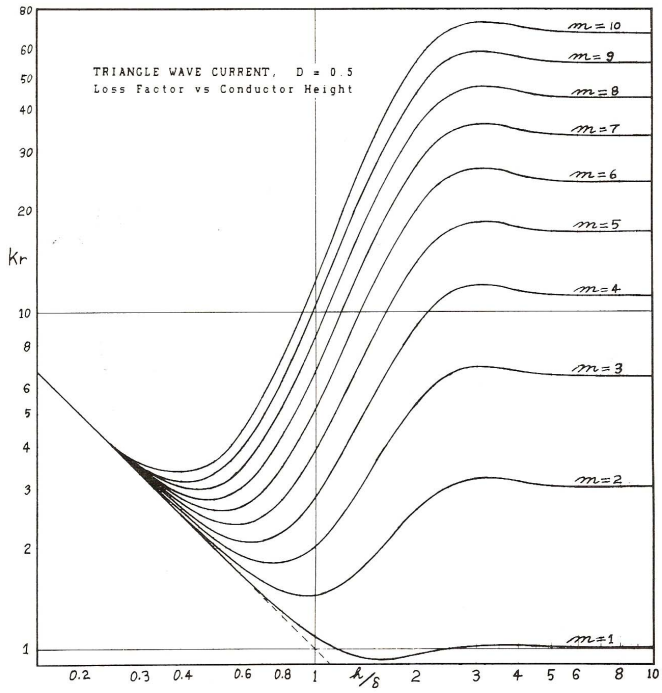

Fig. 2. Normalized effective ac resistance factor Kr, as function of conductor height in penetration depth.

Alternatively, a marginal reduction of approximately 13 % could be obtained by using uneven conductor thicknesses, whereby the winding foil thickness can be gradually increased from the inner most turn to the outer turn, as proposed by [6]. However, this approach will not significantly reduce the ac losses, and are very difficult to implement.

III. PROPOSED OPTIMALLY DESIGNED TWO WINDING INDUCTOR

For a fixed operating point of an inductor with same core and inductance, R^*_w and $I^2_{ac,rms}$ will be constant, and thus the ac power loss of a winding is directly proportional to its K_r factor, as expressed below.

$$P_{w,ac} = K_r R_w^* I_{ac,rms}^2 \propto K_r \quad (3)$$

In Fig. 2 we can see that for multi layer windings ($m \geq 2$), the K_r factor reaches a minimum value for ratio of conductor height to penetration depth h/δ, somewhere in the region of $0.4 < h/\delta \leq 1$. As the ratio of conductor height to penetration depth is generally much higher than one, h/δ is typically in the range of 5-10 in high-current high-power inductors. This implies that if the ac part of the inductor current is forced to flow in a thinner winding, which is in parallel with a thicker winding, then the ac loss could be significantly reduced. This steering or forcing of the ac current into a thinner winding

can be obtained by adding an auxiliary ac-winding inside the main dc-winding, as illustrated in Fig. 3.

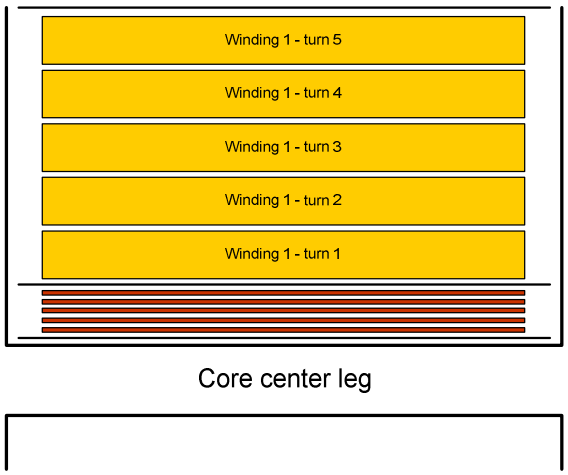

Fig. 3 A winding with an inner auxiliary ac-winding W2, and outer main dc-winding W1.

The winding, shown in Fig. 3, can be represented by an ac model in Fig. 4, where $L_{LK,W1}$, $L_{LK,W2}$, $R_{W1,ac}(n\omega_L)$, and $R_{W2,ac}(n\omega_L)$ are the leakage inductances and ac resistances of the two windings.

Because of invariably larger K_r factor, the main dc-winding W1 will have a significantly larger ac-resistance, which is in series with the relatively large leakage inductance of the outer dc-winding. The inner ac-winding W2 will have a significantly lower ac-resistance (but higher dc-resistance), and also a smaller leakage inductance, primarily from terminations.

Since the impedance of inductor L_1 is much larger than the two winding ac impedances Z_1 and Z_2, the majority of the applied voltage will appear across L_1. The ac inductor current $i_{L1,ac}$ thus becomes a triangular current as illustrated in Fig. 5.

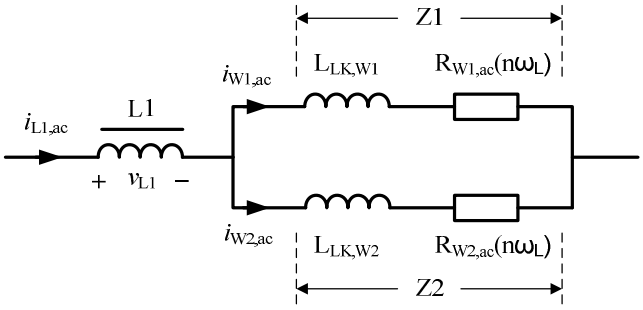

Fig. 4. Equivalent circuit diagram of a two-winding inductor.

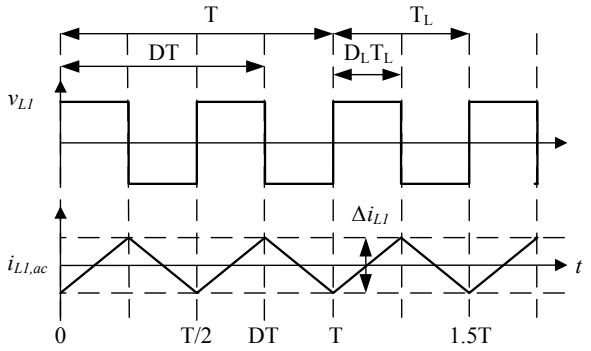

Fig. 5. Inductor voltage and ac current at 50 % inductor duty cycle D_L.

The RMS value of the triangular inductor ripple current $i_{L1,ac}$, can be found by the following relationship

$$i_{L1,ac,rms} = \frac{\Delta i_{L1}}{2\sqrt{3}} \tag{4}$$

Using Fourier analysis, the inductor ac current at 50 % duty cycle can be expressed as

$$i_{L1,ac} = \frac{4\Delta i_{L1}}{\pi^2} \sum_{n=1,3,5\ldots} \frac{\cos n\omega_L t}{n^2} \tag{5}$$

Where n=1, 3, 5… is the harmonic number and $\omega_L = 2\pi f_L = 2\pi/T_L$, and T_L is the period of the ac ripple current in the inductor as shown in Fig. 5.

Since the two winding ac impedances Z_1 and Z_2 share the same voltage, the current sharing between the windings, at each harmonic frequency, is defined as

$$\frac{i_{W1}(n\omega_L)}{i_{W2}(n\omega_L)} = \frac{Z2(n\omega_L)}{Z1(n\omega_L)} = \frac{jn\omega_L L_{LK,W2} + R_{W2,ac}(n\omega_L)}{jn\omega_L L_{LK,W1} + R_{W1,ac}(n\omega_L)} \tag{6}$$

The ac resistance of the windings at the n^{th} harmonic frequency, $R_{W1,ac}(n\omega_L)$ and $R_{W2,ac}(n\omega_L)$, are the proximity effect factor $F_R(n\omega_L)$, at the n^{th} harmonic frequency multiplied by the winding dc resistance

$$R_{W,ac}(n\omega_L) = F_R(n\omega_L)R_{W,dc} =$$

$$= \left[\varphi_n \frac{\sinh 2\varphi_n + \sin 2\varphi_n}{\cosh 2\varphi_n - \cos 2\varphi_n} + \frac{2(m^2-1)}{3}\varphi_n \frac{\sinh \varphi_n - \sin \varphi_n}{\cosh \varphi_n + cos\varphi_n}\right] R_{W,dc}. \tag{7}$$

Where h is the conductor height, m, is the number of layers and $\varphi_n = h/\delta_n$ where $\delta_n = \sqrt{2\rho_C / \mu_0\mu_r n\omega_L}$ is the penetration depth at the n^{th} harmonic frequency.

From the above, it becomes clear that current sharing between the two windings will vary with frequency i.e. with the harmonic content of the inductor current.

In (5) we can see that the amplitude of the current harmonics falls exponentially with the harmonic number. Since further the power loss is proportional to the square of the RMS current, then most of the power losses will be concentrated at the fundamental frequency and the lower harmonics.

In this particular case, the ac impedances of the two windings are dominated by the inductive voltage drops across the two winding leakage inductances. Therefore

$$\left|jn\omega_L L_{LK,W2}\right| \gg R_{W2,ac}(n\omega_L)$$

and

$$\left|jn\omega_L L_{LK,W1}\right| \gg R_{W1,ac}(n\omega_L)$$

And the sharing of winding currents becomes simply

$$\frac{i_{W1,ac}}{i_{W2,ac}} = \frac{L_{LK,W2}}{L_{LK,W1}} = Constant. \qquad (8)$$

As can be seen from (8), the current sharing is simply controlled by the ratio of the winding leakage inductances. The shapes of the currents are triangular, hence similar to the total inductor ac current $i_{L1,ac}$.

Under this condition, the power loss can be calculated using (8), and the relative reduction in the ac winding losses of the inductor becomes

$$\frac{P_{W1,ac} + P_{W2,ac}}{P_{W,L1,ac}} = \frac{K_r(W1)l_{W1}(\Delta i_{W1})^2 + K_r(W2)l_{W2}(\Delta i_{W2})^2}{K_r(L1)l_{W,L1}(\Delta i_{W1} + \Delta i_{W2})^2} \qquad (9)$$

Where l_{W1}, l_{W2} and $l_{W,L1}$ are the lengths of wires of winding 1, 2 and the single winding, respectively.

IV. Experimental Verification

In order to validate the proposed design, a prototype 10 kW isolated boost converter intended for applications such as fuel cell hybrid electrical vehicles, was built with a high power inductor. For the converter to operate from 30 V input at a switching frequency of 45 kHz, a 1.8 µH and 350 A storage inductor with an ac ripple at 90 kHz, is needed. The required inductor was built, using five turns on a Magnetics Kool Mµ EE80 core 00K8020E40µ, and allowing 40% reduction in initial permeability at maximum current. The available window area of the core allowed the use of up to 3.1 mm thick and 45 mm wide turns for the two windings, providing a copper cross section area of 139.5 mm^2, corresponding to a dc current density of 2.5 A/mm.

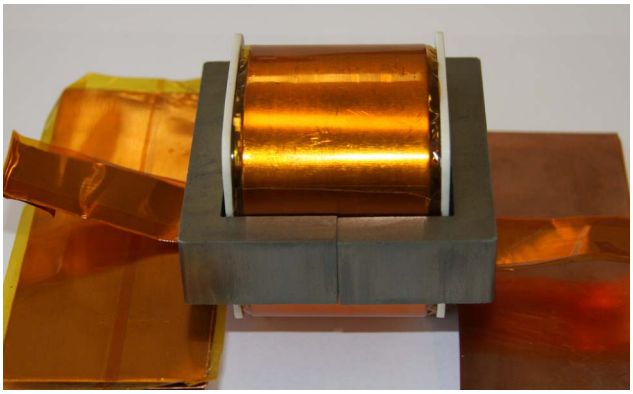

Fig. 6 Prototype 350 A boost inductor used in the 10 kW converter.

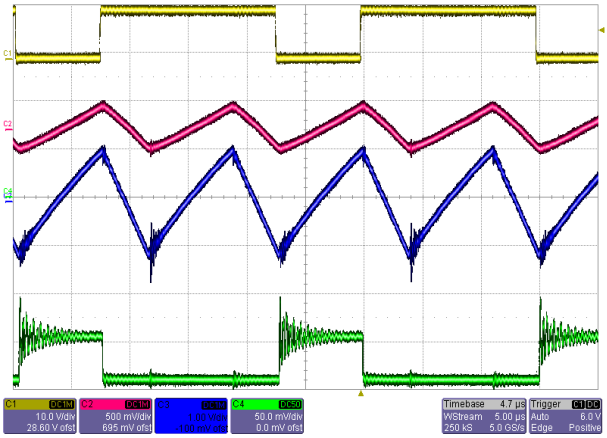

Fig. 7. From top: Control signal, Main dc-winding ac current 25A/div, Auxiliary ac-winding ac current 20A/div, primary switch voltage 50 V/div.

The low impedance ac or auxiliary winding W2, with five turns, was made of 0.1 mm x 45 mm copper foil, and was placed inner most close to the centre leg of the core. Outside this ac winding, the main dc-winding was placed. The dc-winding W1, has five turns, each consisting of 6 layers of 0.5 mm x 45 mm copper foil. The ac inner and dc outer windings were interconnected at the winding terminals.

Once the inductor with two windings was built, as shown in Fig. 6, and tested on its own, it was integrated into the 10 kW fuel cell boost converter, shown in Fig. 1. At full output power and minimum input voltage, ripple currents in both windings were measured using two Rogowski current probes, and the results are shown in Fig. 7. It can be noted that the winding currents are almost triangular, with only minor deviation. The peak-to-peak current ripple in the main winding Δi_{W1}, is 22 $A_{P\text{-}P}$. The ripple current in the auxiliary winding Δi_{W2}, is 45 $A_{P\text{-}P}$.

For the built prototype inductor with two windings, the penetration depth of the copper at 90 kHz and 60 ^{0}C is 0.24

mm, and the total lengths of the dc and ac winding foils are 0.83 m and 0.50 m, respectively. If only a single winding is considered, then the total length of the foil would be approximately 0.83 m.

The dc input current at 30 V input and 10 kW output is 345 A. Using (1) the inductor dc winding losses at 60 ºC is

$$P_{W,dc} = \frac{\rho_c \, l_w}{A} I_{dc}^2 = 13.4\ W \qquad (10)$$

A single winding inductor L1, on the same core, will have 5 turns of 3.1 mm height and a total length of 0.83 m. The ripple current will be 67 $A_{P\text{-}P}$. Using (2) and obtaining the effective resistance factor K_r, from the curve in Fig. 2, we get the ac winding losses for a single winding inductor

$$P_{W,L1,ac} = K_r(L1) R_w^* \left(\frac{\Delta i_{L1}}{2\sqrt{3}}\right)^2 = 9.3\ W. \qquad (11)$$

The total winding loss of the single winding inductor is thus 22.7 W.

The two-winding inductor will have the same dc winding losses, but the ac winding losses will be the sum of the two winding losses. Using the measured ripple currents in each winding (Fig. 7.) and the K_r value for each winding, the winding ac losses for the main winding W2, and the auxiliary winding W2, can be calculated.

$$P_{W1,ac} = K_r(W1) R_w^* \left(\frac{\Delta i_{W1}}{2\sqrt{3}}\right)^2 = 1.05\ W \qquad (12)$$

$$P_{W2,ac} = K_r(W2) R_w^* \left(\frac{\Delta i_{W2}}{2\sqrt{3}}\right)^2 = 0.41\ W \qquad (13)$$

The total winding ac losses is thus reduced from 9.3 W in the single winding inductor to only 1.46 W in the two-winding inductor, corresponding to an 84 % reduction in ac winding losses. The total winding losses are reduced from 22.7 W in the single winding inductor to 14.9 W in the two-winding inductor corresponding to only 0.15 % loss of efficiency.

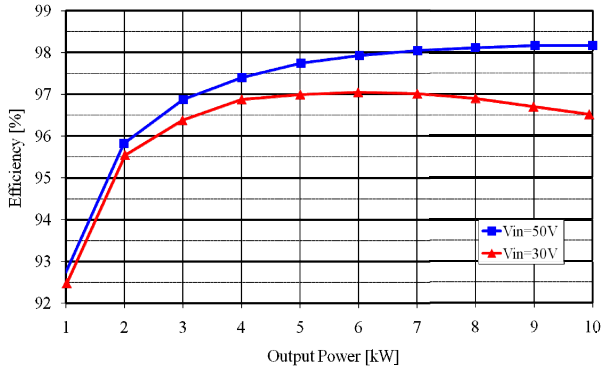

Fig. 8 Measured efficiency of prototype 10 kW isolated Boost converter

V. Conclusion

A very simple and efficient method to achieve a very significant reduction in ac winding losses in high-current high-power storage inductors has been presented. The technique steers the ac ripple current into an optimally designed inner auxiliary winding, which has a much lower ac resistance, and the dc current mainly into an outer main winding, ensuring low dc losses. The current sharing between the two windings can be controlled by the relative magnitudes of the ac impedances of the windings. Test results of a prototype 350A inductor, used in a 10 kW fuel cell dc-dc converter, have been presented to verify both the design and theoretical analysis. The method enables scaling of storage inductors to much higher current and power levels without sacrificing the efficiency of the converter.

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Appendix A5

M. Nymand, M. A. E. Andersen, "New primary-parallel boost converter for high-power high-gain applications," in *Proc. IEEE APEC,* Washington, USA, 2009, pp. 35-39.

New Primary-Parallel Boost Converter for High-Power High-Gain Applications

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***Abstract*—A new simple and low cost method for paralleling multiple power stages in high-power high-gain isolated full-bridge boost converters is presented. A small current balancing transformer and serial connection of transformer secondary windings provides ideal current sharing between paralleled power stages. Effective and safe parallel operation of multiple switching stages can thus be performed. By splitting high-current ac-loops into multiple smaller loops of smaller ac-currents, switching losses are reduced. Transformer turns ratio and power level is reduced, simplifying transformer design and manufacturing. Extension of the principle to other isolated boost converter topologies are demonstrated as well as extension to higher numbers of parallel operated power stages. Test results from a 3 kW experimental prototype converter are presented, verifying converter operation and demonstrating current sharing capability. Very high converter efficiency is achieved. Worst case efficiency at minimum input voltage and maximum power is 96.9 %. Maximum efficiency is 98 %.**

I. INTRODUCTION

Distributed generation systems, back-up systems or traction systems based on fuel cells or batteries, requires high-power high-gain dc-dc converters to boost the low source voltage (30-60 V) to a higher dc-link voltage (350-400 V). For safety or EMC reasons, transformer isolation are often required or preferred.

As power levels increase, input currents quickly reach levels where paralleling of primary switches become necessary. Since transistors are often operated close to their maximum drain current rating, direct paralleling of MOSFET's may require screening and parameter matching of on-resistance, gain and/or threshold voltages. Slowing switching speed by increasing gate impedance or addition of source inductance may also be required [1].

Variation in device avalanche voltage will cause all currents, in parallel connected unclamped power MOSFETs, to flow into the device having the lowest avalanche voltage, thereby potentially overstressing the device [2].

Full- or partial paralleling of converters in order to share primary current among paralleled branches can be an attractive alternative [3-8]. Cost of screening and matching is saved and converter efficiency is not sacrificed by reduced switching speed.

Power dissipation is distributed among several smaller components providing improved thermal management. Lower currents and smaller size components simplify interconnecting wiring and reduce size of ac-current loops thus reducing switching times and losses.

Lower power converters generally allow operation at higher switching frequencies thereby further reducing overall size. Standard components and assembly technologies can be utilized, taking advantages of cost savings from mass production.

Disadvantage of paralleling converters, is clearly the potential increase in number of components required and the associated increase in cost and complexity. The challenge is therefore to find solutions that best balance the advantage of paralleling high-ac-current circuit parts against the need to keep total cost and complexity at a minimum.

In recent years, several approaches to scaling converter power level by paralleling have been proposed. A three phase full-bridge buck type topology (V6) is presented in [3-5]. Three phase-shift controlled full-bridge converters are interleaved on primary side. Secondary windings are Y-connected and fed to a common three phase bridge rectifier. In [6] multiple phase-shift controlled full-bridge converters are interleaved by means of variable phase-shift control.

Interleaving of isolated boost converters are suggested in [7]. Single ended isolated boost converters in a primary-parallel-secondary-series structure are presented in [8].

The isolated full-bridge boost converter in fig. 1, has demonstrated very high conversion efficiencies in the range of 97-98 % in high-power high-gain applications [9].

The purpose of this paper is to present a new, simple and low cost method to extend power level in isolated boost converters by means of minimum paralleling of critical high-ac-current circuit parts.

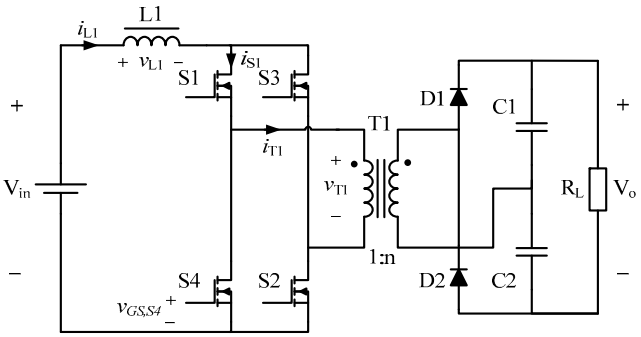

Figure 1. Isolated full-bridge boost converter.

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II. PROPOSED CONVERTER

Boost type topologies, with their inherent low input current ripple (continuous input current), requires only limited additional filtering of input ripple current in high-power fuel cell and battery powered applications. Further, having the high ripple current content (discontinuous current) on the high voltage output side, also output filter size is quite small.

In buck derived converters for high-power fuel cell applications, input ripple current are much higher requiring much larger input filters. When scaling buck derived converter topologies for higher power levels by paralleling converter stages, a common approach to reduce magnitude of input ripple, is thus to employ interleaving techniques [3-6]. However, interleaving of converters requires duplication of all converter functions including inductors and rectifiers, as well as independent current control of each converter stage in order to guarantee current sharing in continuous inductor conduction mode (CCM).

A potential cost saving therefore exist in boost type converters, since scaling of power level by means of parallel operation of power stages does not necessary require use of interleaving technique to reduce input ripple current. Partial paralleling of boost type converters, only duplicating high-stress-parts, is a low cost option to paralleling of full converters.

The proposed converter is presented in fig. 2. The converter is a hard switched full-bridge isolated boost converter with paralleled primaries. Two transformers T1, T2, operate in parallel on primary side and in series on secondary side. A single common rectifier stage D1-D4, rectifies all output power.

Switches S1-S4, drive primary winding of transformer T1, and switches S5-S8 drive transformer T2. The two bridges are driven synchronously and in-phase using the same control signals but with individual driver stages. The series connected transformer secondaries in combination with a small current balancing transformer T3, effectively split the inductor L1, current i_{L1}, into two equally sized continuous currents i_{P1}, i_{P2}, for each of the full-bridge primaries.

The current balancing transformer T3, absorbs any differential voltages between the two parallel branches caused by mismatches in switch transistor parameters, transformer- and circuit impedances or differences in driver delay times. Current sharing between all primary switches is thus guaranteed.

Any need for selection and parameter matching of primary switches or slowing of switching speed to guarantee current sharing between switches is therefore eliminated. Also during unclamped inductive switching, avalanche currents are shared between switches. Finally, keeping transformer primary currents equal under all operating conditions, avoids primary side clamping losses due to differences in currents.

The converter has a minimum degree of paralleling; only high-current ac-loops are paralleled i.e. primary switches and transformers. This paralleling effectively split the primary side high-current ac-loop into two smaller loops with only half the switching currents, thereby reducing current switching times and losses.

All control and protection circuits, output rectifiers, input and output filters etc. are common to both branches, significantly reducing cost. Transformer turns ratio is reduced by a factor two, simplifying transformer design and manufacturing.

Basic converter operating waveforms are presented in fig. 3.

Converter steady state transfer function is:

$$\frac{V_o}{V_{in}} = \frac{n}{1-D} \tag{1}$$

The principle can be readily applied to other isolated boost converter topologies, such as push-pull boost, two-inductor boost or even single ended boost converters. A primary-parallel isolated two-inductor boost converter is presented in fig. 4.

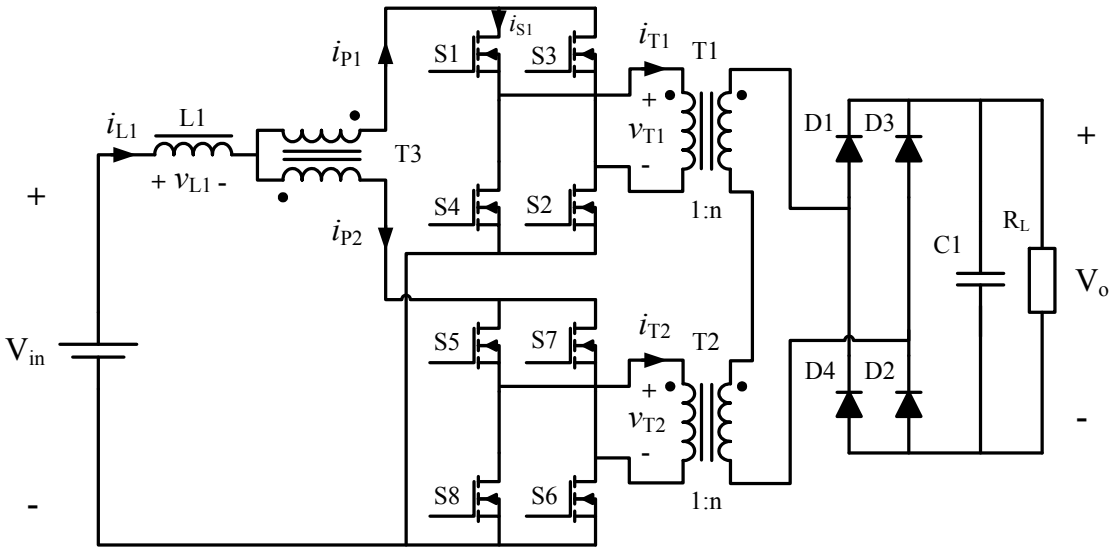

Figure 2. New primary-parallel isolated full-bridge boost converter.

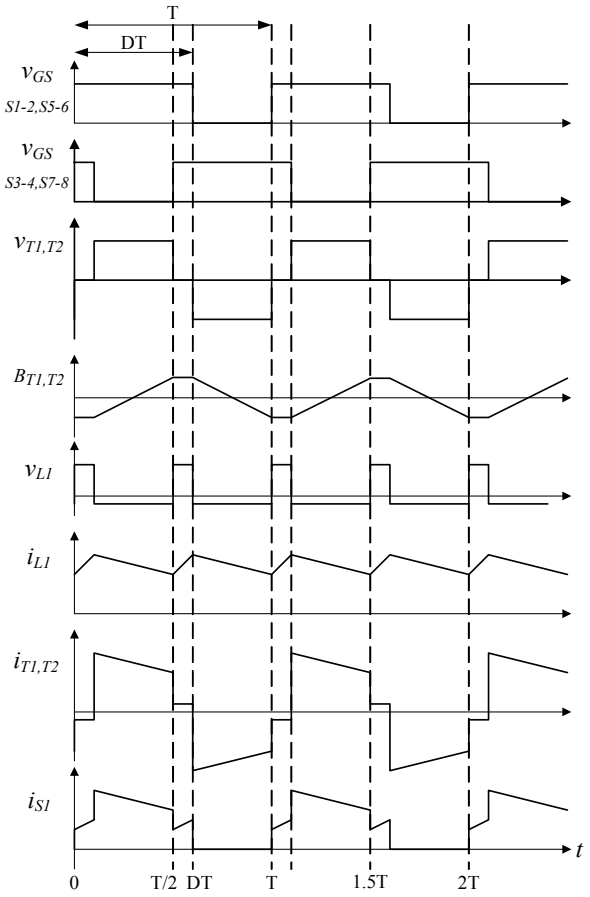

Fig.3. Basic converter waveforms.

Extension to higher numbers of paralleled converters is possible by adding an extra current transformer for each extra paralleled power stage. For even numbers of paralleled power stages, the current transformer turns ratio should be 1:1. For odd numbers of paralleled power stages, one current transformer needs to have a turns ratio of 2:1, with the winding having the higher turns number supplying the extra odd number power stage.

Inductor and current transformer configuration for a 3-paralleled power stage converter is shown in fig. 5. Fig. 6, show the configuration for a 4-paralleled power stage converter. In general, N-1 current balancing transformers are needed for paralleling N power stages.

III. Experimental verification

A 3 kW experimental prototype converter was designed, built and tested to verify operation of the converter and demonstrate achievable efficiency. Input voltage range is 30-50 V and output voltage is 360-400 V.

Primary switches S1-S8, are 75 V, 3.3 mΩ avalanche rated MOSFET devices rated at 75 A maximum (International Rectifier IRFB3077). Rectifier diodes D1-D4, are 600 V, 12 A SiC Schottky diodes (Infineon IDT12S60C).

Transformers T1, T2, use E55 cores in N87 material. Turns ratio is 1:4 (n=4). A Magnetics Kool Mμ E core (00K5528E060) is used for the storage inductor L1. Transformer T3, core is a planar EELP32. Copper foil windings are used for all transformer and inductor windings. Extensive interleaving of transformer windings is used to decrease ac-resistances and leakage inductances. Switching frequency is 45 kHz, with input- and output

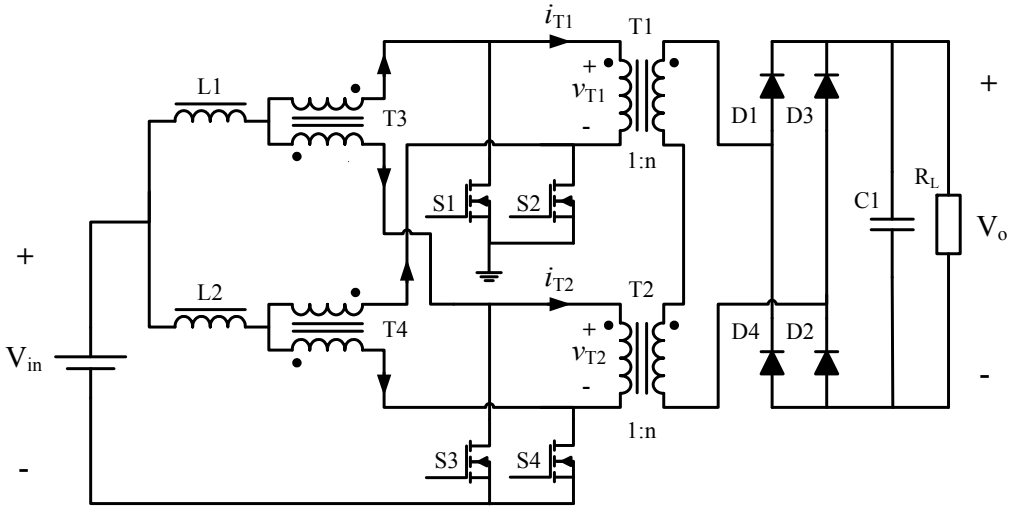

Figure 4. New primary-parallel isolated two-inductor boost converter.

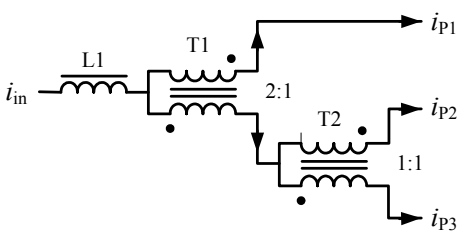

Figure 5. Inductor and current balancing transformer arrangement for three parallel power stages.

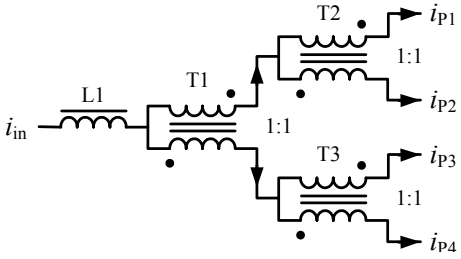

Figure 6. Inductor and current balancing transformer arrangement for four parallel power stages.

ripple at 90 kHz.

Low leakage inductance design of transformers and the use of avalanche rated switches allow primary voltage clamp circuits to be eliminated and voltage rating of primary switches to be reduced significantly. Thus, very significant reductions in conduction losses are achieved, resulting in very high conversion efficiency [9].

Oscilloscope plots of the two primary currents i_{P1} and i_{P2}, and switch S4 drain-source voltage is shown in fig. 7. Observe that the two currents are identical. Removing oscilloscope offset, causes current traces to fully coincide.

In fig. 8, measured primary currents of transformer T1 and T2 are shown together with drain-source voltage and gate-source voltage of transistor S1.

Measured diode D1, current and voltage together with transformer secondary current are shown in fig. 9.

Notice that diode reverse voltage is well clamped to output voltage effectively limiting diode voltage stress. Also notice that since magnetizing current in transformer T1 and T2 is only approx. 6 % of maximum load current, primary- and secondary currents are almost identical.

Converter efficiency measurements, including drive power, are presented in fig. 10. Worst case efficiency, at minimum input voltage and maximum load, is 96.9 %. Maximum efficiency is 98 %.

Efficiency measurements in the 97-98 % range are not trivial. Great care has been taken to ensure very high precision of the efficiency measurements. High stability (< 10 ppm) 0.1 % shunt resistors were used. Agilent 34410A high precision multimeters were used for all measurements. Current sense signals were shielded and fitted with common mode filters. Measurement tolerance of the critical output-to-input current ratio I_o/I_{in}, was verified by serial connecting current sensors and checking measurement results against the ideal sensor ratio. Measured error in current ratio was less than 0.01 %. Tolerance of efficiency measurements was less than +/- 0.1 %.

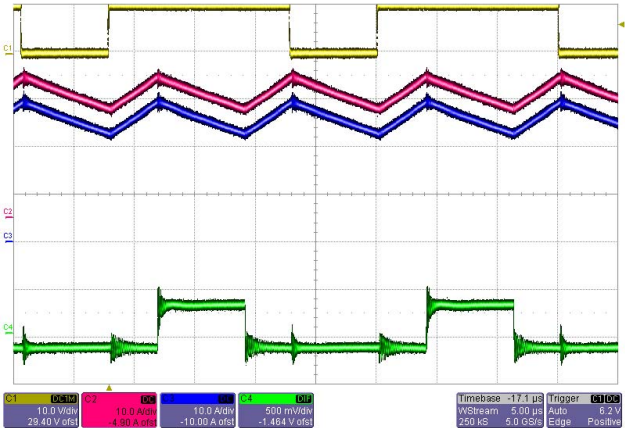

Figure 7. Measured converter waveforms at 30 V input. From top: drive signal for S1-2, S56, primary current i_{P1}(10 A/div), primary current i_{P2} (10 A/div) and bottom trace is S4 drain-source voltage (50 V/div). Time base is 5 µs/div.

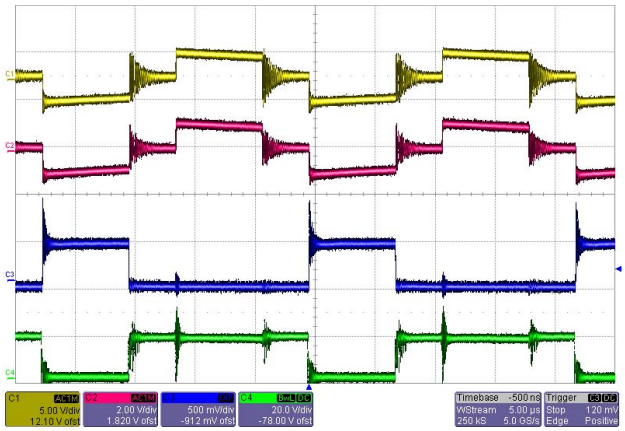

Figure 8. Measured converter waveforms at 30 V input and 2.8 kW output. From top: Transformer T1, primary current (100 A/div), Transformer T2, primary current (100 A/div), S1 drain-source voltage (50 V/div) and bottom trace is Si, gate-source voltage. Time base is 5 µs/div.

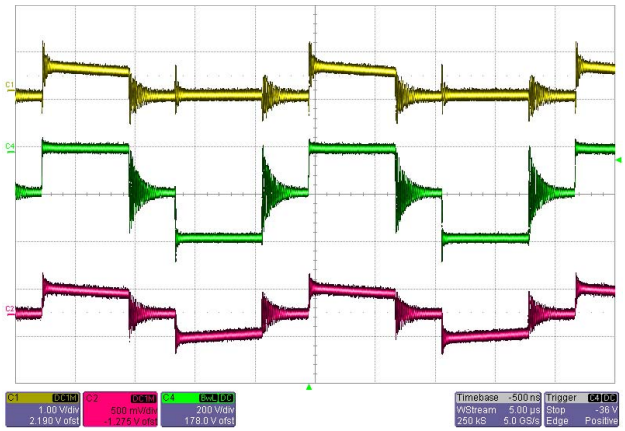

Figure 9. Measured converter waveforms at 30 V input and 2.8 kW output. From top: Diode D1, current (20 A/div), Diode D1, voltage (200 V/div) and bottom trace is transformer secondary current (25 A/div). Time base is 5 µs/div.

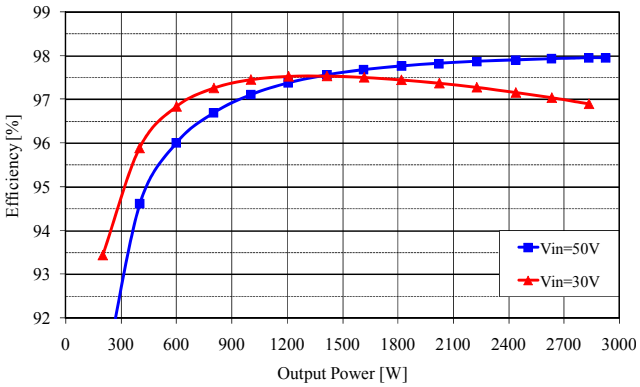

Figure 10. Measured converter efficiency including drive power.

Table 1, is a detailed break-down of power losses at 30 V input and 3 kW output power. Notice that switching losses are very small; more than 70 % of all losses are conduction losses.

The current balancing transformer is depicted in fig. 11-12. The two windings each has one turn of two interleaved cobber layers on a planar EELP32 core. Before assembly, windings are insulated using Kapton tape.

Fig. 13, is photo of the 3 kW experimental prototype converter.

TABLE I.
CONVERTER POWER LOSS BREAK DOWN AT 3 KW / 30 V

Component	Loss type	Loss [W]	Total [W]
MOSFET 8 pcs. IRFB 3077	Conduction	28.2	37.6
	Capacitive	0.54	
	Drive	1.44	
	Inductive clamp	7.5	
Diodes 4 pcs. IDT12S60C	Conduction	29.4	30.2
	Capacitive	0.82	
Transformer 2 pcs. E55 N87	Conduction	7.54	11.0
	Core	3.5	
Inductor 1 pcs. Kool Mμ E core 00K5528E060	Conduction	5.5	7.0
	Core	1.5	
Misc. others	Wiring, ac-resistance etc.		14.4
Converter	Measured		100,2

IV. CONCLUSION

A new method for extending power levels in high-power high-gain isolated boost converters has been presented. A minimum amount of paralleling is utilized to allow safe and efficient parallel operation of multiple primary switching bridge-stages.

Current switching losses are reduced by splitting primary side high-current ac-loops into multiple smaller loops with only fractional switching currents.

Small current balancing transformers in combination with serial connected transformer secondary windings, guarantee current sharing in all switch transistors.

Selection and matching of switch transistors are therefore not required and avalanche operation can be utilized without risk of switch overstress.

Transformer turns ratio is reduced by the number of parallel operated transformers. Paralleling of smaller power transformers significantly simplify transformer and converter design and manufacturing.

Test results from a 3 kW experimental prototype verify converter operation and demonstrate ideal current sharing capability. Very high converter efficiency is achieved. Worst case efficiency at minimum input voltage and maximum power is 96.9 %. Maximum efficiency is 98 %.

Low complexity, low cost and very high conversion efficiency makes the proposed converter an optimum choice for high-power high-gain converter applications.

Figure 11.Disassembled current balancing transformer T3.

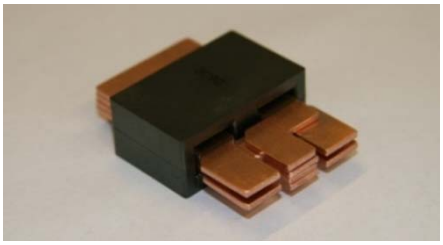

Figure 12. Assembled current balancing transformer T3.

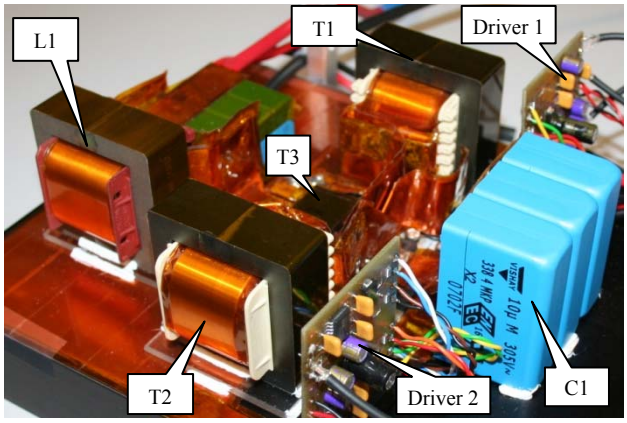

Figure 13. Photo of 3 kW experimental prototype converter.

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Appendix A6

M. Nymand, M. A. E. Andersen, "A new very-high-efficiency R4 converter for high-power fuel cell applications," in *Proc. PEDS*, Taipei, Taiwan, 2009*,* pp. 997-1001.

A New Very-High-Efficiency R4 Converter for High-Power Fuel Cell Applications

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***Abstract* -- A new very high efficiency 10 kW isolated R4 boost converter for low-voltage high-power fuel cell applications is presented. Using a new concept for partially paralleling of isolated boost converters, only the critical high ac-current parts are paralleled. Four 2.5 kW power stages, consisting of full-bridge switching stages and power transformers, operate in parallel on primary side and in series on secondary side. Current sharing is guaranteed by series connection of transformer secondary windings and three small cascaded current balancing transformers on primary side. The detailed design of a 10 kW prototype converter is presented. Input voltage range is 30-60 V and output voltage is 800 V. Test results, including voltage- and current waveforms and efficiency measurements, are presented. A record high converter efficiency of 98.2 % is achieved. The proposed R4 boost converter thus constitutes a low cost solution to achieve very high conversion efficiency in high input current applications.**

***Index Terms*—Current transformers, fuel cell power system, power electronics, pulse width modulation, switched mode power supply.**

INTRODUCTION

In high power fuel cell based systems such as in three phase UPS systems and fuel cell electrical vehicles, primary currents of many hundreds of amperes (2-400 A) at low input voltage (30-60 V) need to be converted to high output voltage compatible with the three phase grid (7-800 V) [1-2]. Achieving high conversion efficiency at lower power levels with input currents in the range of 50 A is a challenge, but to maintain this efficiency at much higher input currents is even harder. Controlling ac-resistances and parasitic inductances in interconnections and switches becomes increasingly difficult. An obvious alternative to making one large converter is to simply parallel several smaller ones, however due to the required duplication of all components this comes at a higher cost.

Three different solutions to a 5 kW output, 22 V input converter (>200 A input current) have been presented in [3-5]. In [3], a buck derived full bridge with two transformers and rectifiers are reported to achieve 90 % efficiency. Another buck derived full bridge [4]; the V6, is reported to achieve an excellent efficiency of 97 %. In [5], a full bridge Boost converter achieves a peak efficiency of 94 %. Analysis of a 10-20 kW single stage boost converter for higher input voltage (1-200 V) is presented in [6]. A 3 kW bidirectional boost converter for boosting 12 V battery voltage to 250-420 V output is presented in [7]. Peak efficiency of 93 % is reached at maximum input voltage (15 V). At the minimum input voltage of only 8.5 V input current reaches 350 A and efficiency drops to approximately 80 %. From the above it is clear that maintaining high efficiency in low-input-voltage high-power converters becomes a significant challenge at input currents above approximately 1-200 A.

A design approach to achieve very high efficiency in low input voltage isolated boost converters is presented in [8]. By careful design of transformer and circuit lay-out, very low parasitic circuit inductances can be achieved allowing traditional clamp circuits to be eliminated. Without the need to accommodate clamp circuit voltages, primary switch voltage rating can be reduced significantly, dramatically reducing switch conduction losses. Using the design approach of [8] and a new partial paralleling method [9], this paper presents a new 10 kW converter for 30-50 V input and 7-800 V output, having input currents up to 345 A.

Test results confirm converter operation and demonstrate that very high conversion efficiency can be achieved by a simple and low cost converter topology. Measured peak efficiency of the prototype converter is 98.2 %.

PROPOSED CONVERTER

The proposed converter is presented in fig. 1. Four power stages, each consisting of a full bridge switching arrangement driving the primary winding of a power transformer, work in parallel on primary side and in series on secondary side. All 4 power stages are driven in synchronism using the same two phase shifted control signals. Switches S1-S2, S5-S6, S9-S10 and S13-S14 are all controlled by the same duty cycle signal with a duty cycle D, of more than 50 %. Similarly switches S3-S4, S7-S8, S11-S12 and S15-S16 are all controlled by the 180 degree phase shifted PWM signal. During the overlap period (D>50 %) input inductor L1, is charged. During transistor off-time, energy is transferred to output through the opposite phase transistors.

The series connected secondary windings, force transformer currents to be identical during energy transfer cycles thus also guaranteeing current sharing between all active switches. During inductor charging, when all switches are turned on, the current sharing between primary switches

are maintained by the cascaded current balancing transformers CT1-CT3. Small difference in switch on-resistance, circuit impedances, switching speed and driver delays accumulates into differential volt-time integrals between parallel coupled power stages. A direct paralleling of such power stages, having low parasitic stray inductances, would lead to unpredictable current distribution between switches and potentially catastrophic failures.

By representing a large circuit inductance towards differential currents between power stages, the current balancing transformers CT1-CT3, absorb any such differential volt-time products between power stages thus effectively separating power stages and maintaining current sharing between switches. Since imbalances between power stages are fairly small, the volt-time product required to be blocked by the current balancing transformers is correspondingly small, thus requiring only very small current balancing transformers. Thus added cost of introducing current balancing transformers is minimal.

Output voltage is rectified by a single common full bridge rectifier D1-D4, followed by a common output capacitor C2. Since input ripple current in Boost converters is very small, only a small additional input capacitor C1, is required to fully attenuate input side ripple current. Seen from a control point of view, the converter behaves like a single large isolated full-bridge Boost converter. Hence a single common current controller is sufficient to control the complete converter.

The need to parallel primary switches to handle higher power levels, are thus fully utilized in this converter architecture to reduce ac-current magnitudes and size of ac-current carrying loops. Physically smaller ac current loops will exhibit smaller stray inductances and ac resistances. Smaller ac current magnitudes and lower stray inductances leads to much faster current switching and thus much lower switching losses. Similarly, lower ac-current levels and ac resistance levels greatly reduce conduction losses. The separation of the critical high-ac-current-loop into smaller parallel ac-current loops, thus allows this converter to operate at much higher switching frequency while achieving much higher conversion efficiency. Finally, transformer turns ratio (and size) is reduced by a factor of 4, greatly simplifying transformer design and manufacturing.

Inspired by the line-placement of cylinders in a row-4-cylinder internal combustion engine, this converter topology is called an R4 Boost converter.

The converter steady state transfer function is given by:

$$\frac{V_o}{V_{in}} = \frac{2n}{1-D} \tag{1}$$

Where D is the conduction duty cycle of the primary switches and n is the transformer turns ratio N_S/N_P.

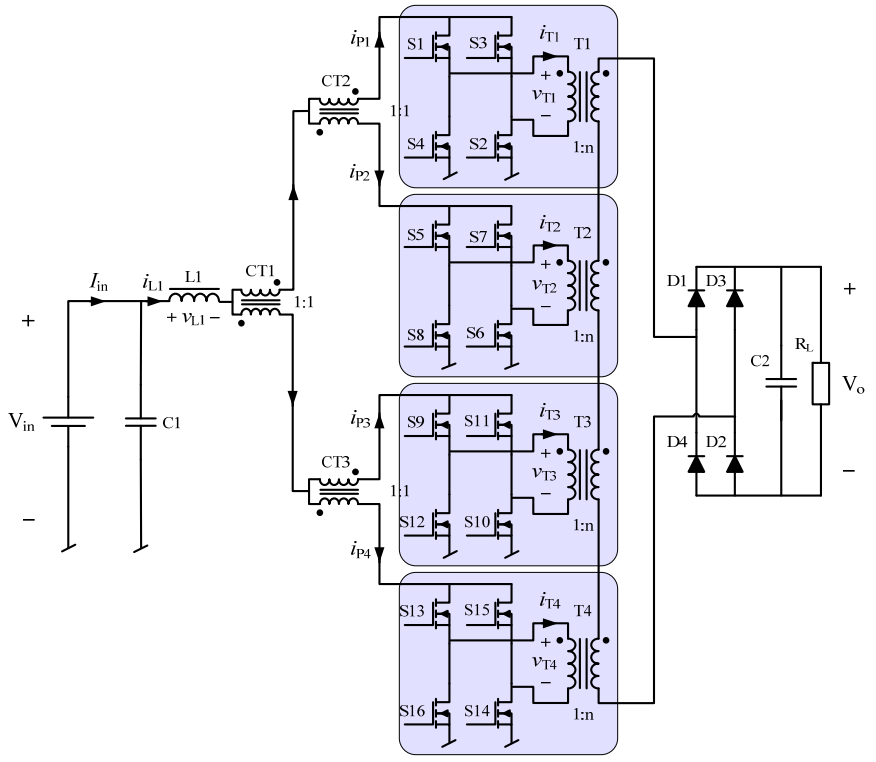

Fig. 1. Proposed R4 isolated Boost converter.

EXPERIMENTAL VERIFICATION

To verify the theoretical design, a 10 kW experimental prototype converter was designed, built and tested. Input voltage range is 30-50 V with start-up transients up to 60 V, output voltage is 700-800 V.

Primary switches S1-S16, are 1.46 mΩ, 75 V power MOSFETs (IRFP4368) from International Rectifiers. Output diodes D1-D4, are 1200 V Silicon Carbide (SiC) Schottky diodes (C2D20120D) from CREE. Switching frequency is 45 kHz with input and output ripple of 90 kHz. The 4 power transformers T1-T4, are made on EE65 cores in N87 material and have a turns ratio of 1:4. The input inductor L1, is made on a EE80 CoolMμ core from Magnetics. Output capacitors are 8 pcs. (4+4) MKP 3,3 μF/630 V and the input capacitors are 6 pcs. MKT 22 μF/100 V capacitors in parallel.

In the design and construction of the converter extreme care has been taken to limit parasitic stray inductances and ac-resistances in the circuit. Transformer windings are heavily interleaved using foil windings. Conductors and interconnections are made as short as possible and using wide foil conductors in close proximity to the return path.

Using a precision impedance analyzer (Agilent 4294A), the transformer leakage inductance and ac resistance were measured referenced to secondary side, fig. 2. Referenced to primary side, transformer leakage inductance is 10.4 nH and ac resistance is 0.93 mΩ at the switching frequency of 45 kHz.

Converter switching waveforms at minimum input voltage and maximum power (30 V, 10 kW) are shown in fig. 3. Fig. 4, is a detailed view of the transistor S3 turn-on sequence. Apart from discharging of internal parasitic capacitances, there are no turn-on losses. Fig. 5 is a detailed view of the transistor S3 turn-off sequence. Switching time is approximately 130 ns with significant overlap of voltage and current, primarily caused by current switching speed being limited by common source stray inductance. Compared to the 30 ns switching time achieved in the 1.5 kW converter presented in [8], this is a significant increase in turn-off losses. This increase in switching time demonstrates the criticality and poor scalability of high-frequency high-current switching thus clearly demonstrating the advantage of dividing large switching ac-current loops into multiple smaller loops.

Measured efficiency of the 10 kW prototype converter is presented in fig. 6. Efficiency measurements are made using high precision multimeters and 0.1 % tolerance current shunts with only 1 ppm temperature coefficient. Transistor drive power (>6 W) is included in the measurements. Although starting to exhibit increased switching losses, this converter still achieves an outstanding peak efficiency of 98.2 %.

The current balancing transformers CT1-CT3 are shown on fig. 7, and fig. 8, before and after preparation for mounting. Fig. 9, is a photo of the complete 10 kW prototype converter.

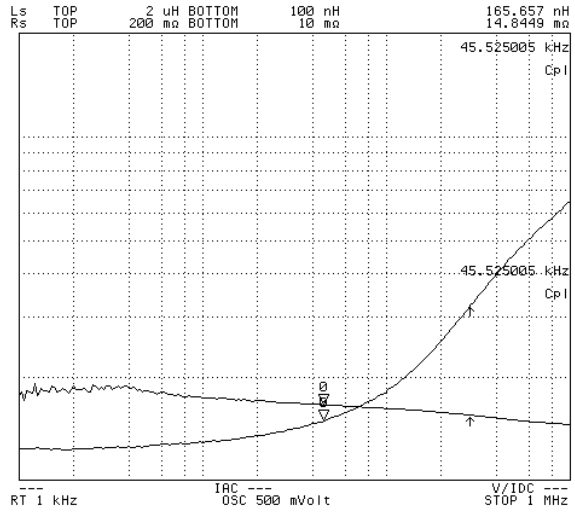

Fig. 2. Measured transformer secondary leakage inductance and ac resistance.

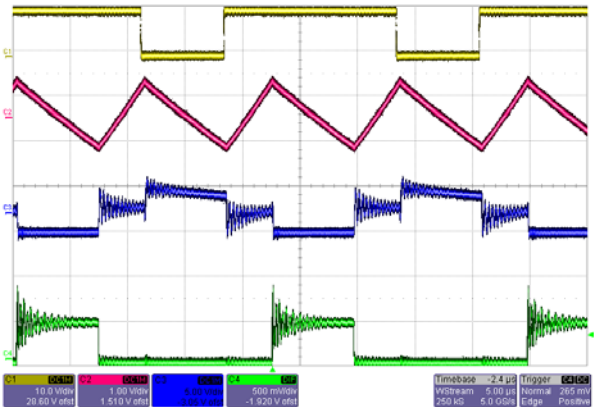

Fig. 3. Measured converter waveforms at 30 V input and 10 kW output. From top: switch drive signal, inductor L1 ac-current (50A/div), switch S3 current (100A/div) and switch S3 drain-source voltage (50V/div). Time base is 5μs/div.

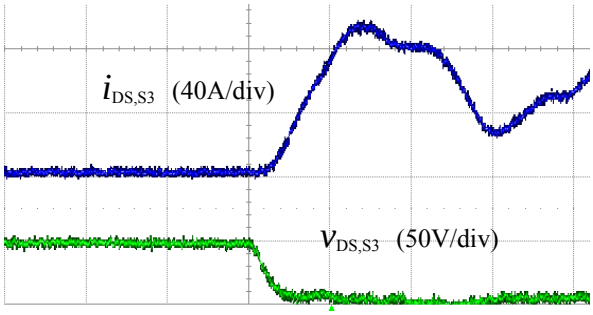

Fig. 4. Expanded view of fig. 3, showing switch S3 turn-on sequence. Time base is 100ns/div.

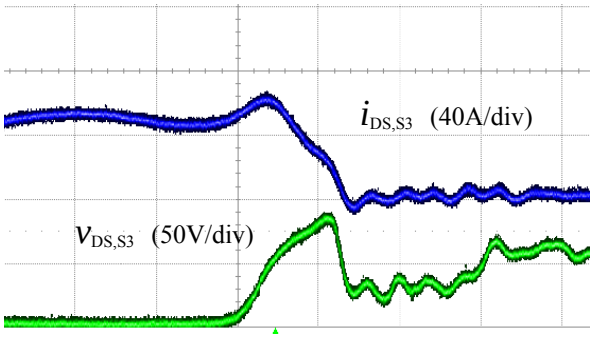

Fig. 5. Expanded view of fig. 3, showing switch S3 turn-off sequence. Time base is 100ns/div.

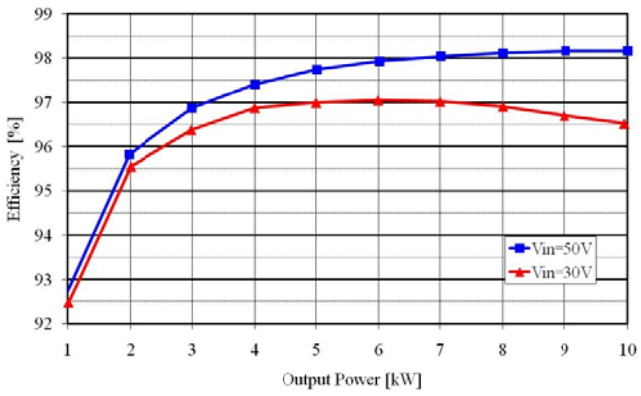

Fig. 6. Measured efficiency of 10 kW prototype converter.

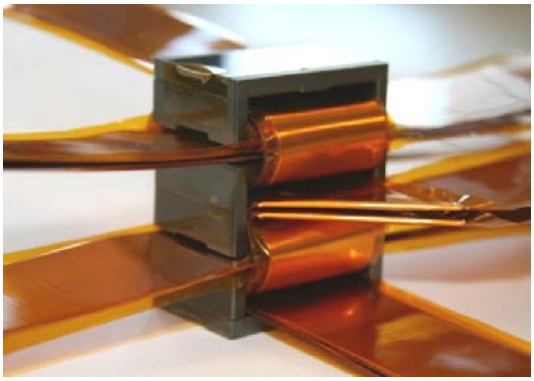

Fig. 7. Photo of 3 integrated current balancing transformer CT1-CT3.

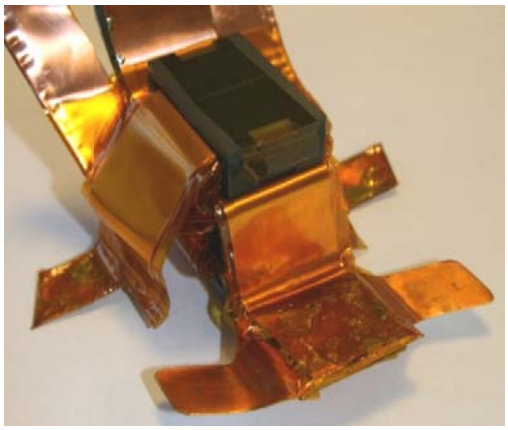

Fig. 8. Photo of current balancing transformers prepared for mounting.

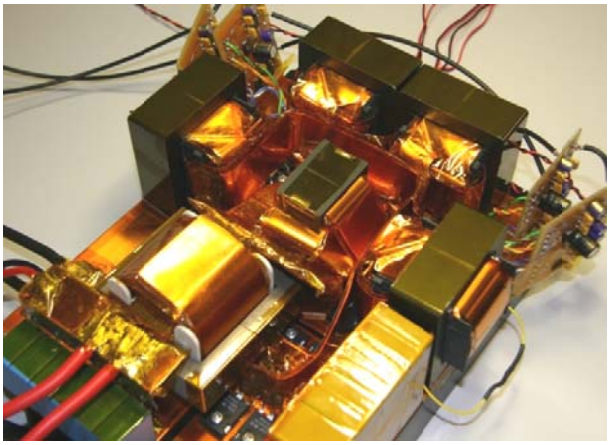

Fig. 9. Photo of 10 kW prototype converter.

CONCLUSION

A new principle for extending power levels in low input voltage converters for high power applications, such as seen in fuel cell powered three phase back-up systems or fuel cell electrical vehicles, has been presented. High switching frequency reduces size and power losses in passive components. Four power stages each consisting of a full-bridge switching stage and a power transformer, operate in parallel on primary side and in series on secondary side. Three small current balancing transformers ensure perfect current sharing between paralleled primary switches ensuring reliable, fast and efficient switching. By dividing the primary side high ac-current loop into multiple smaller loops, very significant increase in current switching speed is obtained thus achieving high efficiency high frequency switching. Furthermore, the use of multiple smaller transformers with much lower turns-ratio, greatly simplifies design and manufacturing of transformers. Limiting paralleling to an absolute minimum number of critical high-ac-current-components, thus leads to a simple, low cost and extremely efficient converter.

The design of a 10 kW prototype converter has been presented. Test results verify converter operation and demonstrate very high conversion efficiency at very high input currents. At minimum input voltage, peak efficiency reaches 97.1 %. Maximum efficiency is 98.2 %.

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Appendix A7

M. Nymand, “Switch mode pulse width modulated dc-dc converter with multiple power transformers,” WO/2009/012778, International Patent application PCT/DK2008/000274.

Title: Switch mode pulse width modulated DC-DC Converter with Multiple Power Transformers

The invention relates to a switch mode pulse width modulated dc-dc converter with multiple power transformers.

Switch mode converters are widely used for converting a given input electrical power to a desired output electrical power. The input power is provided from a source to the converter through input terminals on an input side, converted by the converter into the desired output power and then output through output terminals on an output side provided to a load. The converter comprises switching arrangements for modulating the input electrical power in time and for rectifying converted electrical power before it is provided to the output terminals. The switches employed in such switching arrangements are typically provided as solid state switches, such as MOS-FET transistors employed in the modulating input switching arrangements, or diodes employed in the rectifying output switching arrangements.

The switches are activated by means of a control circuit controlling the time, frequency and/or duty cycle of the switches in the switching arrangements to assume an ON-state (switch closed) or an OFF-state (switch open). For example, in the case of MOSFET switches, the control circuit is adapted to provide a gate voltage to switch the source-drain conduction channel ON (conducting) or OFF (non-conducting) in a timed manner. A rectifying diode may also be implemented by a three-terminal device, such as a MOSFET, by operating the control circuit driving the three-terminal device in a synchronous rectification mode.

The dc-dc converter may be a boost-type converter converting an input voltage to a higher output voltage. For a given amount of electrical power transferred from the input to the output this means in particular that the input side needs to be adapted to handle large currents.

The dc-dc converter may be a buck-type converter converting an input voltage to a lower output voltage. For a given amount of electrical power transferred from the input to the output this means in particular that the output side needs to be adapted to handle large currents.

The converter may be configured as a bi-directional converter adapted to be operated in both directions, i.e. where terminals interchangeably can be operated as input or output terminals.

The converter is an isolated converter, where input and output are galvanically isolated from each other. A galvanic isolation is achieved by employing power transformers for transferring the electrical power from the input side to the output side.

An example of a high power application of dc-dc converters is the conversion of electrical power provided by fuel-cells in the form of high current at low voltages into a high voltage output. Due to the large currents involved in such a conversion, the components of the converter circuit are subjected to considerable current and voltage "stress". In a converter of the known type, components with large physical dimensions may be required to handle the large currents, with increased inductive losses as a consequence. In addition to the reduction in conversion efficiency, excessive heat dissipation may lead to a need for additional cooling and may severely limit the power rating of a converter.

Furthermore, the leakage inductance in converter circuits, in particular that associated with the switching components and associated connecting leads, tends to increase with the power converted. In particular, the circuit handling the lower voltage, and therefore the higher current, is affected by the leakage.

A way to overcome this problem is by operating a number of converters in parallel. Alternatively, the circuit handling the high currents may be split into a number of stages operating in parallel and the terminals of the circuit handling high voltages may be connected in series.

US patent application no. 6,297,616 discloses a charge and discharge apparatus for electric power storage means. The apparatus comprises an AC power source and a transforming apparatus with a first side and a second side. One of the two sides comprises a number of parallel full bridges converters, which are driven with a constant 50 percent duty cycle. The apparatus further comprises a number of storage inductors, which are charged by leading current through two primary switches coupled in series and on through the primary windings and the secondary windings of the transforming apparatus and finally through two secondary switches.

A major disadvantage of the above approaches is the need for additional switching, rectifying and/or control units. Furthermore, considerable loss may be introduced due to differences between nominally identical components in the parallel stages. The differences between nominally identical components arise mostly from fabrication tolerances. These differences may be reduced to a certain degree by selecting higher quality components complying with smaller fabrication tolerances. However, this is a costly approach; in particular as these circuits themselves require a larger number of components.

The object of the present invention is to provide a converter reducing power conversion losses and overcoming the above mentioned problems by means of a simple converter arrangement.

This is achieved by a pulse width modulated switch mode DC-DC boost converter according to the invention comprising at least one first electronic circuit on a input side and a second electronic circuit on a output side, the input side and the output side being coupled via at least two power transformers, each power transformer comprising a first winding arranged in a input side converter stage on the input side and a second winding arranged in a output side converter stage on the output side, each of the windings having a first end and a second end. The first electronic circuit comprises terminals for connecting a source or a load, at least one energy storage inductor coupled in series with at least one of the first windings of the power transformers, and for each power transformer, an arrangement of switches being adapted to switch the current through the first winding between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state, wherein the at least one energy storage inductor is arranged so as to be charged, when all switches of the switching arrangements are conducting. The second electronic circuit comprises terminals for connecting a load or a source, and a single arrangement of switches being adapted to switch the current through the second windings of the power transformers between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state, and/or being adapted to provide rectified current to the terminals. The second windings of all power transformers are connected in series and coupled via the single arrangement of switches of the second circuit to the terminals of the output side.

The current flowing in the at least one first circuit on the input side is higher than the corresponding current in the second circuit on the output side. The current on the input side is therefore referred to as high current, while the current flowing on the output side is referred to as low current.

The arrangement of the first winding together with the corresponding switching arrangement on the input side is referred to as a input side converter stage. The arrangement of the second windings together with the single switching arrangement of the output side is referred to as output side converter stage.

The input side converter stages are connected to terminals for connecting a source or a load. In practice, the different input side converter stages are often connected to the same DC-source (or load) so as to operate in parallel.

Alternatively, different input side converter stages may be connected to different DC-sources (or loads), thereby operating independently as different first circuits. Furthermore, in an arrangement of more than one first circuit, it can be conceived that each of the first circuits comprises a number of input side converter stages connected in parallel.

The terminals in the first circuit may be connected to a source providing a high current (low voltage) source output. The high current to be handled on the input side is split up and distributed to separate input stages. In each input stage, the current is provided to the first winding through its corresponding switching arrangement adapted to control the current state in the first winding. By distributing the high current over at least two input side converter stages, the power handled by each of the input side converter stages is divided correspondingly, thereby reducing current stress on the individual switching components and losses due to parasitic impedances, such as leakage inductance and/or wiring resistance. The current is via the power transformers transferred to the output side output stage and via the terminals of the output side provided as rectified output current to a load. Since all second windings are coupled directly in series, the current through the second windings is clamped, thereby contributing to an equal current distribution between the input side input stages. Furthermore, only a single switching arrangement, here a common rectifier circuit, is required, thereby reducing circuit complexity and cost.

The at least one energy storage inductor is charged from the terminals of the input side, when all switches of the switching arrangements are conducting, and where no current is conducting through the second windings on the output side and/or where the arrangement of switches on the output side is blocking the current.

Charging of the energy storage inductor is stopped by rendering one or more of the switches in the switching arrangement non-conducting so as to disconnect at least one end of the energy storage inductor from the source. At the same time one or more switches in the switching arrangement are kept conducting so as to maintain a current path for transferring the energy stored in the at least one energy storage inductor to the at least one first winding.

A typical switching cycle of a converter according to the invention operated with input from the input side comprises four consecutive parts as associated with the state of the current through the at least one first winding:

- during the first OFF-state, the energy storage inductor is charged,

- during the first ON-state, the energy is transferred from the energy storage inductor to the at least one first winding by running a current in a first direction through the first winding,

- during the second OFF-state, the energy storage inductor is re-charged, and

- during the second ON-state the energy is transferred from the energy storage inductor to the at least one first winding by running a current in a second direction opposite to the first direction through the first winding.

The current pulses thus induced in the first windings of the power transformers are coupled to the corresponding second windings. The second windings are coupled directly in series, and therefore the current induced in the second windings is limited by the power transformer providing the smallest induced current, thereby clamping the currents in the other power transformers to an essentially equal distribution. An equal distribution reduces the risk for uneven stress on the components in the different converter stages on the input side, reducing the need for dimensioning of components to a large safety margin and thereby reducing production cost. The current pulses in the

second windings are rectified by the single switching arrangement of the second circuit and provided as low current rectified output via the terminals on the output side to a load.

A further advantage of the converter according to the invention is that the switching arrangements of different input side converter stages are typically operated in a synchronous manner in order to simultaneously provide essentially the same current state in all of the first windings of the input side converter stages. Therefore, a single control circuit is sufficient for driving all input side switching arrangements. This considerably simplifies the overhead circuitry for a converter according to the invention, thereby reducing production cost.

As mentioned, the at least one energy storage inductor is charged directly through the ,preferably four, primary switches. Thereby, the losses due to parasitic impedances corresponds to the impedance from one switch only. Thus, compared to US patent application no. 6,297,616, the present invention saves the losses from one primary switch, the primary and secondary windings of the transformation stage and two secondary switches.

Preferably, the pulse width modulated switch mode DC-DC boost converter is controlled via the arrangement of switches on the input side.

According to a first advantageous embodiment, the at least one energy storage inductor is coupled to or is part of a current-balancing electrical circuit. The current-balancing has been necessitated by the new converter topology in order to minimise losses from the converter. In practice, the current balancing according to the invention can be achieved in two ways, viz. by at least pair-wise magnetically coupling energy storing inductors on a common magnetic core so as to equalise their inductance, or by coupling the energy storage inductor in series with at least one current balancing transformer on the input side. These embodiments are described later.

The current balancing may also be utilised for buck converters. Therefore, according to another aspect, the invention provides: a pulse width modulated switch mode DC-DC buck converter comprising at least one first electronic circuit on a input side and a second electronic circuit on a output side, the input side and the output side being coupled via at least two power transformers, each power transformer comprising a first winding

arranged in a input side converter stage on the input side and a second winding arranged in a output side converter stage on the output side, each of the windings having a first end and a second end. The first electronic circuit comprises terminals for connecting a load or a source, and a single arrangement of switches being adapted to switch the current through the first winding between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state. The first windings of all power transformers are connected in series and coupled via the single arrangement of switches of the first circuit to the terminals of the input side. The second electronic circuit comprises terminals for connecting a source or a load, at least one energy storage inductor coupled in series with at least one of the second windings of the power transformers, and for each power transformer, an arrangement of switches being adapted to rectify current.

The at least one energy storage inductor is charged, when the current through the first winding is in the first ON-state and/or the second ON-state. Typically, this occurs when two of the switches on the input side are conducting. In one embodiment a first energy storage inductor is charged when two of the switches are conducting, and a second energy storage inductor is charged when two other switches are conducting.

According to a first advantageous embodiment of the buck converter, the at least one energy storage inductor is coupled to or is part of a current-balancing electrical circuit. In practice, the current balancing according to the invention can be achieved in two ways, viz. by at least pair-wise magnetically coupling energy storing inductors on a common magnetic core so as to equalise their inductance, or by coupling the energy storage inductor in series with at least one current balancing transformer on the output side. Thus, the methods described for current balancing the boost converter and the following described embodiments may also be used for the buck converter.

According to another advantageous embodiment, the arrangement of switches is adapted to switch the current through the first windings comprises two parallel coupled stages, each of the parallel coupled connections comprising a first switch serial connected to a second switch, and wherein the first end of the first winding is coupled to the serial connection of one of the two parallel coupled stages, and wherein the second end of the first winding is coupled to the serial connection of the other of the two parallel coupled stages.

According to one aspect of the invention, the converter is adapted for operation as a boost converter, wherein the input side converter stages are provided as modulating input stages and the output side converter stage is provided as a rectifying output stage.

In practice, the modulating input stages are – apart from fabrication tolerances – nominally identical, and the switching arrangements of the modulating input stages are typically equipped with solid state switches, such as MOSFETs having a source-terminal and a drain terminal connected to the source-terminal via a source-drain channel, as well as a gate terminal for switching the conductivity of the source-drain channel. The switching action is timed and driven by a control unit. In order to avoid current and voltage stress over individual components, the switching arrangements are driven in a synchronous manner. Therefore, a single control unit is often sufficient for controlling all solid state switches of the modulating input switches.

According to one embodiment, the output stage is provided with a single rectifying arrangement of switches in common for all power transformers. The switches may be diodes or three terminal solid state switches driven in a synchronous manner so as to render the switches conducting, when current flows in one direction, and non-conducting, when current flows in the opposite direction, whereby the solid state switches effectively act as diodes.

In one embodiment of the invention, all modulating input stages are connected in parallel to the common input terminals, and the arrangement of switches in each of the modulating input stages is a full-bridge boost arrangement of switches.

In another embodiment according to the invention, all modulating input stages are connected in parallel to the common input terminals, and the arrangement of switches of the modulating input stages is a push-pull boost arrangement of switches.

In yet another embodiment according to the invention, all modulating input stages are connected in parallel to the common input terminals, and the arrangement of switches of the modulating input stages is a two-inductor boost arrangement of switches.

In a further development of the above mentioned embodiments, the single arrangement of switches in the output stage is provided by diodes in a rectifying full-bridge arrange-

ment. Other configurations of the rectifying output stage, such as split secondary rectifier or voltage doubler rectifier configurations, may be conceived.

In one advantageous embodiment according to the invention, the input side converter stages are connected in parallel to a common pair of terminals. This embodiment is particularly advantageous, when the DC-power from one high current (low-voltage) source, such as a fuel cell arrangement, is to be converted in order to drive a load requiring voltages exceeding the voltage provided by the source. Alternatively, one high power load requiring a large current may be supplied from a low current (high voltage) source through a converter according to this embodiment of the invention.

In a further embodiment according to the invention, each of the input side converter stages comprises at least one energy storage inductor connected in series with the first winding of said input side converter stage. By arranging an energy storage inductor in each converter stage, it is achieved that each energy storage inductor only handles a fraction of the current. This is particularly advantageous for high power applications, where e.g. heat dissipation in a single energy storage inductor otherwise might limit scaling of the converter to the required specification.

Further, according to the invention, at least two energy storage inductors, each being arranged in a different input side converter stage, are at least pair-wise magnetically coupled via a common magnetic core so as to equalise their inductance. In practice, the magnetic coupling is typically provided by winding the at least two energy storage inductors onto a common magnetic core. Consequently, the at least two energy storage inductors may be perceived as a single energy storage inductor having at least two windings on a common core.

Advantageously, the inductor windings are wound together to form interleaved coils on the same magnetic piece. The magnetic coupling ensures a substantially identical inductance for the coupled inductors and that the currents are balanced between the two coupled stages. The current distribution can effectively be controlled by the power transformers. The well-balanced current distribution between the coupled stages thus achieved minimises the loss, since the difference in currents otherwise would have to be dissipated in a protection circuit on the input side in order to fulfil the condition of current limitation to the smallest of the first winding currents as imposed by the direct serial coupling of the second windings. Furthermore, current and voltage stresses in

the converter stage components, such as the solid state switches in the switching arrangements are minimised, thus allowing for a more optimised and consequently more cost efficient dimensioning of the components.

In a further embodiment according to the invention, the at least one energy storage inductor is provided as a common energy storage inductor for the power transformers. This embodiment eliminates artefacts in the current distribution between input side converter stages due to differences between different energy storage inductors, as all input side converter stages are supplied from the common energy storage inductor.

In a further aspect of the invention, the converter comprises at least one current balancing transformer on the input side. The current balancing transformer comprises at least one primary winding provided in a primary branch in series with the arrangement of switches of a first converter stage on the input side, and at least one secondary winding provided in a secondary branch in series with the arrangement of switches of a further input side converter stage. The primary windings and the secondary windings are arranged with opposite polarity to magnetically couple the primary branch and the secondary branch so as to induce opposite currents in the coupled branches, thereby pair-wise balancing the current distribution between the coupled branches at a predetermined current balancing ratio.

The at least one current balancing transformer provides a coupling between at least two input side converter stages, whereby energy can be transferred between the at least two converter stages in order to balance the current in the corresponding first windings. The current balancing transformer does not have to handle the full power provided to the respective converter stages, but only balance the deviations from the pre-determined balancing ratio and, consequently, the current balancing transformer is in practice dimensioned to the expected spread of deviations from the nominal current flowing in each of the input side converter stages. The balancing ratio is essentially determined by the transformer ratio, which is adapted to the ratio between the number of power transformers to be supplied through the primary branch to the number of power transformers to be supplied through the secondary branch. Typically, the primary branch and the secondary branch will be adapted to distribute current equally to an identical number of power transformers and the current balancing ratio is chosen to be 1:1.

In a further development of the above mentioned embodiment, a converter comprises an even number N=2n of the power transformers, where n is an integer number greater than one, and a cascading arrangement of a number M=(2n-1) of the current balancing transformers arranged to successively balance the current through the first windings of the N power transformers in cascading pairs of coupled branches, wherein each of the current balancing transformers provides a current balancing ratio of 1:1.

This tree-like arrangement of current balancing transformers is mostly applicable for input side converter stages operated in parallel and being supplied via a common pair of terminals from the same source. In particular, a number of 2^k power transformers is well suited for such an arrangement, where k is the number of times the branches are divided before the power transformer stage.

In a first step of the cascade, a first branch connected to one terminal on the input side is bifurcated into a first primary branch and a first secondary branch. The first primary branch is coupled to the first secondary branch via a first current balancing transformer in order to provide for an equal distribution of currents between the primary and secondary branch. In each further step of the cascade, each of the first primary and secondary branches of that step are bifurcated into primary and secondary branches of the next step until the number of branches equals the number of input side converter stages each comprising one power transformer. The branches of the final step of the cascade are then connected so as to supply one input side converter stage each. In each step of the cascade, primary and secondary branches are provided with a current balancing transformer having a balancing ratio of 1:1 in order to ensure an equal distribution of current into each of the branches, thereby ensuring an equal distribution of the current to all input side converter stages.

In another development of the above mentioned embodiment, the converter comprises an uneven number P=(2n+1) of the power transformers, where n is an integer number greater than or equal to one, and a cascading arrangement of a number Q=2n of the current balancing transformers arranged to successively balance the current through the first windings of the N power transformers in cascading pairs of coupled branches, wherein at least one of the current balancing transformers provides a current balancing ratio of 2:1. This arrangement of current balancing transformers ensures an even distribution of current over an uneven number (greater than one) of input side converter stages. This embodiment according to the invention is particularly relevant for convert-

ers where the number of power transformers to be supplied from one branch can not be expressed as a power of two, such as an uneven number of power transformers. For example, an equal distribution of current to three input side converter stages, each comprising one power transformer, can be achieved in a first step of the cascade by providing twice the current to the first primary branch than to the first secondary branch and subsequently only bifurcating the first primary branch into a further primary and a further secondary branch supplied at a current distribution ratio of 1:1. The current distribution ratio in the first step is balanced by a current distribution transformer with a current balancing ratio of 2:1, while the current distribution between the further primary branch and the further secondary branch is balanced by a current balancing transformer with a current distribution ratio of 1:1. The first secondary branch, the further primary branch and the further secondary branch are then connected to supply one input side converter stage each.

According to another aspect of the invention the converter is adapted for operation as a bidirectional converter, wherein all arrangements of switches are provided by switches in a full-bridge configuration. In order to operate the converter in both directions, the switches in the switching arrangements have to be controllable switches, i.e. three terminal devices. Control circuits have to be provided for both sides of the converter, said control circuits being adapted to drive the switches for input modulation when the corresponding converter stage is operated as input, and to drive the switches for rectification when the corresponding converter stage is operated as output.

In a practical implementation of the converter circuit according to the invention, the parallel stages of the first circuit may be connected through a clamping and protection circuit. Furthermore, a low-pass filter is provided, in practice often as a capacitor connected across the input terminals and/or output terminals, in order to remove transients and ripples from the dc-current to be provided at the respective terminals. For the sake of clarity, such clamping, protection and filtering circuitries are not described in detail.

The invention is now explained by exemplifying embodiments with reference to the drawings. The drawings show in:

Fig. 1 a prior art isolated boost converter,

Fig. 2 an isolated boost converter with two parallel input stages, each comprising an energy storage inductor,

Fig. 3 an isolated boost converter with two parallel input stages and magnetically coupled energy storage inductors,

Fig. 4 an isolated boost converter with two parallel input stages, one common energy storage inductor and a current balancing transformer,

Fig. 5 an isolated boost converter with two parallel input stages, magnetically coupled energy storage inductors and a current balancing transformer,

Fig. 6 an isolated boost converter with four parallel input stages and a cascading arrangement of three current balancing transformers,

Fig. 7 an isolated boost converter with three parallel input stages and a cascading arrangement of two current balancing transformers,

Fig. 8 an isolated buck converter with two parallel output stages with current doubler rectifier arrangements, magnetically coupled energy storage inductors and current balancing transformers,

Fig. 9 an isolated bidirectional converter with two parallel first side converter stages, each comprising a current doubler rectifier arrangement, magnetically coupled energy storage inductors and current balancing transformers,

Fig. 10 an isolated boost converter with independent input side converter stages coupled through a current balancing transformer, and

Fig. 11 the isolated boost converter of Fig. 3 with a protection circuit.

Fig. 1 shows a prior art isolated boost converter with one input stage and one output stage coupled through a power transformer T1.

The input stage is provided with an energy storage inductor L, and a full-bridge arrangement of modulating switches S1, S2, S3, S4 controlling the current through a first winding T1a of the power transformer T1.

The output stage comprises a full-bridge rectifier arrangement of diodes D1, D2, D3, D4 for rectifying the current pulses received from the second winding T1b of the power transformer T1. Output power can be provided to a load (not shown) through a pair of output terminals B0, B1. The output current is controlled by modulating the pulse width of the current pulses through the first winding by controlling the switches S1, S2, S3, S4 accordingly by use of a control unit (not shown). When all switches S1, S2, S3, S4 are closed, the energy storage inductor L is charged while the first end and the second end of the first winding T1a are short circuited. The current in the first winding T1a is in first OFF-state. Opening the pair of switches S1, S4 simultaneously puts the current through the first winding T1a in a first ON-state for driving a first current pulse through the first winding T1a, thereby transferring energy from the boost inductor to the power transformer until the switches S1, S4 are closed again and the energy storage inductor L is recharged. Subsequently, the remaining pair of switches S2, S3 is activated and a second current pulse running opposite to the first is generated. The activation scheme of the switches S1, S2, S3, S4 is intended to be operated to always provide a current path for discharge of the energy storage inductor in order to avoid an excessive build-up of harmful voltage stress across any of the switches S1, S2, S3, S4. Commonly, a protection circuit (snubber, not shown here) is provided in order to absorb excessive currents/voltages.

Furthermore, a capacitor C is connected across the output terminals B0, B1 in order to remove ripple and transients from the output power. The function of the capacitor C is the same throughout all embodiments, and therefore the description of the capacitor C is omitted in the following.

Fig. 2 shows a first embodiment of a dc-dc converter according to the invention. The isolated boost converter shown in Fig. 2 has on a input side 1 two input side converter stages 3, 4 connected in parallel and coupled through two power transformers T1, T2 to a output side converter stage 5 on a output side 2.

The input side 1 converter stages 3, 4 are configured as input stages, wherein each converter stage comprises an energy storage inductor L1, L2, and a full-bridge ar-

rangement of modulating switches {S1, S2, S3, S4}, {S5, S6, S7, S8} controlling the current through the first windings T1a, T2a of the power transformers T1, T2.

The output side 2 converter stage 5 comprises a single full-bridge rectifier arrangement of diodes {D1, D2, D3, D4} for rectifying the current pulses received from the second windings T1b, T2b of the two power transformers T1, T2. The second windings T1b and T2b are directly connected in series, the outermost ends being connected to the rectifier {D1, D2, D3, D4}.

In operation, high current is provided to the input side through terminals A0, A1. The current is split at a node N1 according to the impedances of the input side converter stages, and fed to the first windings T1a, T2a as modulated by the arrangements of switches {S1, S2, S3, S4}, {S5, S6, S7, S8}, respectively. The generated current pulses are transferred to the second windings T1b, T2b. Because of the direct serial connection of the second windings T1b, T2b, the therein induced current is limited to the smallest of the currents transferred in parallel from the first windings T1a, T2a. The excess current that can not be transferred from the input side 1 to the output side 2 is typically absorbed by a protection circuit (snubber) P on the input side. The absorbed energy may either be dissipated in, or in some cases recovered for a later transfer from the protection circuit P. The current pulses induced in the series of second windings T1b, T2b are rectified in a common rectifier unit formed by a single arrangement of switches, here shown as a full-bridge arrangement of diodes {D1, D2, D3, D4}. The rectified output may be passed through a low-pass filter C and via output terminals B0, B1 provided to a load.

Fig. 3 shows a modified version of the isolated boost converter shown in Fig. 2, which is modified by providing a coupling between the two parallel input stages 3, 4 in order to equalise the current distribution to said input stages 3, 4. The coupling is provided by magnetically coupling the energy storage inductor L1-1 provided in a first input stage 3 and the energy storage inductor L1-2 provided in a second input stage 4, for example by winding the two inductors onto a common magnetic core. The magnetic coupling ensures that the coupled energy storage inductors assume essentially the same inductance, and current balancing between the two inductors is controlled during the energy transfer state, i.e. the ON-state, by the serial connection of the second windings of the power transformers.

Fig. 4 shows a further embodiment of an isolated dc-dc converter according to the invention. The energy storage inductor is provided as a common inductor L that is placed before the bifurcation in node N1. This embodiment is particularly applicable where the size and/or power performance of the single energy storage inductor L are not limiting. The advantage of this embodiment is that no spread in the current distribution occurs. This spread typically arises due to differences in inductance between separate energy storage inductors L1, L2 placed within the input stages of for instance the embodiment shown in Fig. 2.

In the embodiment shown in Fig. 4, the two parallel input stages 3, 4 are coupled by a current balancing transformer X1. The current balancing transformer X1 comprises a primary winding X1-1 arranged in a primary branch 6 in the first input stage 3, and a secondary winding X1-2 in a secondary branch 7 in the second input stage 4.

If the currents in the two input stages 3, 4 differ from each other, the transformer X1 balances the currents in the two input stages by "pulling" a voltage from one of the input stages to the other input stage. The current balancing transformer X1 does only have to handle the smaller voltages required to balance the currents rather than having to handle the full power in each input stage 3, 4. This has a considerable practical advantage, because the current balancing transformer X1 only requires a fraction of the power rating as compared to the full power converted.

Fig. 5 shows a combination of the embodiments of an isolated boost converter shown in Figs. 3 and 4. Each of the input stages 3, 4 is provided with an energy storage inductor L1-1, L1-2. The energy storage inductors L1-1, L1-2 are magnetically coupled in order to equalise their inductance. In addition, a current balancing transformer X1 is provided to couple the two input stages 3, 4 so as to compensate for differences in the currents flowing in the two input stages 3, 4. An embodiment where the energy storage inductors L1-1, L1-2 are not magnetically coupled is also anticipated by the invention.

Fig. 6 shows an isolated boost converter comprising four power transformers T1, T2, T3, and T4 respectively, connected to one of four parallel input stages on the input side 1, and to a rectifying output stage Re on the output side 2.

Each of the four input stages comprises an energy storage inductor L1-1, L1-2, L1-3, L1-4, and a full-bridge arrangement of modulating switches for controlling the current

through the first winding of the corresponding power transformer T1, T2, T3, T4. In the configuration shown, all four energy storage inductors L1-1, L1-2, L1-3, L1-4 are magnetically coupled so as to equalise their inductance.

Current is supplied to the input side 1 through a cascading arrangement of bifurcating nodes N3, N2, N1 splitting the input current provided through terminal A1 so as to provide equal current input to all four input stages. At each bifurcation N3, N2, N1, the current distribution is balanced by a current balancing transformer X3, X2, X1, each comprising a primary winding X3-1, X2-1, X1-1, and a secondary winding X3-2, X2-2, X1-2.

In order to achieve an equal current distribution, the impedances of all four input stages are designed to be essentially the same, and the current balancing ratio as given by the transformer ratio is 1:1 for all three current balancing transformers X3, X2, X1.

Embodiments where the energy storage inductors L1-1, L1-2, L1-3, L1-4 are not magnetically coupled are also anticipated by the invention.

Fig. 7 shows another embodiment of a dc-dc boost converter according to the invention. The embodiment shown in Fig. 7 comprises three power transformers T1, T2, T3 supplied from the input side 1 through a cascading arrangement of bifurcating nodes N4, N1 with current balancing transformers X4, X1, each comprising a primary winding X4-1, X1-1, and a secondary winding X4-2, X1-2. Node N1 provides current to two nominally identical input stages. Therefore, the current balancing transformer X1 balances the currents at a balancing ratio of 1:1. Node N4, however, provides current to three input stages, viz. two input stages being supplied through the primary winding X4-1, and one input stage being supplied through the secondary winding X4-2 of the current balancing transformer X4. Therefore, the current balancing ratio of the current balancing transformer X4 is 1:2, so as to provide twice as much current through the primary winding X4-1 as through the secondary winding X4-2. X4-2 therefore comprises twice as many windings as X4-1. Embodiments where the energy storage inductors L1-1, L1-2, L1-3 are not magnetically coupled are also anticipated by the invention.

Fig. 8 shows an alternative embodiment of a dc-dc converter utilising a current balancing transformer. The embodiment shown in Fig. 8 is an isolated buck-type converter comprising two power transformers T1, T2, where the output side 2 is operated as input stage, and the input side 1 comprises two parallel rectifying output stages.

On the input side, a single full-bridge-arrangement of switches {S9, S10, S11, S12} controls the current through all second windings T1b, T2b coupled in series with each other.

On the output side, each of the first windings T1a, T2a feeds a current-doubler rectifying circuit. Depending on the direction of the current in the first windings T1a, T2a the output is provided in parallel through energy storage inductors L1-1 and L1-2 connected to the input side of the first windings T1a, T2a, or through energy storage inductors L2-1, L2-2 connected to the output side of the first windings T1a, T2a.

Corresponding branches of the parallel output stages are coupled in order to ensure an equal distribution of currents between the output stages. The corresponding branches are those branches that are connected to simultaneously provide current to the output terminal A1 through node N5. That is, branch 8 and branch 10 correspond to each other, and branch 9 and branch 11 correspond to each other. The coupling is achieved by magnetic coupling of the energy storage inductors L1-1, L1-2 and L2-1, L2-2 in the corresponding branches of the parallel output stages and/or by means of current balancing transformers X5, X6 for balancing current between the primary winding X5-1 in the primary branch 8 and the secondary winding X5-2 in the secondary branch 10, and accordingly between branch 9 and branch 11 by balancing current between the primary winding X6-1 and the secondary winding X6-2 of the current balancing transformer X6, respectively.

When S9 and S12 are conducting, the current through the second windings T1b, T2b are in a first ON-state, and diodes D6 and D8 are OFF. Thus, energy storage inductors L1-1 and L1-2 are charged, while energy storage inductors L2-1 and L2-2 are discharged. When S10 and S11 are conducting, the current through the second windings T1b, T2b are in a second ON-state, and diodes D5 and D7 are OFF. Thus, energy storage inductors L2-1 and L2-2 are charged, while energy storage inductors L1-1 and L1-2 are discharged.

Embodiments where the energy storage inductors L1-1, L1-2 and/or the energy inductors L1-3, L1-4 are not magnetically coupled are also anticipated by the invention.

Fig. 9 shows a further embodiment of a dc-dc converter according to the invention. The embodiment shown in Fig. 9 is an isolated bidirectional converter comprising two power transformers T1, T2. The switching arrangements of both sides are provided with controllable switches {S9…S12}, {S13, S14}, {S15, S16}, such as three-terminal solid-state switches. Thus, the converter can be operated in both directions. On the side chosen as the input, the switching arrangement(s) are driven to modulate the input current. On the opposite side (chosen as the output), the switching arrangement(s) are driven to rectify the current pulses received from the power transformers T1, T2.

Embodiments where the energy storage inductors L1-1, L1-2 and/or the energy inductors L1-3, L1-4 are not magnetically coupled are also anticipated by the invention.

Fig. 10 shows an isolated boost-type converter according to the invention comprising two power transformers T1, T2. The input side 1 is operated as input, wherein the input side converter stages are operated independently. The two input stages on the input side are coupled to ensure an equal distribution of the current between the two input stages. In the embodiment shown in Fig. 10, the coupling is achieved via a current balancing transformer with a primary winding X7-1 arranged in one input stage and a secondary winding X7-2 in the other input stage. Alternatively or in addition thereto the energy storage inductors L1 and L2 may be coupled magnetically, e.g. by winding both inductors L1, L2 onto a common magnetic core so as to equalise their inductance.

Deviations from the nominal current distribution between the input side converter stages or a failure in the controlling unit driving the switches of a switching arrangement can lead to undesired stress on the components and consequently lead to a failure of those components. In order to avoid such stresses, the input circuit is typically equipped with a protection circuit P. Many implementations of protection circuits are possible. Some protection circuits absorb and dissipate excess energy. Other protection circuits may provide for an at least partial recovery of the absorbed energy. Fig. 11 shows an example for a dissipative protection circuit P in the isolated boost converter of Fig. 3. The protective circuit P may receive excess current from the first input stage 3 through a node N6 and a diode D9, and from the second input stage 4 through a node N7 and a diode D10. The excess energy is absorbed by a large capacitor Cp and eventually dissipated through a resistor Rp.

The invention has been described with reference to a preferred embodiment. However, the scope of the invention is not limited to the illustrated embodiment, and alterations and modifications can be carried out without deviating from said scope of the invention.

List of reference numerals

1	input side
2	output side
3, 4	input side converter stages
5	output side converter stage
6, 8, 9	primary branch
7, 10, 11	secondary branch
A0, A1, A2, A3	input side terminal
B0, B1	output side terminal
C	capacitor
D1, D2, … , D10	diode
L, L1, L2	energy storage inductor
L1-1, L1-2, L1-3, L1-4	magnetically coupled energy storage inductor
L2-1, L2-2	magnetically coupled energy storage inductor
N1, N2, … , N7	node
Re	rectifier unit
S1, S2, … , S16	switch
T1, T2, T3, T4	power transformer
T1a, T2a	first winding
T1b, T2b	second winding
X1, X2, … , X7	current balancing transformer

transformer	primary winding	secondary winding
X1	X1-1	X1-2
X2	X2-1	X2-2
X3	X3-1	X3-2
X4	X4-1	X4-2
X5	X5-1	X5-2
X6	X6-1	X6-2
X7	X7-1	X7-2

Claims

1. A pulse width modulated switch mode DC-DC boost converter comprising at least one first electronic circuit on an input side (1) and a second electronic circuit on an output side (2), the input side (1) and the output side (2) being coupled via at least two power transformers (T1, T2), each power transformer (T1, T2) comprising a first winding (T1a, T2a) arranged in an input side converter stage (3, 4) on the input side (1) and a second winding (T1b, T2b) arranged in an output side converter stage (5) on the output side (2), each of the windings (T1a, T1b, T2a, T2b) having a first end and a second end, wherein

the first electronic circuit comprising:

- terminals (A0, A1) for connecting a source or a load,

- at least one energy storage inductor (L) coupled in series with at least one of the first windings (T1a, T2a) of the power transformers (T1, T2),

- for each power transformer (T1, T2), an arrangement of switches being adapted to switch the current through the first winding (T1a, T2a) between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state, and wherein

- the at least one energy storage inductor (L) is arranged so as to be charged, when all switches of the switching arrangements are conducting,

and

the second electronic circuit comprising:

- terminals (B0, B1) for connecting a load or a source,

- a single arrangement of switches being adapted to switch the current through the second windings (T1b, T2b) of the power transformers (T1, T2) between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state,

and a second OFF-state, and/or being adapted to provide rectified current to the terminals (B0, B1), and wherein

the second windings (T1b, T2b) of the power transformers (T1, T2) are connected in series and coupled via the single arrangement of switches of the second circuit to the terminals (B0, B1) of the output side.

2. Converter according to claim 1, wherein the pulse width modulated switch mode DC-DC boost converter is controlled via the arrangement of switches on the input side (1).

3. Converter according to claim 1 or 2, wherein the at least one energy storage inductor (L) is coupled to or is part of a current-balancing electrical circuit.

4. Converter according to any of the preceding claims, wherein the arrangement of switches being adapted to switch the current through the first windings comprises two parallel coupled stages, each of the parallel coupled connections comprising a first switch serial connected to a second switch, and wherein the first end of the first winding is coupled to the serial connection of one of the two parallel coupled stages, and wherein the second end of the first winding is coupled to the serial connection of the other of the two parallel coupled stages.

5. Converter according to any of the preceding claims, wherein the input side converter stages (3, 4) are provided as modulating input stages and the output side converter stage (5) is provided as a rectifying output stage.

6. Converter according to claim 5, wherein the modulating input stages (3, 4) are connected in parallel to the common input terminals (A0, A1) and wherein the arrangement of switches in each of the modulating input stages (3, 4) is a full-bridge arrangement of switches, alternative a push-pull boost arrangement of switches, or alternative a two-inductor boost arrangement of switches.

7. Converter according to any of the preceding claims, wherein the input side converter stages (3, 4) are connected in parallel to a common pair of terminals (A0, A1).

8. Converter according to any of the preceding claims, wherein each of the input side converter stages (3, 4) comprises at least one energy storage inductor (L1, L2) connected in series with the first winding (T1a, T2a) of said input side converter stage (3, 4).

9. Converter according to claim 8, wherein at least two energy storage inductors (L1-1, L1-2), each being arranged in a different input side converter stage (3, 4), are at least pair-wise magnetically coupled via a common magnetic core.

10. Converter according to any of claims 1-7, wherein the at least one energy storage inductor L is provided as a common energy storage inductor for the power transformers (T1, T2).

11. Converter according to any of the preceding claims, further comprising at least one current balancing transformer (X1) on the input side, said current balancing transformer (X1) comprising:

- at least one primary winding (X1-1) provided in a primary branch (6) in series with the arrangement of switches of a first converter stage (3) on the input side (1),

- at least one secondary winding (X1-2) provided in a secondary branch (7) in series with the arrangement of switches of a further input side converter stage (4),

wherein the primary windings (X1-1) and the secondary windings (X1-2) are arranged with opposite polarity to magnetically couple the primary branch (6) and the secondary branch (7) so as to induce opposite currents in the coupled branches (6, 7), thereby pair-wise balancing the current distribution between the coupled branches (6, 7) at a predetermined current balancing ratio.

12. Converter according to claim 11, wherein the converter comprises:

- an even number N=2n of the power transformers (T1, T2, …), where n is an integer number greater than one, and
- a cascading arrangement of a number M=(2n-1) of the current balancing transformers (X1, X2, …) arranged to successively balance the current through the first windings (T1a, T2a, …) of the N power transformers (T1, T2, …) in cascading pairs of

coupled branches, wherein each of the current balancing transformers (T1, T2, …) provides a current balancing ratio of 1:1.

13. Converter according to claim 11, wherein the converter comprises:

- an uneven number P=(2n+1) of the power transformers (T1, T2, …), where n is an integer number greater than or equal to one, and

- a cascading arrangement of a number Q=2n of the current balancing transformers (X1, X2, …) arranged to successively balance the current through the first windings (T1a, T2a, …) of the N power transformers (T1, T2, …) in cascading pairs of coupled branches, wherein at least one of the current balancing transformers provides a current balancing ratio of 2:1.

14. Converter according to any of the preceding claims, wherein the single arrangement of switches in the output stage (5) is provided by diodes in a rectifying full-bridge arrangement.

15. Converter according to any of claims 1-13, wherein the converter further is adapted for operation as a bidirectional converter.

16. Converter according to claim 15, wherein all arrangements of switches are provided by switches in a full-bridge configuration.

17. Converter according to any of the preceding claims, further comprising a capacitor (C) connecting the terminals (A0, A1) on the input side (1) and/or a capacitor (C) connecting the terminals (B0, B1) on the output side (2).

Switch mode pulse width modulated DC-DC Converter with Multiple Power Transformers.

Abstract

A switch mode pulse width modulated DC-DC power converter comprises at least one first electronic circuit on a input side (1) and a second electronic circuit on a output side (2). The input side (1) and the output side (2) are coupled via at least two power transformers (T1, T2). Each power transformer (T1, T2) comprises a first winding (T1a, T2a) arranged in a input side converter stage (3, 4) on the input side (1) and a second winding (T1b, T2b) arranged in a output side converter stage (5) on the output side (2), and each of the windings (T1a, T1b, T2a, T2b) has a first end and a second end. The first electronic circuit comprises terminals (A0, A1) for connecting a source or a load, at least one energy storage inductor (L) coupled in series with at least one of the first windings (T1a, T2a) of the power transformers (T1, T2), and for each power transformer (T1, T2), an arrangement of switches being adapted to switch the current through the first winding (T1a, T2a) between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state, and/or being adapted to provide rectified current to the terminals (A0, A1) wherein the at least one energy storage inductor (L) is arranged so as to be charged, when all switches of the switching arrangements are conducting, and the current through the at least one first winding coupled in series to the energy storage inductor is in an OFF-state. The second electronic circuit comprises terminals (B0, B1) for connecting a load or a source, a single arrangement of switches being adapted to switch the current through the second windings (T1b, T2b) of the power transformers (T1, T2) between a first ON-state, a first OFF-state, a second ON-state with a polarity opposite to the first ON-state, and a second OFF-state, and/or being adapted to provide rectified current to the terminals (B0, B1). The second windings (T1b, T2b) of the power transformers (T1, T2) are connected in series and coupled via the single arrangement of switches of the second circuit to the terminals (B0, B1) of the output side.

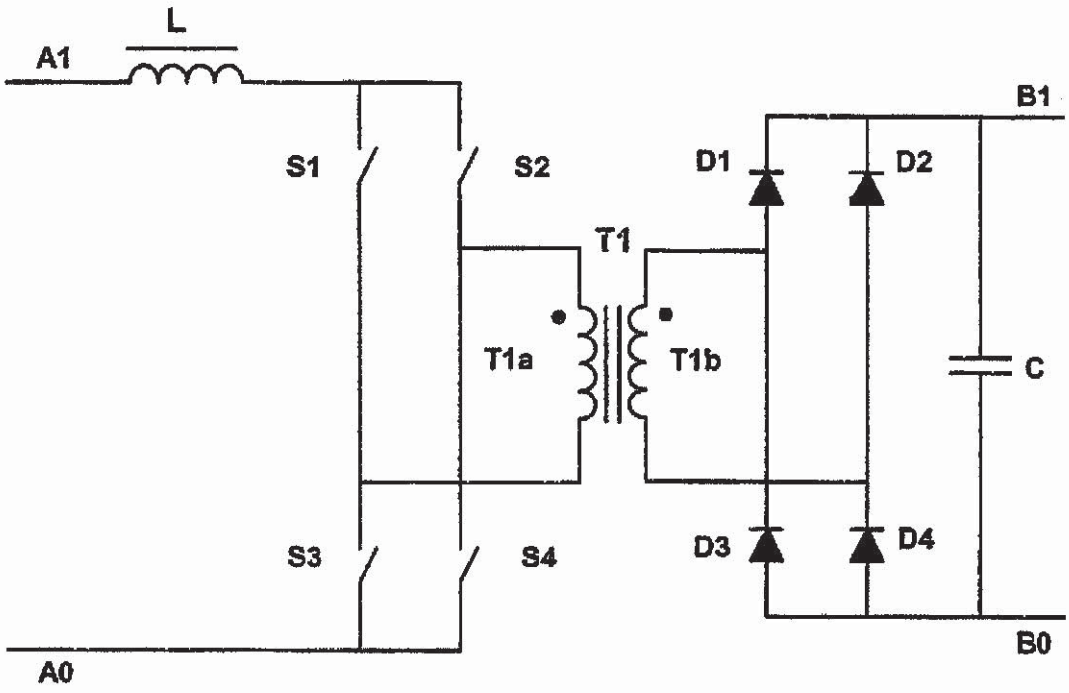
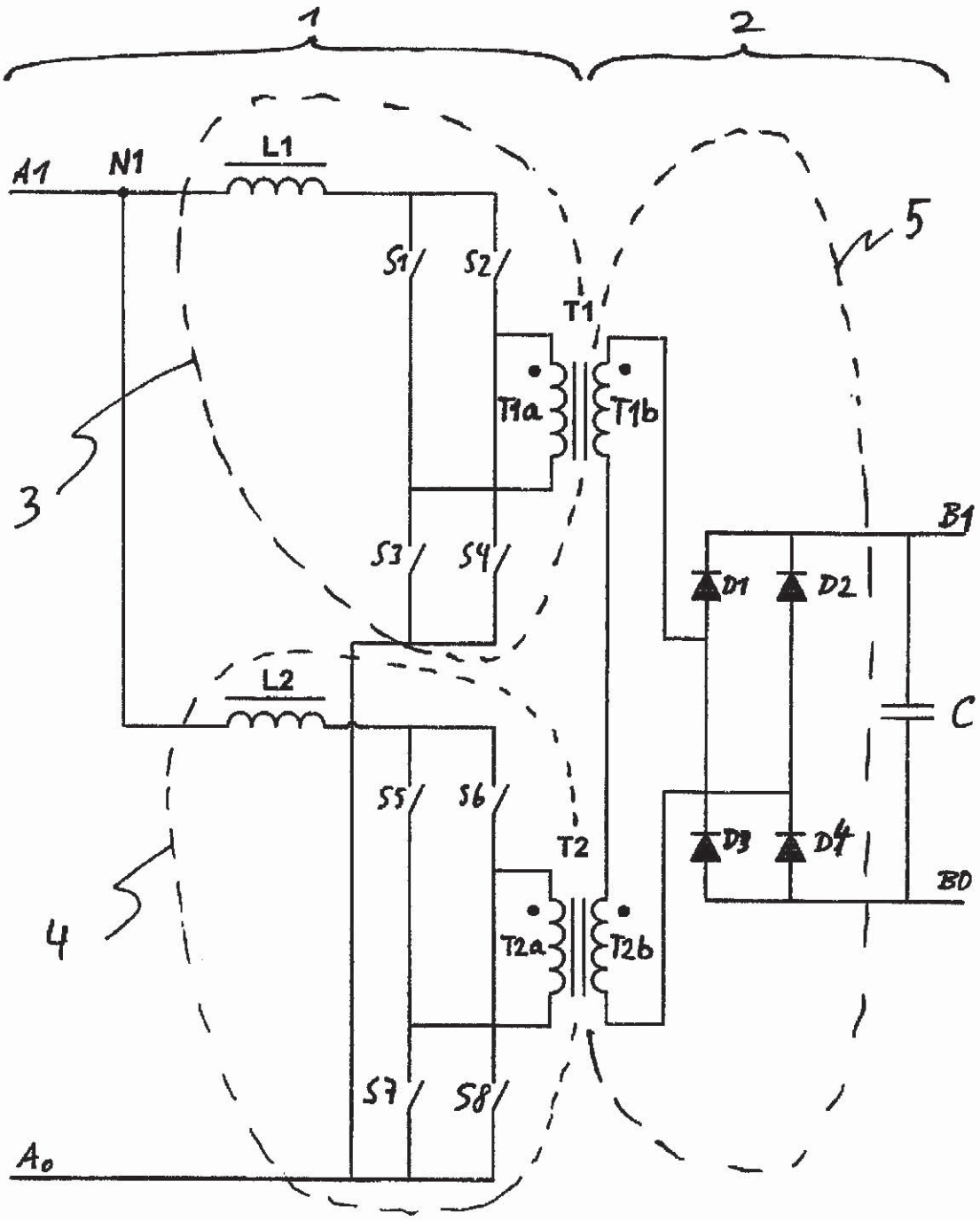


Fig. 1
(Prior Art)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S8
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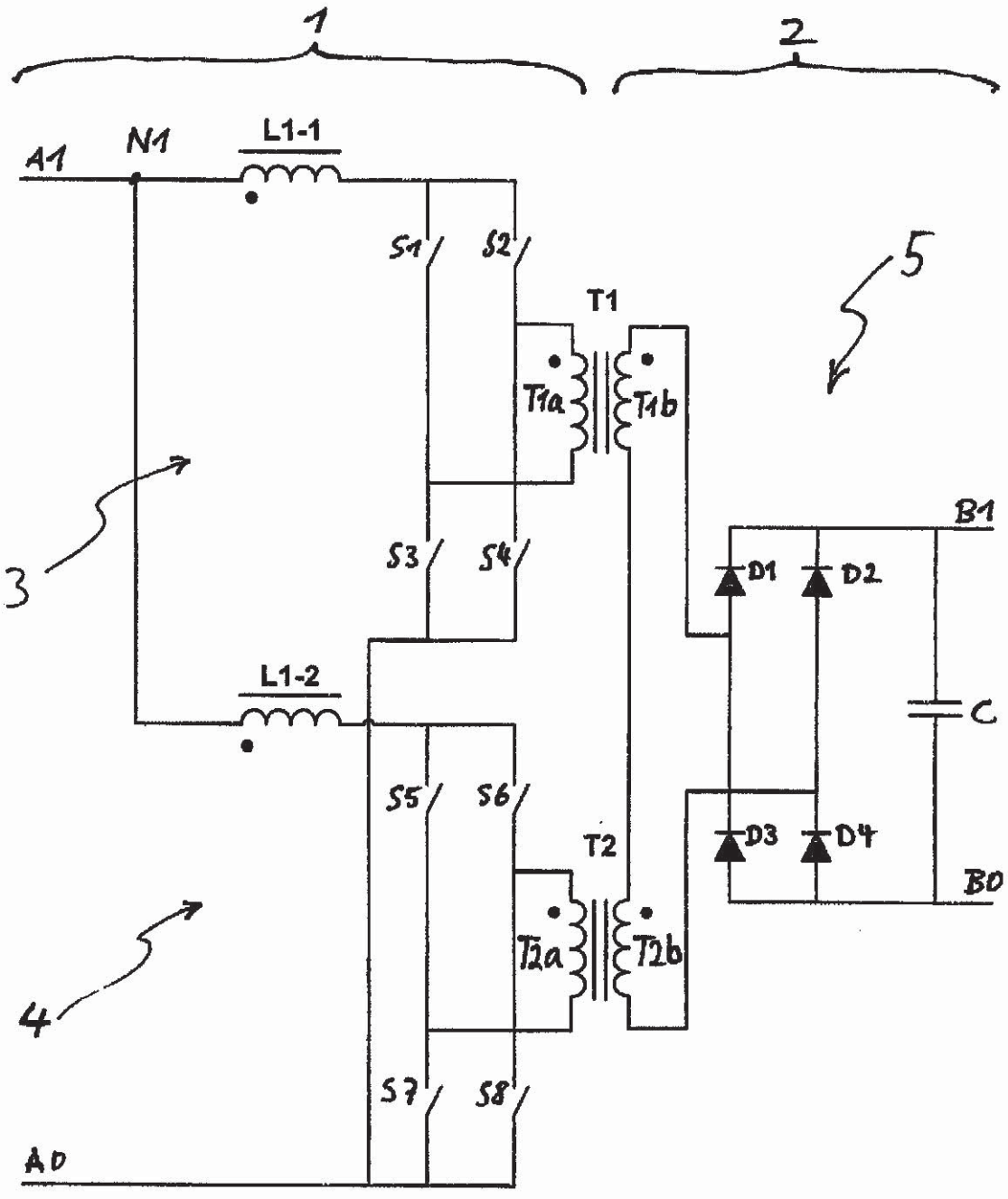
Fig. 2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D2
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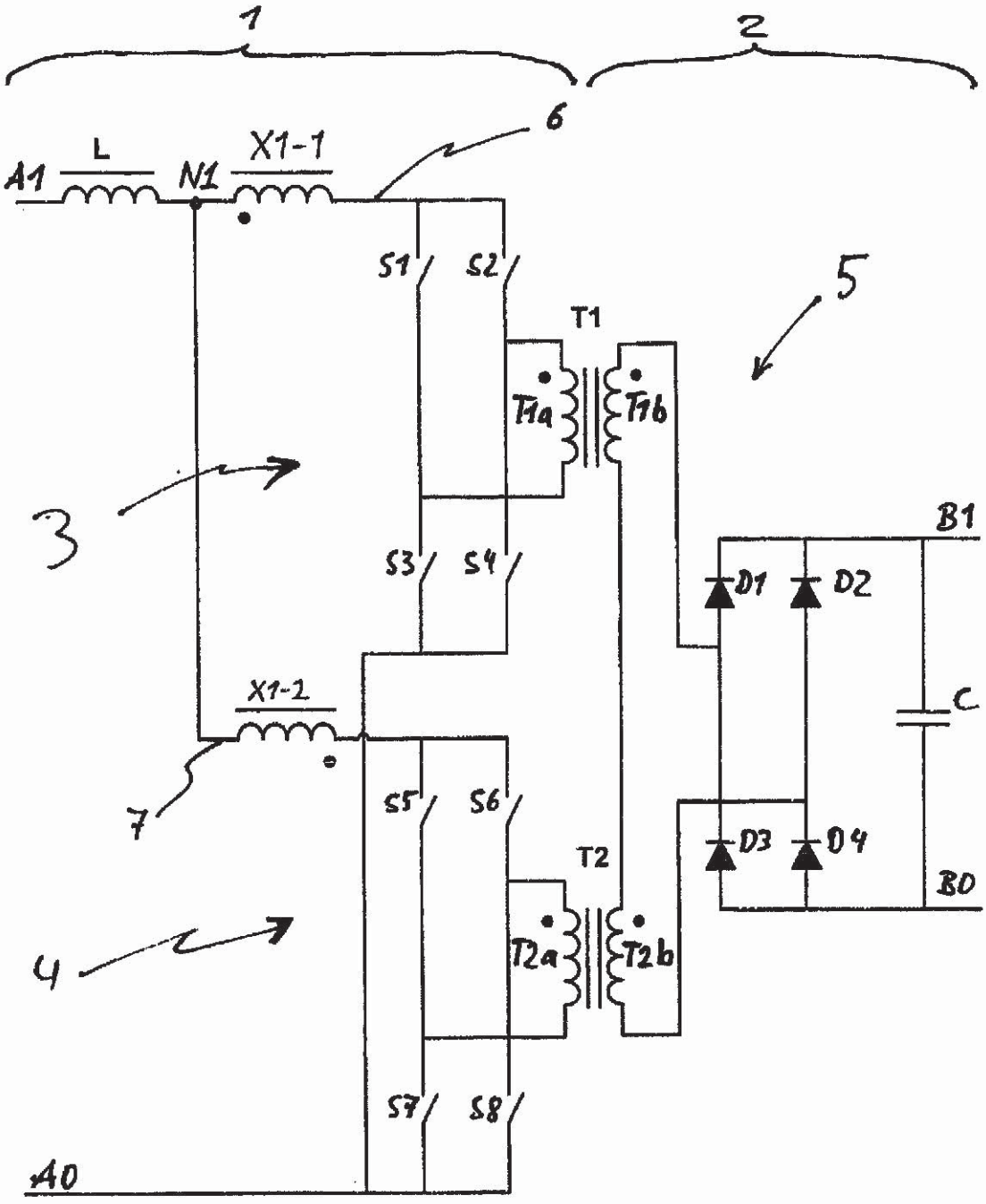
Fig. 3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D1
D2
X1-2
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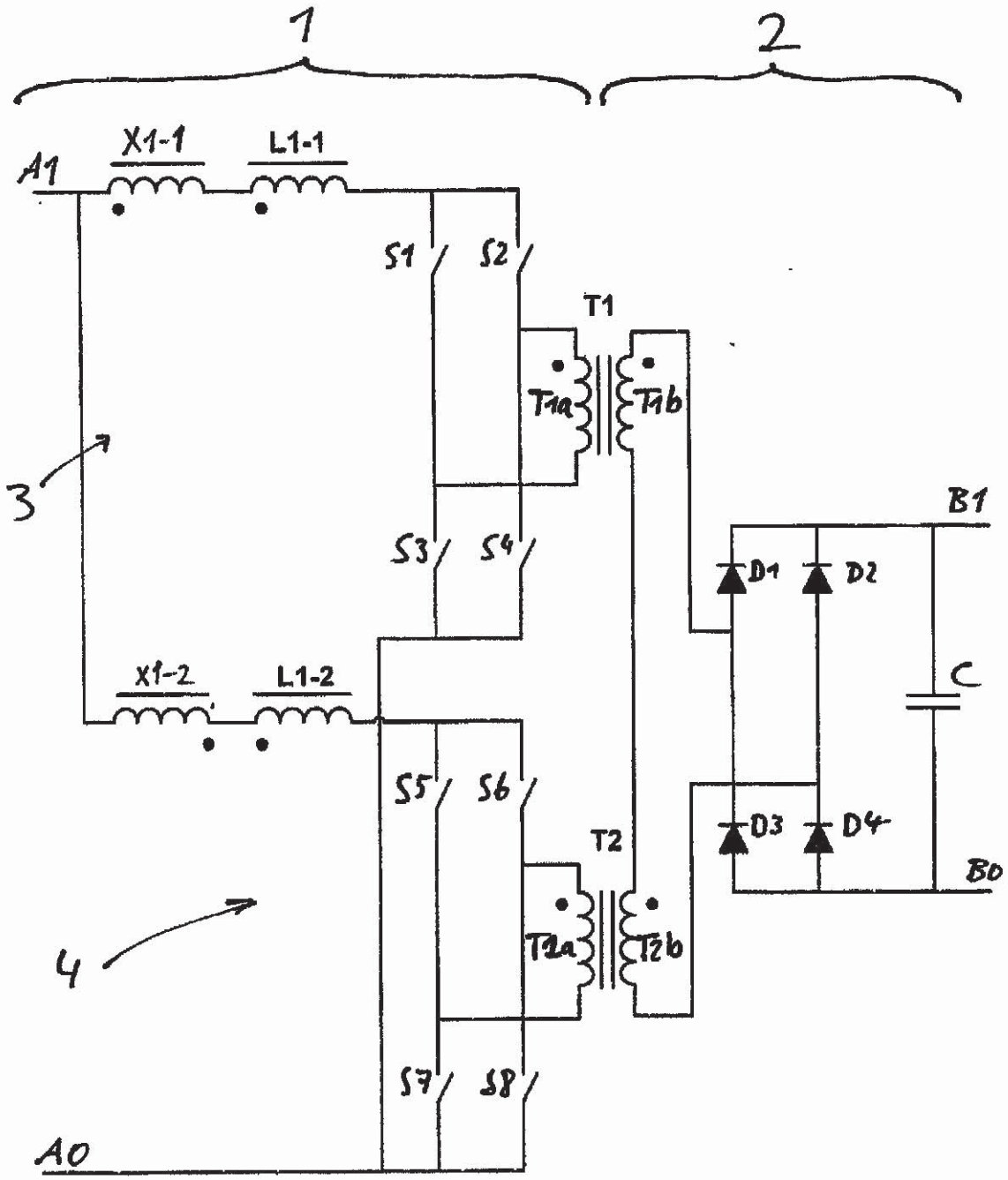
Fig. 4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S8
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Fig. 5

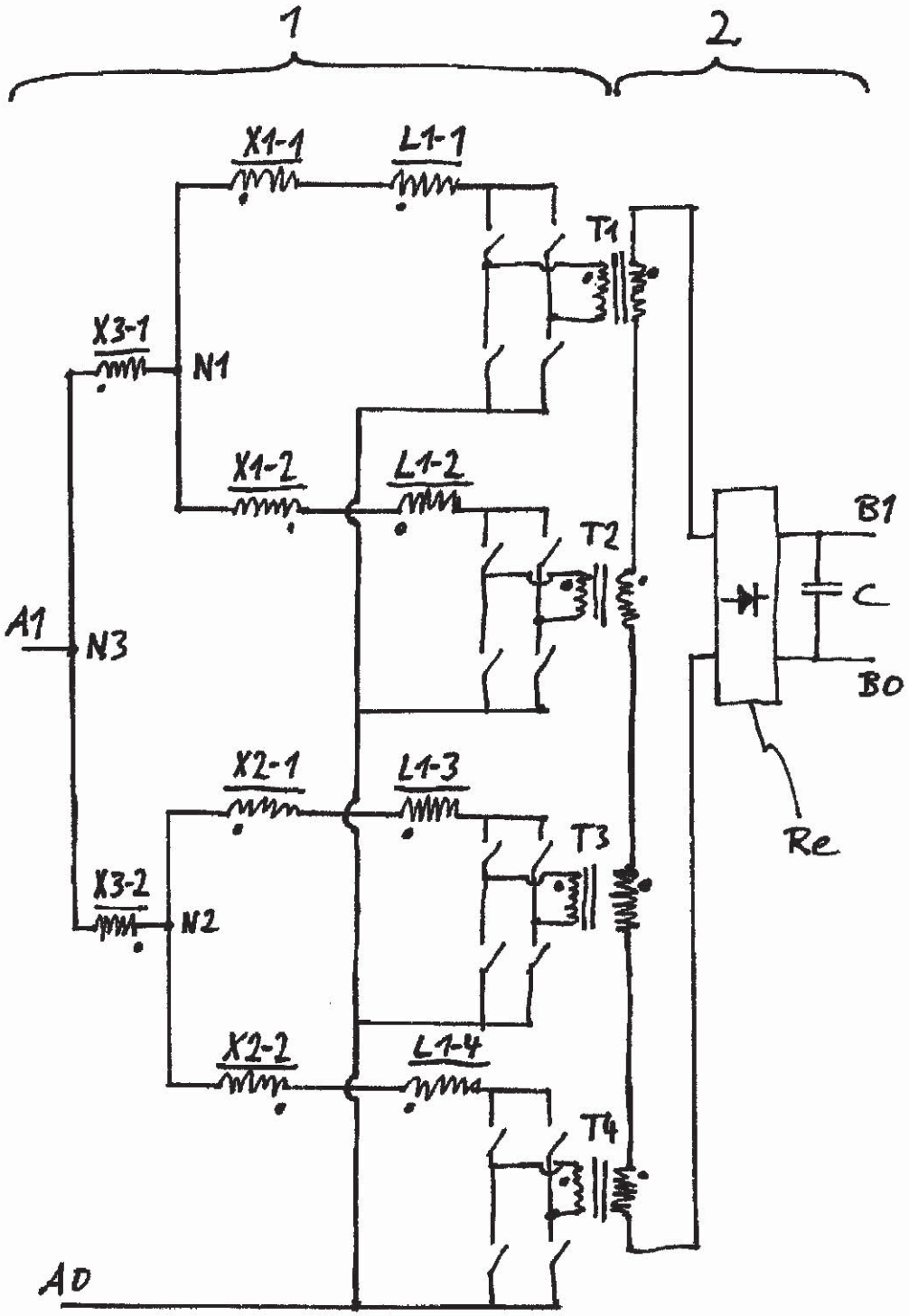
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Fig. 6

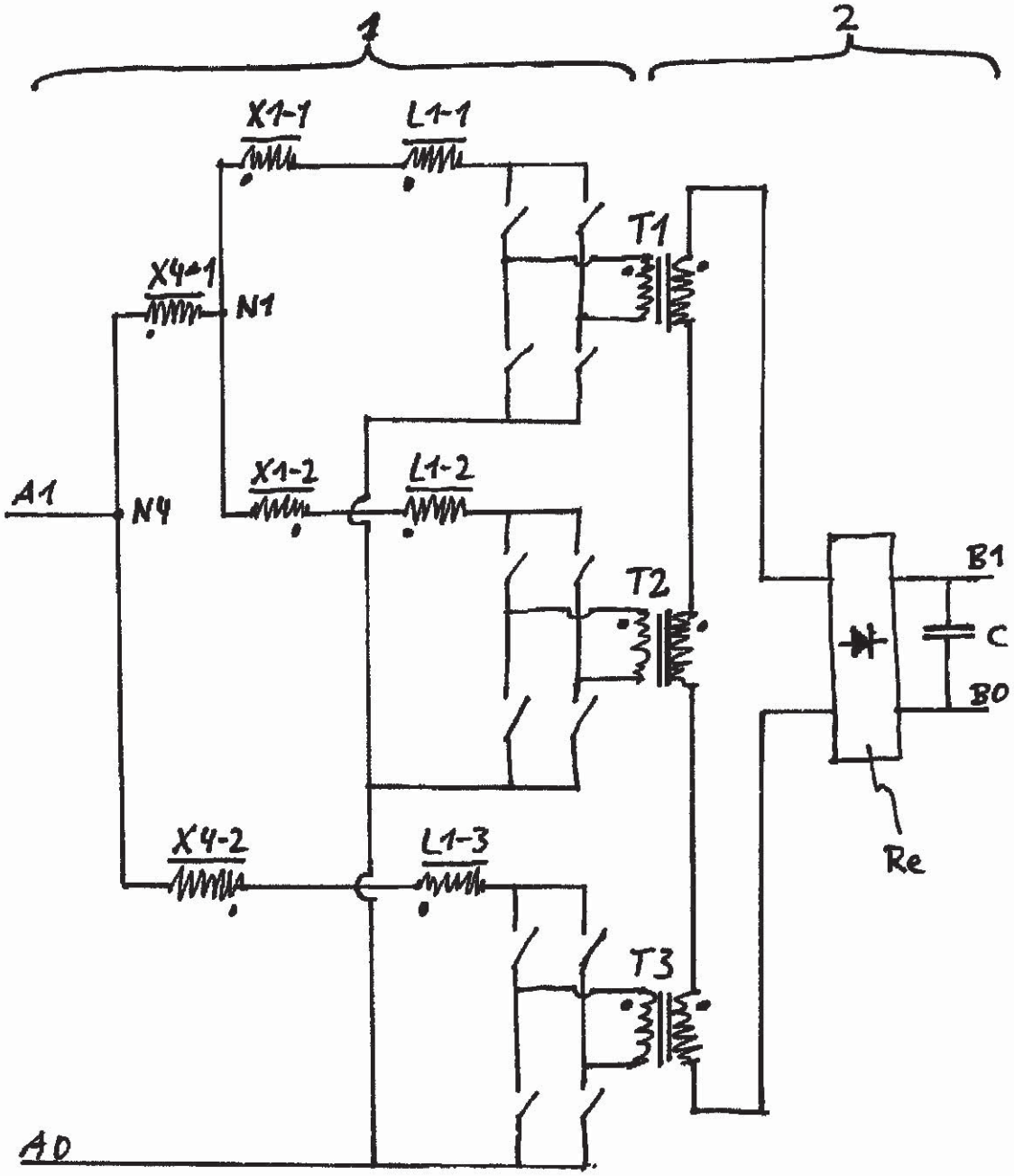
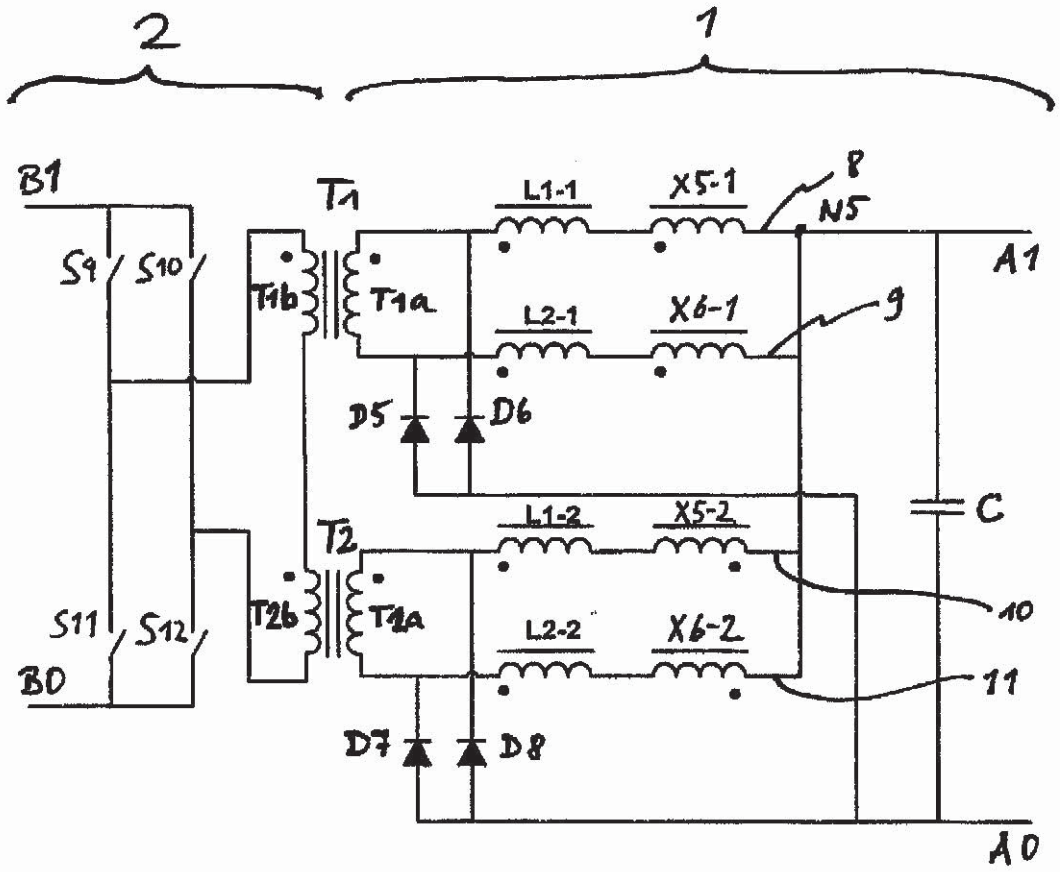


Fig. 7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X6-1
9
D5
D6
C
T2
L1-2
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S11
S12
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X6-2
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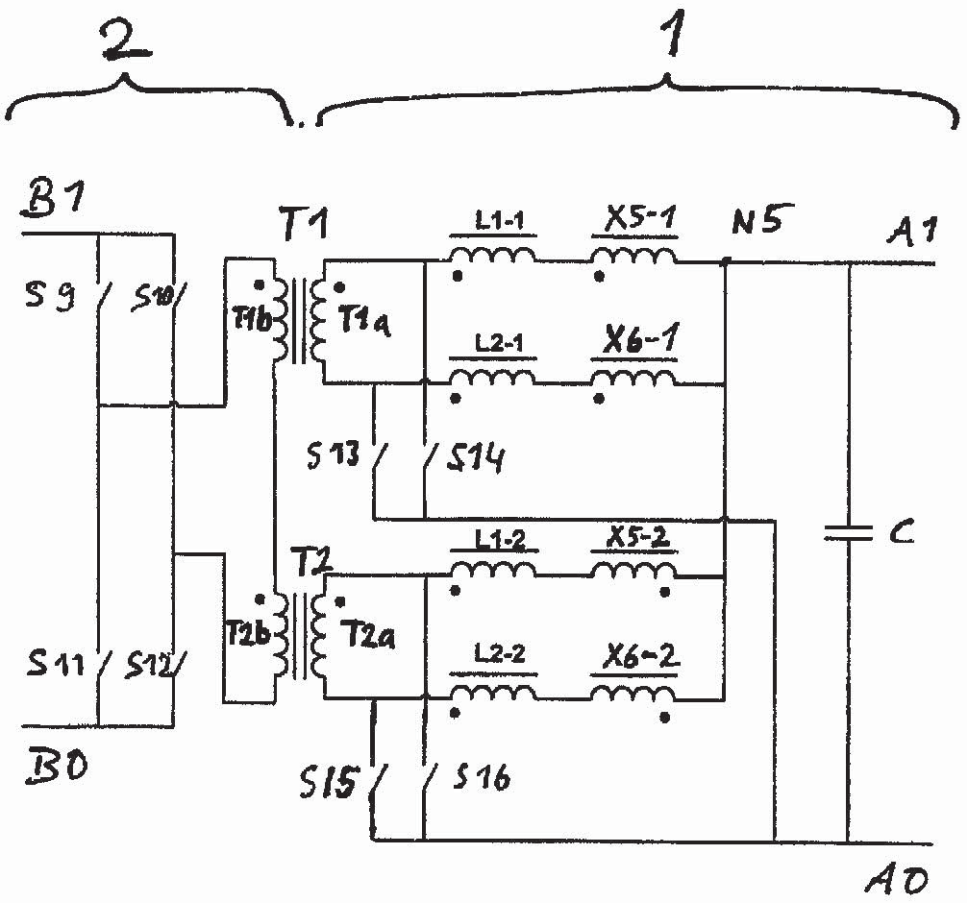
B0
D7
D8
A0

Fig. 8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T2
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S15
S16
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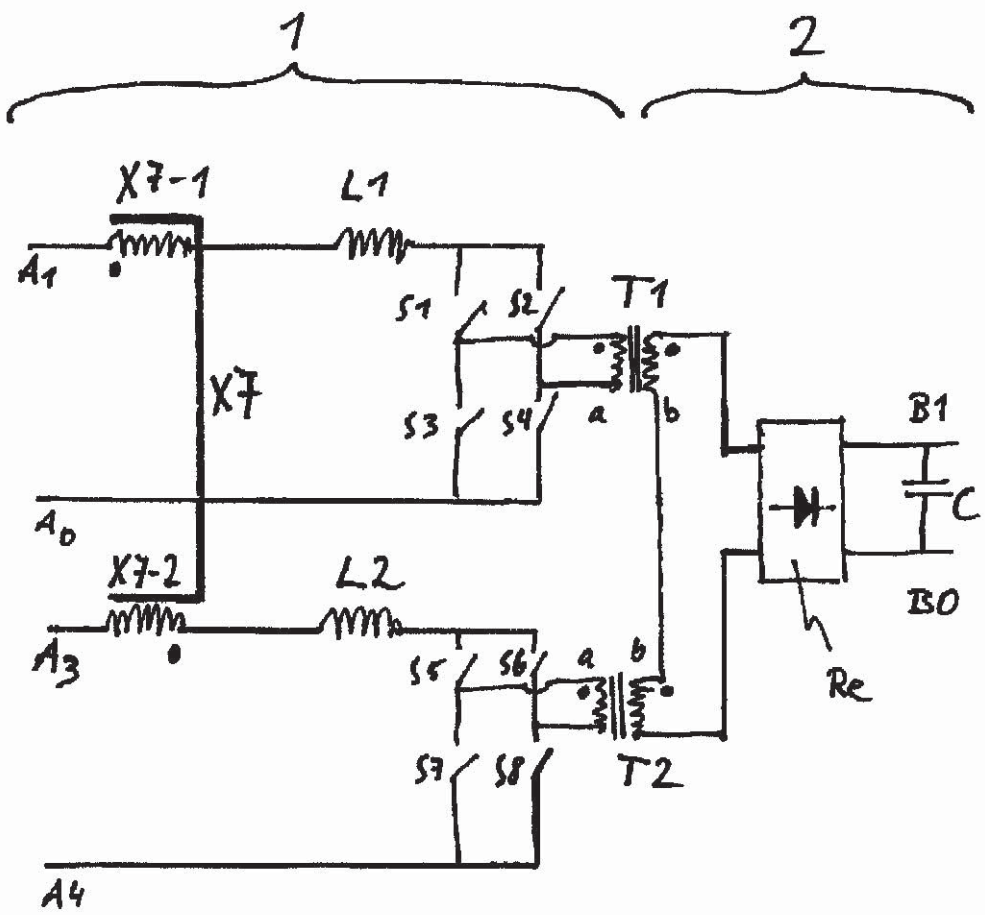
Fig. 9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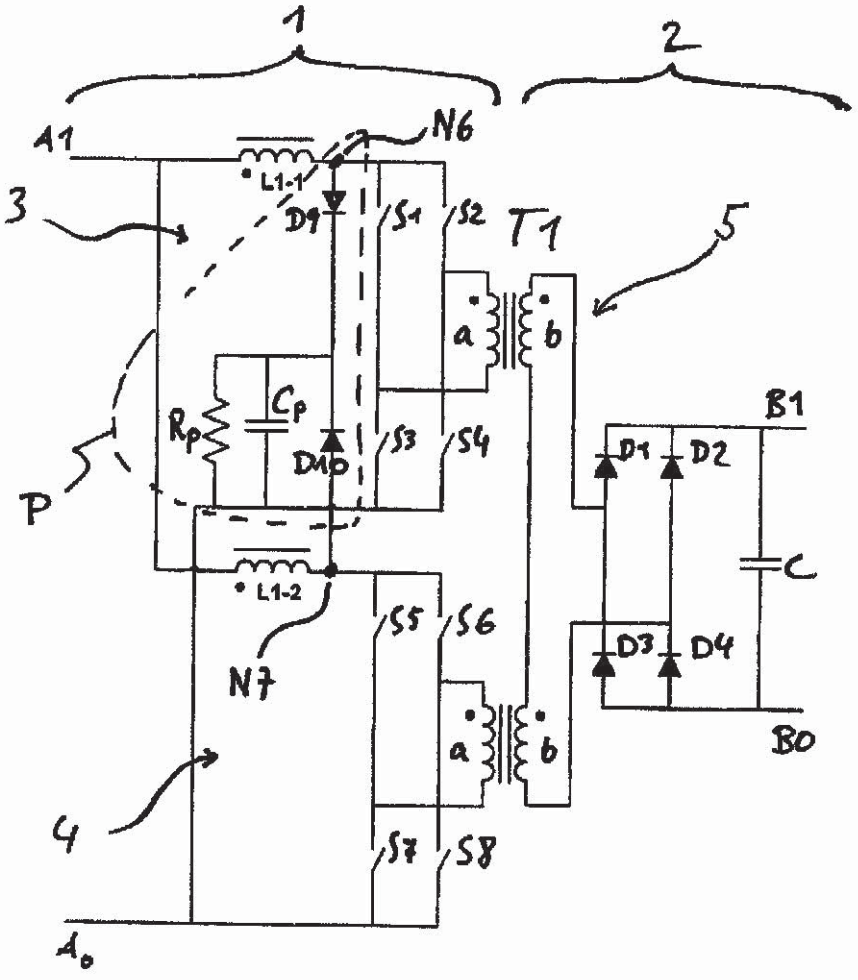
A4

Fig. 10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B1
D1
D2
P
C
L1-2
S5
S6
N7
D3
D4
a
b
B0
4
S7
S8
A0

Fig. 11

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