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Vidkjær, Jens

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Instabilities in RF-Power Amplifiers Caused by a Self-Oscillation in the Transistor Bias Network

JENS VIDKJAER, MEMBER, IEEE

Abstract—**This paper describes a self-oscillation in the bias network of an amplifier which is commonly used for the output stage in mobile transmitters. It is demonstrated how some often observed spurious oscillations may be related to the self-oscillation and a method for stabilizing the amplifier is derived and discussed.**

I. Introduction

SPURIOUS oscillations in RF-power amplifiers is a well-known experimental phenomena for which many origins have been suggested in literature [1], [2]. According to common practice and in agreement with Müller and Figel [2], the origins may be classified as follows.

1) Instabilities which can be explained by analogy with instability problems in linear circuits.

2) Parametric instabilities.

The classification of a particular oscillation is mainly based on observations where 1) oscillations of frequencies which are independent of the signal frequency may exist, and 2) subharmonics are generated.

This paper provides an alternative explanation of the observed instabilities based on a nonlinear self-oscillation in the bias network of a commonly recommended amplifier for mobile transmitters [3], [4]. It is known from nonlinear system theory [12] that the presence of self-oscillation in a circuit may result in both types of spurious oscillations described above, and this will be the basis for the following discussion.

Due to the strongly nonlinear operation of the transistor and the complexity of the RF-amplifier circuit the most realistic method for a detailed study is combined experimental and numerical investigation. The computational and modeling aspects of the amplifier will, however, not be considered here; they are thoroughly discussed in [8] and are the planned subject for a subsequent paper. It should only be mentioned that the following physical effects must be included in the transistor model in order to achieve satisfactory agreement between simulations and experiments:

1) transit time and gain modulation due to base widening [5]-[7];

2) high-field current saturation in the collector epitaxial region [6], [7];

3) avalanche and Zener breakdown in the emitter and collector junctions.

II. Spurious Oscillations

The amplifier which is the basis for most of the following discussion is shown in Fig. 1. The RF-power transistor is biased for class-C operation through the chokes L_b and L_c. R_b is a damping resistance. At the input side the matching network raises the rather low transistor RF-input impedance to the impedance level of the generator. The nominal load is transformed through the output matching network to the collector load which gives maximum output power at the given input drive level.

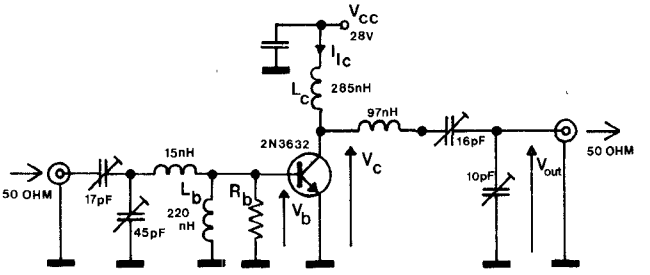

Fig. 1. 160-MHz power amplifier. Performance data: output power—13.8 W; gain—9 dB; and collector efficiency—73 percent.

TABLE I
Experimental Observations on the Amplifier of Fig. 1

Damping of Base Choke	Circuit Performance
$R_b = 1$ kΩ	Tuning impossible.
$R_b = 470$ Ω	Tuning possible. No spurious oscillations for output VSWR ≤ 1.3 or supply voltages down to 22 V. A very small reduction in input drive causes spurious oscillations.
$R_b = 47$ Ω	No spurious oscillations for output VSWR ≤ 7 and supply voltages down to 8 V. Spurious oscillations occur at drive power levels 9 dB below the nominal level.
$R_b = 26$ Ω	No spurious oscillations at any load, supply voltage, and drive power conditions.

The primary goals in the design of amplifiers of this type are obviously connected with the fulfillment of power, gain, and bandwidth specifications. For this purpose methods are well established [9], [10]. It is, however, a frequent experience that if the bias chokes and their damping are not properly chosen spurious oscillations may appear in an otherwise well-designed amplifier, either before optimal tuning conditions are obtained, or if the working conditions, i.e., load, drive power, and supply voltage are altered from their nominal magnitudes. Since mobile transmitters are often required to work properly or at least survive under heavily changing conditions the suppression of the spurious oscillations may become the most serious problem in the circuit design. Table I summarizes some experiments with the amplifier in Fig. 1.

A series of experimental collector voltages showing spurious oscillations is given in Fig. 2. It is notable that despite the highly different types of disturbances the resultant oscillations

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The author is with the Laboratory for Semiconductor Devices and Electronics Laboratory, Technical University of Denmark, Copenhagen, Denmark.

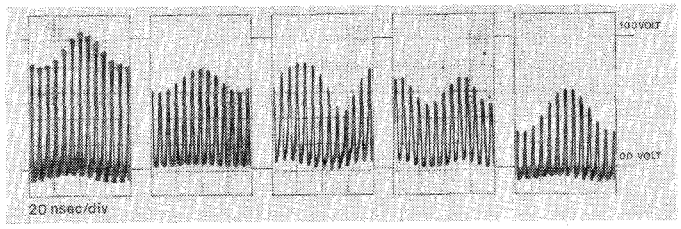


Fig. 2. Collector voltage waveshapes where the envelopes show spurious oscillations in the amplifier of Fig. 1 for $R_b = 470\ \Omega$. In (a)-(c) the oscillations are caused by mismatches of VSWR = 3 and 180°, 70°, -60° reflection angles, respectively. (d) is caused by a 3-dB reduction in the drive power, and (e) results from a halving of the supply voltage.

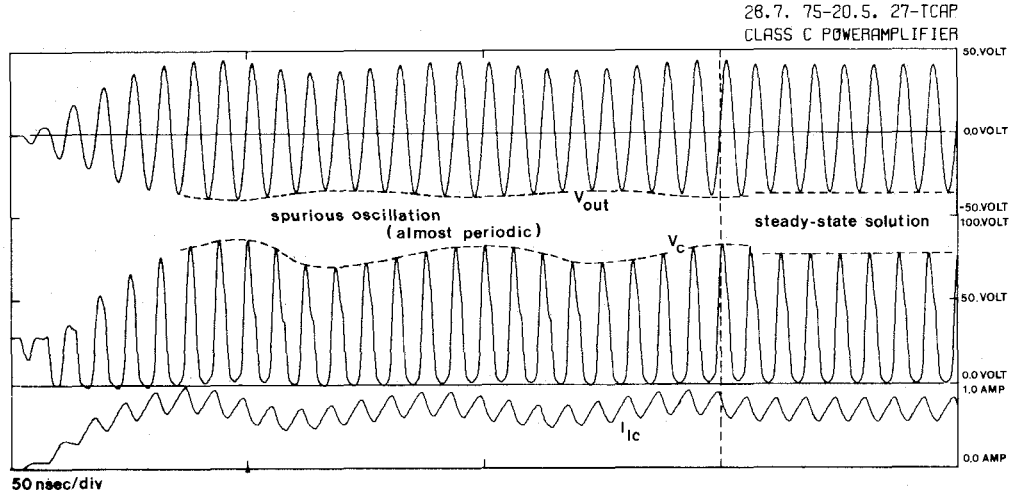


Fig. 3. Simulated response of the amplifier shown in Fig. 1 using $R_b = 470\ \Omega$ and nominal operation conditions. At the time given by the dashed line a numerical steady-state analysis is employed.

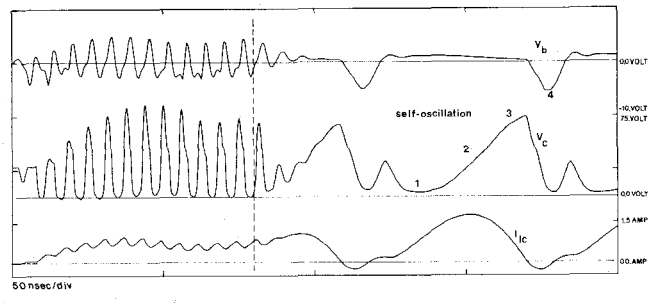


Fig. 4. Releasing of a self-oscillation in the amplifier by turning the signal generator off at the time given by the dashed line. During the course of the oscillation the transistor is thrown into operation modes of: 1) base widening, 2) combined high-field current saturation and base widening, 3) negative dc current gain provided by avalanche current in the collector junction, and 4) Zener breakdown in the emitter junction.

differ only moderately with respect to frequency. As will be discussed, the same basic phenomena are excited in all the cases.

The fundamental observation in this context is the existence of a self-oscillation in the circuit. Fig. 3 shows the computer simulated response of the amplifier using $R_b = 470\ \Omega$, correct load, and drive power. According to Table I this should result in a stable operation, but it is seen that a spurious oscillation is present as soon as the signal source is turned on. At the time which is indicated by the dashed line in the figure, a steady-state algorithm [11] has been applied in the computations. Since convergence is obtained within a signal period both a low-frequency modulated and a strictly periodic mode of operation exist in the circuit. The occurrence of spurious oscillations is therefore a question of whether the underlying self-oscillation is excited or not. This happens initially in the simulation where the signal source can be turned on instantly, whereas the actual amplifier requires a slight variation in, for instance, the drive power level.

Fig. 4 shows initially the same situation as Fig. 3, but after the first periods the signal source is turned off. Like the behavior of the experimental amplifier the circuit does not ring out but it continues in the self-oscillation. The course of the waveshapes will be discussed in the subsequent section.

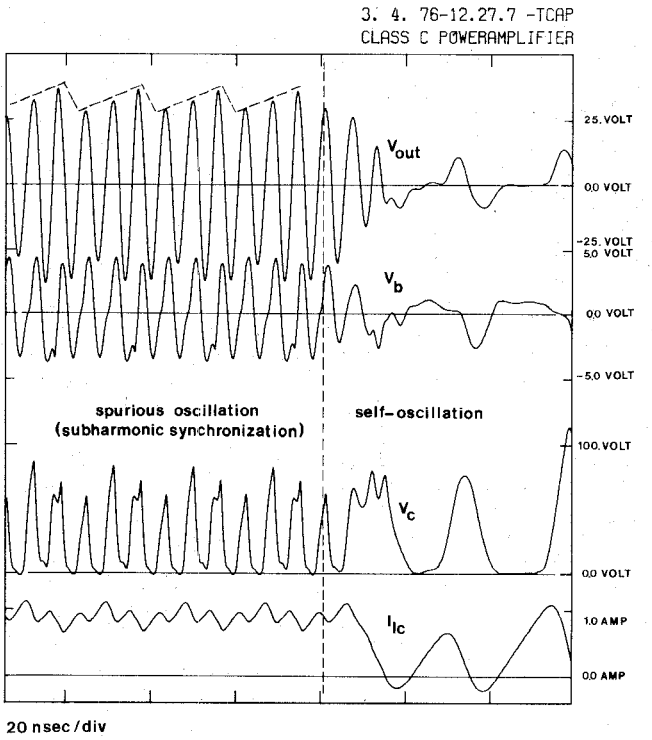


Fig. 5. Spurious oscillations in the amplifier of Fig. 1 using L_b = 20 nH, R_b = 50 Ω, and a slightly detuned output matching network which corresponds to a mismatch of VSWR = 2.2, -60°. At the time given by the dashed line, the generator is turned off and the self-oscillation becomes visible.

Here it should be noted that the oscillation is accompanied with a considerable power dissipation in the transistor, so both for the sake of stability and for the sake of avoiding transistor damage by second breakdown this oscillation should be suppressed.

Experiments and simulations on the amplifier in Fig. 1 have shown that every time spurious oscillations are excited, a self-oscillation of the type in Fig. 4 is also present in the circuit. The resultant oscillations have always taken forms among which the two extremes can be characterized.

1) Almost periodic oscillations [12]: If the frequency distance between the drive signal and the self-oscillation is relatively long, the effect of the drive signal may be considered as a smoothing of the distinct nonlinear properties in the circuit. The resultant modulation of the signal becomes thereby less typical than the isolation oscillation or it even disappears, an effect which is known and utilized in nonlinear control systems [13].

2) Subharmonic synchronization [12], [15][1]: If the drive signal is strong enough and if the frequency distance is sufficiently small the self-oscillation may synchronize to an integral multiple of the signal period.

The examples in Figs. 2-4 clearly show oscillations of the same type as in 1). Fig. 5 shows an oscillation of the same type as in 2) where a 3rd subharmonic results from a synchronization between the drive signal and the self-oscillation. It is seen in the figures that the two types of oscillations are the same as those which earlier have been ascribed to either "linear" or parametric instabilities. This distinction was, however, made from the assumption [2] that the amplifier could be considered as a superposition of a linear amplifier and a nonlinear amplifier, i.e., the point of view which commonly applies to systems with small nonlinearities [12]. The main purpose of the power amplifier is to utilize the highly nonlinear characteristics of the transistor for high efficiency amplification. Since it will be shown that the self-oscillation is due to the same nonlinear characteristics, the distinction above in 1) and 2) seems the most natural one when the stability problem, as here, is considered as a purely nonlinear problem.

III. The Self-Oscillation

The self-oscillation in the amplifier is localized to the simple bias network which remains if the two matching networks are removed, as shown in Fig. 6. In this circuit an oscillation can be excited by the breaking of a dc current path in the base choke. The resultant waveshapes from both simulation and experiment are shown in Fig. 7. Although some discrepancies with respect to the amplitudes are observable the two sets of curves reflect undoubtedly the same basic phenomena. Since the deviations are caused by the specific construction of the 2N3632 transistor[2], the computed results will be the main concern below and the highly simplified equivalent diagram in

[1] In literature, also often referred to as subharmonic entrainment, frequency demultiplication, and frequency division.

[2] The 2N3632 transistor is made of two paralleled chips. At high power levels the current tends to concentrate in one chip which causes a heavy distortion of the transistor characteristics [14]. This effect has not been included in the simulations.

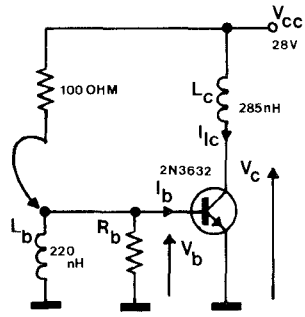
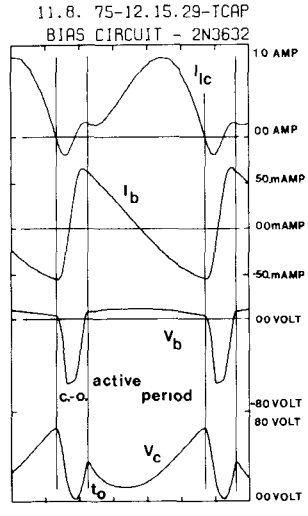
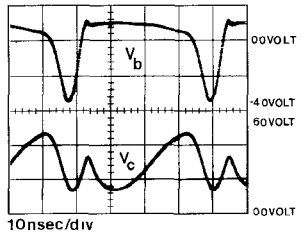


Fig. 6. Simple bias network where a self-oscillation can be excited by the break of a dc current through the base choke.



(a)



(b)

Fig. 7. (a) Simulated and (b) experimental waveshapes showing the self-oscillation in the bias network of Fig. 6. The oscillation can be subdivided into a period where the transistor is cutoff, c.-o., and a period where the transistor is active.

Fig. 8 will be used in the interpretation of the results. The following simplifications are made initially.

1) The collector capacitance can be modeled by a linear capacitor C_c and the collector voltage remains positive throughout the oscillation.

2) A linear capacitor C_e models the emitter capacitance when the transistor is cutoff. When the emitter charge Q_e exceeds the positive level Q_{eo}, the transistor turns active and the base voltage is fixed to the value V_{bo}.

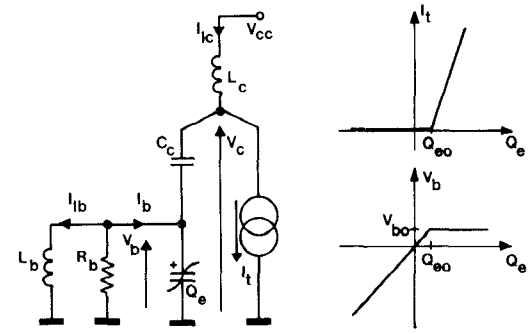


Fig. 8. (a) Equivalent circuit for the bias network. (b) and (c) The main nonlinear characteristics of the transistor.

3) The current through the transistor I_t is related to the emitter diffusion charge Q_{ed} by a constant transit time τ_f:

$$I_t = Q_{ed}/\tau_f. \tag{1}$$

When the transistor is active, the diffusion charge is given by

$$Q_{ed} = Q_e - Q_{eo}; \tag{2}$$

otherwise the diffusion charge is zero.

4) The transit time τ_f is assumed to be rather short in comparison with all the other characteristic times in the circuit.

5) The resistive base current contributions, i.e., the recombination, the avalanche, and the Zener breakdown currents are ignored.

Obviously these simplifications cannot provide the background for a genuine analytical treatment of the oscillation. This would require a much more comprehensive transistor model. What can be done is to achieve enough understanding of the dynamics of the oscillation from the simple model that a sufficient method of suppressing this can be extracted.

It is easily seen in Fig. 7 that the self-oscillation can be subdivided into a period where the transistor is active ($V_b \cong V_{bo}$) and a period where the transistor is cutoff ($V_b < V_{bo}$). The periods will be considered separately below but briefly the oscillation can be summarized as follows: during the active period an initial positive base current causes a charging of the collector capacitor. At the end of the active period the base current has the opposite sense. The discharge of the collector capacitor in the cutoff period forces a current through the base-emitter circuit which causes the base current to again go sufficiently positive to initiate a new active period.

A. The Active Period

The time, $t_o = 0$, where the transistor has just turned active, will be used as the starting point. According to the curves in Fig. 7 the initial state of the circuit can be summarized:

$$[I_b, I_{lc}, V_c, V_b]_{t_0} = [I_{bo}(>0), I_{lco}(>0), V_{co}(\cong V_{cc}), V_{bo}]. \tag{3}$$

Since the voltage across the base choke is fixed, the base current must be a linearly decreasing function of time, i.e.,

$$I_b = I_{bo} - (V_{bo}/L_b)t. \tag{4}$$

If it is assumed that the whole base current charges the collector capacitor, the collector voltage becomes

$$V_c = V_{co} - \int_0^t (I_b/C_c)\,dt = V_{co} - (I_{bo}/C_c)t + \tfrac{1}{2}(V_{bo}/L_bC_c)t^2. \quad (5)$$

Moreover, the transit current in the transistor must take the form

$$I_t = I_{lc} + I_b = I_{lco} + \int_0^t ([V_{cc} - V_c]/L_c)\,dt + I_b = I_{lco} + I_{bo} + ([V_{cc} - V_{co}]/L_c - V_{bo}/L_b)t + \tfrac{1}{2}\omega_c^2 I_{bo}t^2 - \tfrac{1}{6}(\omega_c^2 V_{bo}/L_b)t^3, \quad (6)$$

where

$$\omega_c = (L_cC_c)^{-1/2}.$$

The main contribution to I_t is given by I_{lc} since $|I_b| \ll I_{lc}$ throughout the active period. The shapes of the first-, second-, and third-order polynomials from (4)-(6) are easily recognized in Fig. 7 despite the crude approximations which led to the expressions. It should be noted that the assumption for (5) is equivalent with the assumption of a short transit time. In this case only an insignificant charging current to the emitter capacitor is required in order to control the diffusion charge which shapes the transit current according to (1). The short transit time can furthermore explain the apparent inconsistency in (6) which shows a transit current different from zero at $t = 0$. If the time t_{o-}, where the transistor just turns active because Q_e passes Q_{eo}, is used as a point of departure, the node equations for the base and the collector nodes provide

$$dQ_{ed}/dt + Q_{ed}/\tau_f - I_{lco} - I_{bo} = 0; \quad Q_{ed}(t_{o-}) = 0, \quad (7)$$

where the first term gives the emitter charging current and the second term is the transit current in the transistor. The current in the collector choke and the base current are taken as constants since the turn-on process is fast. Equation (7) has the solution

$$Q_{ed} = \tau_f I_t = \tau_f(I_{lco} + I_{bo})[1 - \exp([t_{o-} - t]/\tau_f)], \quad (8)$$

so due to assumption 4), the transit current practically jumps from zero to the sum of the initial currents, $I_{lco} + I_{bo}$. Before the transistor turned active these currents initiated the turn-on by charging the emitter capacitor.

The description of the active period is thereby complete, since the circuit behavior has been accounted for from the time where Q_e exceeds Q_{eo} to the time where the active period closes itself due to the negative third-order term in (6). By equating the two last and most significant terms in (6) the duration of the active period can be estimated:

$$t_c = 3L_b I_{bo}/V_{bo}. \quad (9)$$

Inserting t_c into (5) gives an estimate of the collector voltage at the time where the transistor becomes cutoff:

$$V_c(t_c) = V_{co} + V_{cx}; \quad V_{cx} = \tfrac{3}{2} L_b I_{bo}^2/V_{bo}C_c. \quad (10)$$

V_{cx}, the excess voltage, denotes the gain in collector voltage over the active period. The initial collector voltage, V_{co}, can finally be estimated by the assumption that the active period is longer than the cutoff period and from the requirement that the mean collector voltage must be equal to the supply voltage,

$$(1/t_c)\int_0^{t_c} V_c\,dt \cong V_{cc} \Rightarrow V_{co} \cong V_{cc}, \quad (11)$$

i.e., the initial voltage should lie in the range of the supply voltage, cf. Fig. 7.

The calculations above show that I_{bo} is the most significant parameter in the active period since this controls the duration of the period, the maximum transit current, and the final collector voltage. It is also clear that all the assumptions for the calculations are violated if I_{bo} is too great. The negative first-order term in (5) implies a possibility for base widening if the collector voltage falls to near-zero values. The main effect of base widening is a considerable rise of the transit time, which in turns requires that a great amount of charge has to be stored in the emitter capacitance. Thereby, the emitter charging current and the base recombination current may become the dominant components in the base current. The second-order term in (6) may give rise to current levels where the high-field current saturation in the collector epitaxial layer becomes appreciable. In this situation much of the collector-base voltage is dropped across the collector bulk region so the intrinsic transistor is forced into base widening. Finally, the second-order term in (5) together with (9) may result in high collector voltages where the avalanche-generated current between the collector and the base has to be taken into account. The main effect of this is that current is taken from the transit current I_t which accelerates the close of the active period. The oscillation in Fig. 4 is an example where all these phenomena occur in sequence and strongly influence both the amplitude and the duration of the active period. In this case the simplified treatment is inadequate. The situation which has been studied is, however, generally useful as a limit case since all the possibilities which have been excluded imply that (10) overestimates the excess collector voltage for a given initial base current. The possible mappings of I_{bo} into V_{cx} provided by the active period will therefore lie in the hatched region of the I_{bo}, V_{cx} plane in Fig. 9.

B. The Cutoff Period

In the cutoff period where the current generator I_t is absent the network reduces to a passive, linear circuit imposed by some initial conditions which can be summarized:

$$[I_{lb}, I_{lc}, V_c, V_b]_{t_c} = [I_{lbc}(\gtrsim 0), I_{lcc}(\cong 0), V_{cc} + V_{cx}, V_{bo}], \quad (12)$$

where the current in the base choke is related to the base current by

$$I_b = I_b(V_b, I_{lb}) = -I_{lb} - V_b/R_b. \quad (13)$$

For the types of transistors in question the inequality $C_e > C_c$ applies. If it is assumed, moreover, that the resonance frequency of the base-emitter circuit is less than the resonance

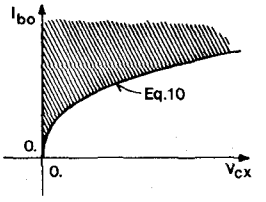


Fig. 9. I_{bo}, V_{cx} plane showing the possible mappings of I_{bo} into V_{cx} provided by the active period of the self-oscillation.

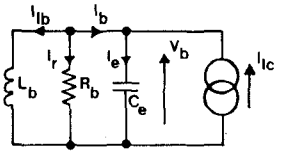


Fig. 10. Equivalent diagram for the base-emitter circuit in the cutoff period.

frequency of the collector series circuit, i.e.,

$$\omega_e = (L_b C_e)^{-1/2} < \omega_c, \tag{14}$$

the mode of the series circuit becomes practically unaffected by the parallel circuit L_b, R_b, and C_e. The current in the collector choke can thereby be approximated:

$$I_{lc} = -\omega_c C_c V_{cx} \sin(\omega_c t), \tag{15}$$

where the onset time for the cutoff period has been set to zero. The situation seen from the parallel circuit is depicted in Fig. 10 where the effect of the series circuit is given by the sinusoidal current generator. The response of the circuit has three components:

1) the steady-state response from the generator,
2) the transient response from the generator turn-on,
3) the transient response from the initial conditions.

If a sustained oscillation takes place the first two contributions are dominant and only these will be considered. The initial state of the circuit is therefore assumed to be $(V_b, I_{lb}) = (0, 0)$. The impedance of the circuit can be written in the form:

$$V_b/I_{lc} = j\omega_c L_b(1 - \delta^2 + j2\zeta\delta)^{-1}, \tag{16}$$

where ζ is the damping coefficient, and δ denotes the resonance frequency ratio, i.e.,

$$\zeta = \tfrac{1}{2}(L_b/C_e)^{1/2}/R_b; \quad \delta = \omega_c/\omega_e. \tag{17}$$

The steady-state response is illustrated by the phasor diagram in Fig. 11. From straightforward calculations using (15)-(17) the amplitudes of V_b and I_{lb} are found

$$V_B = C_c\delta^2 V_{cx}/C_e\Delta; \quad I_L = \tfrac{1}{2} C_c\delta V_{cx}/R_b\zeta C_e\Delta, \tag{18}$$

where

$$\Delta = (\delta^4 + 2\delta^2(2\zeta^2 - 1) + 1)^{1/2}. \tag{19}$$

The steady-state response describes an ellipse with the half-axis

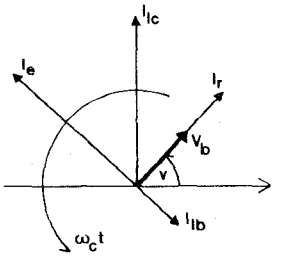


Fig. 11. Phasor diagram illustrating the initial conditions for the steady-state response in the base-emitter circuit–Fig. 10.

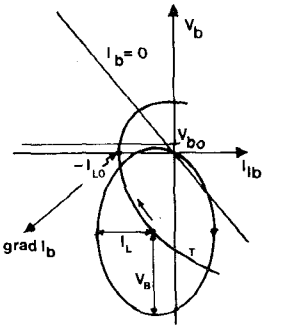


Fig. 12. V_b, I_{lb} phase plane for the base-emitter circuit–Fig. 10. The total response is combined from the steady-state ellipse and the transient trajectory T.

V_B and I_L in a V_b, I_{lb} phase plane, Fig. 12. The origin of the ellipse moves along a trajectory which, according to the zero-initial state assumption, goes through the point:

$$(V_b, I_{lb}) = (-V_B \cos v, -I_L \sin v); \tag{20}$$

$$\cos v = (\delta^2 - 1)/\Delta; \quad \sin v = 2\delta\zeta/\Delta. \tag{21}$$

The state equations for the unforced circuit can be written

$$dI_{lb}/dt = V_b/L_b; \quad dV_b/dt = -I_{lb}/C_e - 2\zeta\omega_e V_b, \tag{22}$$

so the trajectory is governed by

$$dV_b/dI_{lb} = -4\zeta^2 R_b(1 + R_b I_{lb}/V_b), \tag{23}$$

where (17) has been used. It is seen from (23) that the trajectory crosses the negative I_{lb} axis at a right angle. The crossing point, which will be denoted $(0, -I_{L0})$, is the leftmost point of the trajectory. The most negative value of I_{lb} due to the joint effect of the transient and the steady-state responses therefore becomes

$$\min I_{lb} \geqq -(I_L + I_{L0}) = -(\tfrac{1}{2} V_{cx}C_c/R_b C_e) f(\zeta, \delta), \tag{24}$$

where the last equation is derived in the Appendix. The function $f(\zeta, \delta)$ is shown in Fig. 13. According to the direction of the I_b gradient in the phase plane, Fig. 12, the maximum base current at the time where the transistor turns active for $V_b = V_{bo}$ must be restricted by the inequality [cf. (13)]

$$\max I_{bo} \leqq I_b(V_{bo}, -I_L - I_{L0}) = (V_{bo}/R_b) \cdot (\tfrac{1}{2} V_{cx}C_c f(\zeta, \delta)/V_{bo}C_e - 1). \tag{25}$$

The possible mappings of V_{cx} into I_{bo} implied by the cutoff

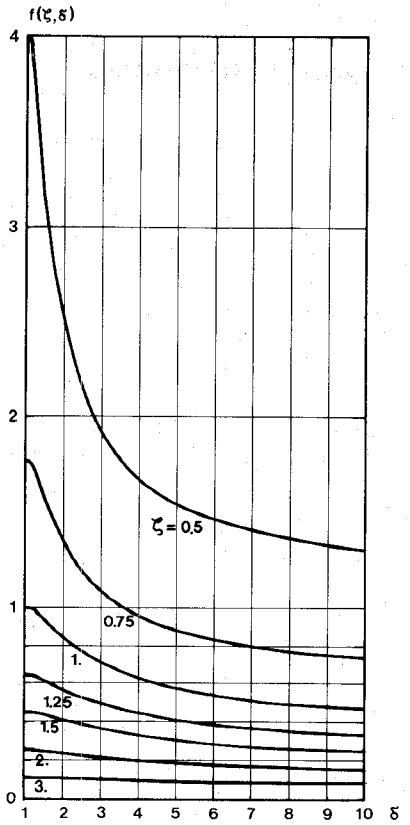


Fig. 13. The function $f(\zeta, \delta)$ in (24), (25), and (27).

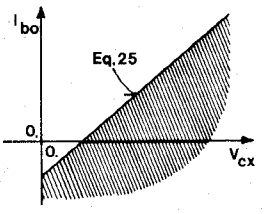


Fig. 14. I_{bo}, V_{cx} plane showing the possible mappings of V_{cx} into I_{bo} provided by the cutoff period of the self-oscillation.

period lie, therefore, in the hatched region of the I_{bo}, V_{cx} plane in Fig. 14 where the boundary is given by a straight line.

The possibility for emitter breakdown has been disregarded in the calculations. Emitter breakdown does not affect the validity of the inequality above because a limitation of the negative V_b amplitude in turn keeps dI_{1b}/dt limited. Thereby a smaller I_{bo} than the one given by the right-hand side of (25) is obtained.

This finishes the discussion of the cutoff period. If the curves of Fig. 7 are considered, the sinusoidal shapes of the currents and voltages are easily recognized. The experimental curves are especially distinct because the excess voltage is lowered by the power concentration phenomenon in the 2N3632 transistor. In the simulation an emitter breakdown results because the excess voltage here is somewhat greater and therefore forces more current through the base-emitter circuit.

IV. Suppression of the Self-Oscillations

A sustained oscillation must clearly imply an excess voltage and an initial base current which lie in the region common to the mappings in Fig. 9 and Fig. 14. By adjusting the parameters ζ, δ the minimum V_{cx} in this region may be moved towards higher magnitudes, but due to the shapes of the boundary curves a common region will always exist. A physical limitation must therefore be introduced, and since the collector avalanche breakdown voltage V_{ac} provides the uppermost collector voltage, this should be used. The maximum excess voltage becomes

$$\max V_{cx} \equiv V_{CX} = V_{ac} - V_{cc}. \tag{26}$$

Insertion of V_{CX} in both (10) and (25) and equating the resultant magnitudes of I_{bo} must lead to a condition where no self-oscillation can be sustained in practice. Using (17) the

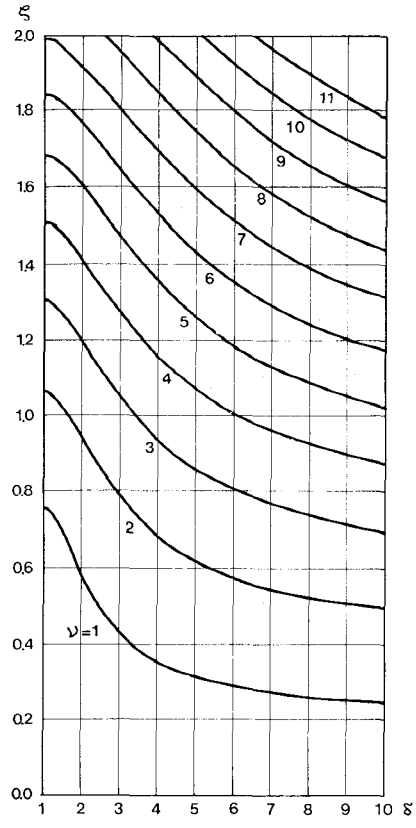


Fig. 15. Contours showing the solutions to (26) using ν as parameter. For a given ν the magnitudes of ζ, δ, which assure suppression of the self-oscillation, lie above the corresponding contour.

TABLE II
EXAMPLES SHOWING ESTIMATED AND EXPERIMENTAL CONDITIONS FOR THE SUPPRESSION OF THE SELF-OSCILLATION

Transistor Data	C_e	C_c	V_{bo}	V_{ac}	ν	BV_{CES}
2N3632	78 pF$\|_{3V}$	13 pF$\|_{28V}$	~1 V	110 V	6.83$\|_{28V}$	65 V
2N5642[a]	150 pF$\|_{3V}$	30 pF$\|_{28V}$	~1 V	100 V	7.20$\|_{28V}$	65 V
2N6082[a]	390 pF$\|_{3V}$	120 pF$\|_{12V}$	~1 V	55 V	6.61$\|_{12V}$	36 V

	Estimation (sufficient criterion)					Experiment (limits for suppression)				
	δ	ζ	L_b[nH]	L_c[nH]	R_b[Ω]	δ	ζ	L_b[nH]	L_c[nH]	R_b[Ω]
2N3632	2.15	1.88	220	285	14.1	2.15	1.02	220	285	26
2N5642	5.90	1.50	452	65	18.0	5.04	1.30	330	65	18
2N6082	3.07	1.74	160	55	5.85	3.07	1.13	160	55	9

[a]Modern emitter ballasted RF-power transistors.

suppression condition becomes

$$\zeta(\nu f(\zeta, \delta) - 1) - (\tfrac{1}{3}\nu)^{1/2} = 0; \tag{27}$$

$$\nu = \tfrac{1}{2} V_{CX} C_c / V_{bo} C_e. \tag{28}$$

The major property of (27) is that the question of stability can be answered in the relative, frequency independent terms ζ, δ and a parameter, ν, which depends solely on properties of the transistor. Therefore, a solution to (27) using ν as a parameter can be generally useful in design. The contours in Fig. 15, which are obtained by numerical methods, show the solution. For a given ν the values of ζ, δ which lie over the corresponding contour should imply that the oscillation cannot be sustained. Thereby the problem of suppressing the oscillation reduces to that of estimating ν.

In Table II some results concerning the utilization of Fig. 15 are summarized. It is seen initially that in agreement with the expectations sufficient conditions are obtained from the estimations in all cases. According to the assumptions for (27), the discrepancies between experiments and estimations arise from three major reasons.

1) The maximum collector voltage does not reach the avalanche breakdown voltage in practice but lies commonly in

the range above the collector–emitter breakdown voltage BV_{CES}.

2) The emitter breakdown often accompanies the backswing in the cutoff period.

3) The actual resonance frequency ratio implies that the worst case current given by (24) cannot be reached when the transistor turns active.

At the present level of analytical development these additional phenomena occur in an unpredictable manner. Future investigations concerning the self-oscillation should therefore take both the direction of providing a better theoretical background and a practical investigation showing whether it is possible to associate a function $\nu = \nu(V_{cc})$ to each transistor type. In connection with Fig. 15 such a function would give the designer the necessary information for an *a priori* suppression of the oscillation.

V. Discussions and Conclusions

If the amplifier circuit of Fig. 1 is considered, two problems appear in connection with the suppression of the self-oscillation. These are the question of whether the suppression can be carried out generally for all working conditions of the amplifier and the question of whether a suppression will imply a reduction of the circuit performance with respect to gain and output power.

The inclusion of the matching networks, the generator impedance, and a possibly mismatched load will clearly change the conditions for the self-oscillation, as illustrated by the differences between the oscillations in Figs. 4 and 7. Experiments have shown that if the period of the self-oscillation is long, as in Figs. 2-4, there are practically no differences between the suppression conditions for the bias network alone and the resultant amplifier. As shown in Table I the amplifier of Fig. 1 could be stabilized for all working conditions. According to (9) and (25) this situation is obtained by means of a relatively large base choke, L_b. For a low frequency self-oscillation the effects of the matching networks and possible mismatches correspond to small variations in δ. It is seen from Table II and Fig. 15 that the suppression criterion is insensitive to δ-variations in the practical range of dampings. The closer the frequency of the self-oscillation comes to the signal frequency, where the matching networks are tuned and where the collector load depends heavily on the load impedance, the more unpredictable becomes the mode of the self-oscillation in the complete amplifier. In this case spurious oscillations of the subharmonic type in Fig. 5 are the most likely to be excited.

The observations above lead in a natural way to the parallel method of damping the base choke, considered in this paper. The criterion in Fig. 15 restricts only ζ and δ so the damping resistance may be determined from the requirement that the gain should not be reduced more than tolerably. The reduction is found *a priori* since the RF input resistance of the transistor is often specified in the data sheets. For a given value of R_b the base choke L_b can be adjusted to meet the suppression criterion. On the basis of the discussion above it is seen that the two goals are followed simultaneously when L_b is enlarged. Firstly (17) shows that the necessary damping for suppression is approached and secondly, the period of the self-oscillation is made long so the stability is maintained under changing working conditions. No damping of the collector choke is prescribed and the amplifier can be stabilized without losses in collector efficiency and output power.

By taking the self-oscillation of the bias network into account, it has been possible to explain how some often observed instabilities in RF-power amplifiers can arise and to specify a well-founded method for stabilization. It is therefore concluded that one of the difficulties in design has been removed and it is supposed that this new insight may throw new light on other unsolved problems in RF-power amplifier constructions, for instance in areas of transistor paralleling and intermodulation.

Appendix

Derivation of (24)

Introduction of the variables

$$x = \omega_e L_b I_{lb}, \quad z = V_b/x, \tag{29}$$

transforms (23) to [using (17)]:

$$dx/x = -z(z^2 + 2\zeta z + 1)^{-1}\, dz = -h(z)\, dz. \tag{30}$$

The solution to (30) is given by

$$x = C \exp(-g(z)); \quad g(z) = \int h(z)\, dz. \tag{31}$$

The constant C is determined from initial conditions x_o, z_o, so the final solution can be expressed

$$x/x_o = \exp(g(z_o) - g(z)), \tag{32}$$

where the function $g(z)$ can be found in standard integral tables:

$$P(z) = z^2 + 2\zeta z + 1, \quad q = \begin{cases} (1-\zeta^2)^{1/2}; & \zeta < 1 \\ (\zeta^2 - 1)^{1/2}; & \zeta > 1 \end{cases}$$

$$\zeta < 1: \quad g(z) = \tfrac{1}{2} \ln P(z) - \zeta \tan^{-1}([z+\zeta]/q)/q; \tag{33}$$

$$\zeta > 1: \quad g(z) = \tfrac{1}{2} \ln P(z) - \tfrac{1}{2}\zeta \ln([z+\zeta-q]/[z+\zeta+q])/q; \tag{34}$$

$$\zeta = 1: \quad g(z) = \ln(z+1) + 1/(z+1). \tag{35}$$

Referring back to the original variables V_b and I_{lb}, using $V_b = 0$ and (20) and (21) gives

$$I_{Lo} = I_{lb}\big|_{V_b=0} = \exp(g(z_o) - g(0)) \sin \upsilon I_L, \tag{36}$$

where

$$z_o = V_B \cos \upsilon/\omega_e L_b I_L \sin \upsilon = \tfrac{1}{2}(\delta^2 - 1)/\zeta. \tag{37}$$

The addition of (18) to (37) results finally in (24):

$$I_L + I_{Lo} = \tfrac{1}{2}(V_{cx} C_c / R_p C_e) f(\zeta, \delta); \tag{38}$$

$$f(\zeta, \delta) = (\delta/\zeta\Delta)(1 + 2\delta\zeta \exp[g(z_o) - g(0)]/\Delta).$$

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References

[1] J. Choma, Jr., "Instabilities in class C transistor amplifiers," in *Proc. 12th IEEE Midwest Symp. Circuit Theory*, New York, pp. X.2.1-6, 1969.

[2] O. Müller and W. G. Figel, "Stability problems in transistor power amplifiers," *Proc. IEEE*, vol. 55, pp. 1458-1466, Aug. 1967.

[3] J. Mulder and J. M. Siemensma, "All solid state transmitters for the 160 MHz band using silicon-planar epitaxial overlay transistors," N. V. Philips' Gloeilampenfabrieken, Eindhoven, The Netherlands, Appl. Infor. 526, 1969.

[4] J. Mulder, "On the design of transistor R.F. power amplifiers," *Electron. Appl.*, vol. 27, pp. 155-171, 1966.

[5] J. Olmstad *et al.*, "High level current gain in bipolar power transistors," *RCA Rev.*, vol. 52, pp. 339-371, Sept. 1971.

[6] R. J. Whitter and D. A. Tremere, "Current gain and cutoff frequency falloff at high currents," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 39-57, Jan. 1969.

[7] D. L. Bowler and F. A. Lindholm, "High current regimes in transistor collector regions," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 257-263, Mar. 1973.

[8] J. Vidkjaer, "Large signal transistor modeling with applications to investigations of RF-power amplifier behavior," Ph.D. dissertation, Electron. Lab., Tech. Univ. Denmark, Dec. 1974.

[9] R. Rejhall, "Systemizing RF power amplifier design," Motorola Semiconductor Products, Inc., Phoenix, AZ, Appl. Note AN-282.

[10] F. Davis, "Matching network designs with computer solutions," Motorola Semiconductor Products, Inc., Phoenix, AZ, Appl. Note AN-267.

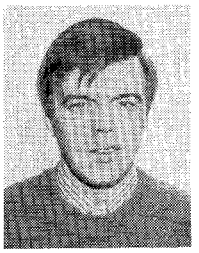
[11] T. J. Aprille and T. N. Trick, "Steady-state analysis of nonlinear circuits with periodic inputs," *Proc. IEEE*, vol. 60, pp. 108-114, Jan. 1972.

[12] C. Hayashi, *Nonlinear Oscillations in Physical Systems.* New York: McGraw-Hill, 1964.

[13] D. Šiljak, *Nonlinear Systems.* New York: Wiley, 1969, ch. 5.

[14] B. Becciolini, "Using balanced emitter in RF applications," Motorola Semiconductor Products, Inc., Phoenix, AZ, Appl. Note AN-521.

[15] T. E. Stern, *Theory of Nonlinear Networks and Systems.* Reading, MA: Addison-Wesley, 1965.



Jens Vidkjaer (M'69-S'72-M'72) was born in Copenhagen on May 13, 1943. He received the M.S. degree in electrical engineering in 1968 and the Ph.D. degree from the Technical University of Denmark, Copenhagen, in 1975.

After military service he joined the Electronics Laboratory at the Technical University of Denmark in 1970 where he was engaged in numerical circuit analysis, transistor modeling, and RF-power amplifier investigations. He is currently with the Laboratory for Semiconductor Devices and Electronics Laboratory, Technical University of Denmark, working in the area of computer-aided design.

The Effect of Base Contact Position on the Relative Propagation Delays of the Multiple Outputs of an I^2L Gate

DAVID V. KERNS, JR., MEMBER, IEEE

Abstract—**The multiple collectors of an I^2L gate do not slew simultaneously, giving different propagation delays for the various outputs; the relative positions of the base contact, the injector, and the collector outputs affect these delays. In this paper, three possible configurations are modeled, simulated, and the results summarized.**

Introduction

INTEGRATED injection logic (I^2L) or merged transistor logic (MTL) has received considerable attention since it was introduced in 1972 [1], [2]. The now well-known structure in which a lateral p-n-p current source is merged with an inverted n-p-n device with multiple collectors (see Fig. 1) is challenging both conventional bipolar and MOS technologies in many applications.

The more or less standard layout for I^2L circuitry is that shown in Fig. 2, where gates are placed along both sides of an injector stripe. This arrangement provides high packing density and ease of layout, since metal routes can be placed over unused positions in neighboring cells. Within a gate, the designer has the freedom to place the base contact at any of the cell positions, the position chosen usually governed by metal routing constraints.

In designing any digital system, certain critical paths require a knowledge of the gate propagation delays. For I^2L gates, the minimum propagation delay has been shown approximately proportional to fan out [3]; however, for a given gate, the propagation delays from input to each of the multiple out-

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The author is with the Department of Electrical Engineering, Auburn University, Auburn, AL 36830.