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Digital Demodulator for Wide Bandwidth SAR

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ABSTRACT

A novel approach to the design of efficient digital quadrature demodulators for wide bandwidth SAR systems is described. Efficiency is obtained by setting the intermediate frequency to 1/4 the ADC sampling frequency. One channel is made filter-free by synchronizing the local oscillator with the output decimator. The filter required by the other channel is optimized through global search using the system level performance metrics integrated sidelobe level ratio (ISLR) and peak sidelobe level ratio (PSLR).

INTRODUCTION

The traditional analog quadrature demodulator with analog-to-digital converters (ADCs) is illustrated in Fig. 1. The intermediate frequency input signal, $s(t)$, is mixed with the local oscillator and a 90 degree delayed version of the same thus providing the two orthogonal channels known as the in-phase (I) channel and the quadrature-phase (Q) channel. The mixer outputs are lowpass filtered to remove the high frequency components and also any local oscillator signal which may be present due to imperfect mixers. The filter outputs are thus bandlimited according to Nyquist and subsequently fed to the ADCs for conversion.

Wide bandwidth analog demodulators suffer from mismatches between the I and Q channel transfer functions. ADC transfer characteristics contribute to the channel mismatch. Phase errors between the local oscillator mixer inputs resulting in a non-perfect orthogonality is also detrimental to performance. Finally, technology issues make it difficult to achieve wide bandwidths and good low frequency performance at the same time.

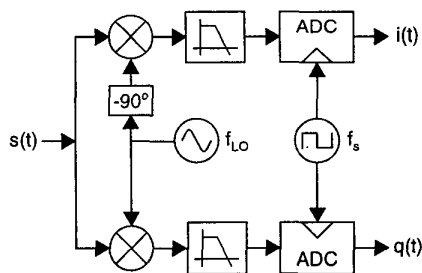


Fig. 1: Analog demodulator principle.

The availability of wide bandwidth ADCs has made it feasible to push the analog-digital boundary from base-band to the intermediate frequency range in SAR systems with bandwidths approaching 1GHz. The quadrature demodulation may be performed in the digital domain and the digital counterpart of the analog demodulator is shown in Fig. 2. The impulse response, $h(n)$, corresponds to the bandlimiting lowpass filters of Fig. 1. The filters are followed by a decimation function which reduces the data rate. ADC mismatch is not an issue for the digital demodulator since only one ADC is required. Also, the DC offset of the ADC(s), which must be dealt with for analog demodulation, is not a problem for the digital demodulator because it lies outside of the signal frequency band. Since the I and Q channels of the demodulator reside in the digital domain it is possible to achieve perfect channel transfer function matching. Perfect orthogonality may be achieved since the local oscillator mixer input signals are digitally generated and the mixers themselves are simple digital multipliers. Finally, the digital demodulator does not have any low frequency problems. The main advantage of analog demodulation over digital demodulation resides in ADC fidelity performance. ADC fidelity performance typically degrades as bandwidths increase and analog demodulators only require half the bandwidth of digital demodulators. Emerging ADCs seem to offer adequate fidelity performance for digital demodulation schemes up to bandwidths of 1GHz.

DIGITAL DEMODULATOR

Fig. 2 illustrates the general principle of the digital demodulator. The main design challenge is to provide a computationally efficient solution which meets a set of requirements.

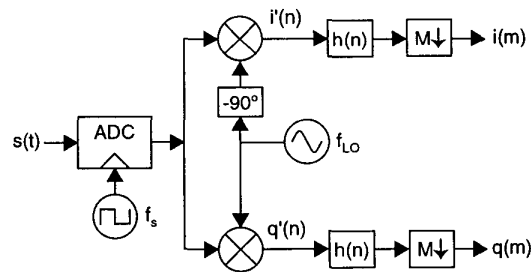


Fig. 2: Digital demodulator principle.

The most commonly used technique for providing an efficient implementation involves selecting the intermediate frequency and thus the local oscillator (LO) frequency to be 1/4 of the ADC conversion frequency. With the local oscillator signal, $g(nT)$, given by (1), the I-channel mixer LO input simply becomes a sequence of 1,0,-1,0... , and the Q-channel mixer LO input becomes a sequence of 0,-1,0,1... . The LO signal generation is now a trivial digital operation and the multipliers implementing the mixers are reduced to a circuit that simply passes, zeros or changes the sign of the data.

$$g(nT) = -\sin(2\pi f_{LO}nT) \quad (1)$$

Consider the situation where a single pulse is transmitted and reflected from a scene containing only one point target. If the complex modulation function, $m(t)$, is given by (2), then the demodulator input, $s(t)$, may be expressed as (3) where arbitrary amplitude and phase constants relating to the radar cross section and position of the target are omitted for convenience.

$$m(t) = a(t) \cdot \exp^{j\phi(t)} \quad (2)$$

$$s(t) = a(t) \cdot \cos(2\pi f_{LO}t + \phi(t)) \quad (3)$$

The sampled version of (3), on the ADC output, is expressed by (4).

$$s(nT) = a(nT) \cdot \cos\left(\frac{\pi n}{2} + \phi(nT)\right) \quad (4)$$

The mixer outputs, $i'(nT)$ and $q'(nT)$, may be expressed as (5) and (6) respectively.

$$i'(nT) = \frac{a(nT)}{2} \cdot [\cos(\phi(nT)) + (-1)^n \cos(\phi(nT))] \quad (5)$$

$$q'(nT) = \frac{a(nT)}{2} \cdot [\sin(\phi(nT)) - (-1)^n \sin(\phi(nT))] \quad (6)$$

The mixer output expressions, (5) and (6), have a baseband component and a high frequency component located at twice the local oscillator frequency. Removing the high frequency components from both channels results in the original complex modulation function.

When maximum bandwidth is required, the decimators of Fig. 2 will decimate by two. When no lowpass filtering is performed, an important feature of equations (5) and (6), relating to the phase of the decimator operation, is seen. The decimator phase will result in the selection of the even samples or the odd samples, thus resulting in (7).

$$r(m) = \begin{cases} 1/2 [m(m) + m^*(m)] & \text{if even samples} \\ 1/2 [m(m) - m^*(m)] & \text{if odd samples} \end{cases} \quad (7)$$

Thus (7) shows that the correct result will be available on the I or Q channel depending on the phasing of the decimator and the other channel will be zero. Correctly phasing the decimator reduces the complexity of the demodulator by effectively removing one of the lowpass filters. The remainder of this paper

assumes that the decimator selects even samples thus eliminating the I channel filter.

The performance of the digital demodulator is now reduced to the design of the Q channel filter.

THE LOWPASS FILTER

Traditionally the design of the filters in a quadrature demodulator strives towards lowpass filters with linear phase and very little ripple in the passband region and large suppression in the stopband region. This design strategy is standard for analog quadrature demodulators and most often applied to digital implementations as well. However, a simpler and more direct approach exists when designing in the digital domain.

Consider a Q channel finite impulse response (FIR) filter $h(n)$ of length N, where N is odd. Also, assume that the FIR filter is symmetrical thus providing linear phase. The Q channel output may be calculated as the convolution of $h(n)$ with (6) followed by a decimation of M. Under the assumption that M is even (typically 2) the Q channel output may be expressed as (8).

$$q(m) = \sum_{k=0}^{N-1} h(k) \left[1 - (-1)^k \right] \frac{a(m-k)}{2} \sin(\phi(m-k)) \quad (8)$$

Equation (8) shows that the wanted Q channel signal is effectively filtered by a linear phase filter, $h_{eff}(n)$, given by (9).

$$h_{eff}(n) = h(n)[1 - (-1)^n] \quad (9)$$

The simple and intuitive interpolation of (9) is that $h_{eff}(n)$ corresponds to the difference between the original filter $h(n)$ and its highpass equivalent. No phase imbalances exist between the I and Q channels and the performance of the digital quadrature demodulator is only degraded by the amplitude imbalance introduced by $h_{eff}(n)$. A filter optimized for best amplitude match could now be found, however, this paper chooses to optimize the filter for metrics which are more directly related to the SAR system performance.

PERFORMANCE METRICS

The two primary metrics of concern are the peak sidelobe ratio (PSLR) and the integrated sidelobe ratio (ISLR). The PSLR is defined as the ratio between the maximum peak outside the mainlobe and the maximum peak within the mainlobe. A poor PSLR results in unwanted ghost images. The ISLR is defined as the ratio between the power outside of the mainlobe and the power within the mainlobe. The ISLR is an indication of the amount of power leaking from the mainlobe to the sidelobes. A target with a radar cross section of X_x will in effect mask out targets in the vicinity with radar cross sections less than $X_x + ISLR$.

The performance metrics are defined on the compressed pulse. Compression is generally accomplished by filtering the output of the demodulator with a weighted matched filter. This paper adopts the Hamming weight function as a reference because of its widespread use in SAR processing.

Note that imaging SAR systems output images which are 2-dimensional by nature and that the PSLR and ISLR are normally evaluated in this 2-dimensional space. This paper only considers the range dimension and assumes that the ISLR is 3dB lower when evaluated in the 1-dimensional range space. The design requirements and goals used in this paper, Table 1, are adopted from SAR systems previously developed at the Department of Electromagnetic Systems.

Table 1: Design Requirements & Goals [1].

	PSLR	ISLR
Required	-30dB	-21dB
Goal	-40dB	-31dB

FILTER OPTIMIZATION

This paper chooses a rather simple strategy for filter optimization which relies on brute-force computing. A global search for filter coefficients is performed using the calculation of PSLR and ISLR as the selection and stop criteria.

The search space is limited by constraining the coefficient word length and the filter length. The search is initiated by attempting all permutations of coefficients with only one bit set. The search continues by adding one extra bit at a time until the performance results are adequate. The stop criteria is set as $PSLR \leq -40dB$ and $ISLR \leq -31dB$. Table 2 shows the search results for filter length $N \leq 15$ and coefficients word length $W \leq 8$ bits. The amplitude responses for the filters are shown in Fig. 3. The search for the best filters was carried out on an SGI Power Challenge using 8 processors and completed in 1.5 hours.

Table 2: Search results. Performance and filter coefficients.

	PSLR [dB]	ISLR [dB]	$h_1, -h_3, h_5, -h_7$
1	-42.6	-32.2	0x26, 0x08, 0x02, 0x00
2	-42.5	-32.2	0x27, 0x08, 0x02, 0x00
3	-43.5	-32.2	0x28, 0x0a, 0x03, 0x00
4	-42.8	-31.9	0x28, 0x0a, 0x04, 0x01
5	-40.8	-31.2	0x26, 0x06, 0x01, 0x00
6	-40.9	-31.2	0x25, 0x06, 0x01, 0x00
7	-40.1	-31.2	0x29, 0x0c, 0x04, 0x00

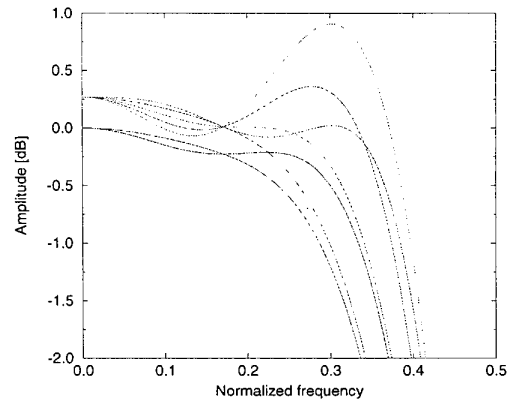


Fig. 3: Amplitude response of Q channel transfer function.

CONCLUSION

The design strategy for digital demodulators set forth has yielded very efficient implementations guaranteeing adequate PSLR and ISLR performance. The results of Table 2 indicates that a complete digital demodulator may be constructed with as few as 7-9 adders operating at half the conversion rate. This result allows digital quadrature demodulators with GHz bandwidths to be implemented in modest sized ASICs. The residual channel amplitude mismatch may be removed with no overhead in a pulse compression system following the demodulator thus effectively providing a perfect quadrature demodulation.

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