Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology

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Ph.d. Thesis, August 2010

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Preface

The Ph.D. project "Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology" was carried out under the Ph.D. school at "DTU Elektro" at the "Technical University of Denmark" in Kongens Lyngby in close collaboration with the amplifier group from "Harman/Becker Automotive Systems GmbH" in Straubing, Germany. During the project, a research visit was carried out at the "Power Electronics Systems Laboratory" at the "Eidgenössische Technische Hochschule" in Zürich. During the project time, I had the pleasure to meet and discuss with many specialists in the field. Special thanks goes to

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- the colleagues at "Harman/Becker Automotive Systems GmbH", for keeping my research efforts practically relevant,
- the colleagues Gerald Stanley at "Crown International Inc." and David

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- the “Power Electronics Systems” group at the ETH Zürich for showing me world-class approaches to build even better switch-mode power electronics.

Summary

Switch-mode power electronics is disturbing other electronic circuits by emission of electromagnetic waves and signals. To allow transmission of information, a set of regulatory rules (electromagnetic compatibility (EMC)) were created to limit this disturbance. To fulfill those rules in power electronics, shielding and filtering is required, which is limiting the size reduction. The motivation for this project was to find alternative ways to avoid trouble with interference of switch-mode power electronics and transmission and receiver circuits. An especial focus is given to audio power amplifiers.
After a historical overview and description of interaction between power electronics and electromagnetic compatibility (chapter 1), the thesis will first show the impact of the high frequency signals on the audio performance of switch-mode audio power amplifiers (chapter 2). Therefore the work of others will be put into perspective and self-oscillating amplifiers will be compared with external synchronized topologies.
After that, solutions to the problem, which are widespread in industry will be given and explained (chapter 3). The challenges and advantages will be described.
The improvement of the described problem where four different approaches:

- Multi Carrier Modulation (MCM)
- Active Electromagnetic Cancellation (AEC)
- Current Driven Power Stages (CDP)
- Radio Frequency Power Electronics (RF SMPS)

Multi Carrier Modulation (chapter 4) is using more than one external carrier and generating multiple PWM signals. Those are combined by a logic circuit to one pulse coded information stream. The average of this stream is

proportional to the modulated signal, while the spectral peaks of the switching frequencies are half compared to state-of-the art pulse width modulation (PWM).
Active Electromagnetic Cancellation (chapter 5) has been known as active filtering in power electronics. It has been applied to switch mode audio power amplifiers. The specialty for the later will be described and a design is shown, decreasing the undesired spectrum by 15 dB.
A different approach to tackle the problem is given by an alternative power stage in Current driven Power Stages (chapter 6). A focus of this approach is to minimize the biggest components, the inductors, in the filters of switch-mode power electronics. This approach results in a size reduction of the filters by around 84 %.
A very promising approach to remove the interference of power electronics circuits and telecommunication circuits is to stay away from the frequencies used for information transmission. Even though the electromagnetic spectrum is used without any exceptions, the situation can be optimized for audio applications. This is done by using switching frequencies beyond the communication frequencies and will be described in Radio Frequency Power Electronics (chapter 7).

Each chapter ends with a section printed in italic. These paragraphs are meant to link the respective chapter with the rest of the work and therefore enables the reader to investigate only parts of the work, while getting the perspective to the rest.

Dansk Resumé

Switch-mode effektelektronik forstyrrer andre elektroniske kredsløb ved emission af elektromagnetiske felter og signaler. Derfor blev en række regulatoriske regler (elektromagnetisk kompatibilitet) sat op, som muliggør transmission af informationer. For at opfylde disse regler, er skærmning og filtrering nødvendig, disse begrænser størrelsesreduktion af effektelektronikkredsløb. Motivationen til projektet var, at finde andre muligheder for at forhindre problemer med kobling mellem switch-mode effektelektronik og transmission- eller modtagerkredsløb. Der var specielt fokus på audio effektforstærker.
Efter et historisk overblik og beskrivelse om vekselvirkning mellem effektelektronik og elektromagnetisk kompatibilitet (kapitel 1), beskriver afhandlingen påvirkning af højfrekvente signaler på lydkvalitet af switch-mode audio effektforstærkere (kapitel 2). Andres arbejde vil blive perspektiveret og selvoscillerende systemer vil blive sammenlignet med ekstern synkroniserede topologier.
Efterfølgende vil nuværende udbredte løsninger, som anvendes i industrien, blive forklaret (kapitel 3). Deres udfordringer og fordele vil blive beskrevet. Forbedring af det beskrevede problem var fire løsninger:

- Multi Carrier Modulation (MCM)
- Active Electromagnetic Cancellation (AEC)
- Strømdrevet effekttrin (CDP)
- Radiofrekvens effektelektronik (RF SMPS)

Multi Carrier Modulation (kapitel 4) benytter mere end en ekstern carrier og generer derfor flere pulsebredemodulation (PWM) signaler. Disse signaler bliver kombineret ved logiske kredsløb og skaber en pulstog. I gennemsnit er pulsene proportionale med modulationssignalet, mens de spektrale toppe

kun er halvt så store som i konventionel PWM.
Active Electromagnetic Cancellation (kapitel 5) har været kendt i effektelektronik som aktiv filtrering. Princippet blev anvendt på switch-mode audio effektforstærkere. Det specielle hermed er beskrevet og en prototype viser en forbedring på 15 dB.
Et andet forsøg på at angribe problemet er gjort ved et alternative effekttrin i CDPen (kapitel 6). Målet af forsøget er at mindske de største komponenter, nemlig spolerne, i filtre fra switch-mode effektelektronik. Metoden giver en formindskelse på cirka 84 %.
En meget lovende mulighed for at fjerne interferens mellem effektelektronik og telekommunikationskredsløb er at undgå frekvenser, som benyttes til informationstransmission. Selvom hele det elektromagnetiske spektrum bliver benyttet uden undtagelser, kan situationen forbedres indenfor audio applikationer. Det bliver gjort ved at sætte switch-frekvensen over de benyttede kommunikationsfrekvenser og er beskrevet i radiofrekvens effektelektronik (kapitel 7).

Hvert kapitel slutter med en paragraf i kursiv. Denne paragraf forbinder kapitlet med resten af afhandlingen og skal derfor give mulighed for læseren for at undersøge dele af beskrivelsen, mens man beholder sammenhængen til resten.

Deutsche Zusammenfassung

Schaltnetzteile stören andere elektronische Schaltungen durch Aussendung elektromagnetischer Felder und Signale. Um die Übermittlung von Informationen zu ermöglichen, wurden regulative Bestimmungen (Elektromagnetische Verträglichkeit) geschaffen, welche die Störungen limitieren sollen. Um diese Regeln zu erfüllen, ist es erforderlich, die leistungselektronischen Schaltungen zu schirmen und zu filtern, was deren physikalische Größe bestimmt. Motivation dieses Projekts ist es, Alternativen zu finden, die die Probleme der Beeinträchtigung von Sendern und Empfängern durch Schaltnetzteile verhindern. Spezieller Fokus liegt dabei auf geschalteten Audioverstärkern. Nach einem historischen Überblick und der Beschreibung der Wechselwirkung von Leistungselektronik und elektromagnetischer Verträglichkeit (Kapitel 1), zeigt diese Arbeit den Einfluss hochfrequenter Signale auf die Audioperformance von geschalteten Audioleistungsverstärkern (Kapitel 2). Dazu wird die Arbeit von anderen erläutert und selbstoszillierende Systeme werden mit extern synchronisierten verglichen.
Danach werden die in der Industrie weitverbreiteten Lösungen vorgestellt (Kapitel 3) und deren Herausforderungen und Möglichkeiten aufgezeigt.
Die Verbesserung der Problemstellung sind vier verschiedene Vorgehensweisen:

- Multi Carrier Modulation (MCM)
- Active Electromagnetic Cancelation (AEC)
- Stromgespeiste Leistungsstufen (CDP)
- Radiofrequenzleistungselektronik (RF SMPS)

Multi Carrier Modulation (Kapitel 4) benützt mehr als ein externes Trägersignal und generiert damit mehrere PWM-Signale. Diese werden anhand einer

Logikschaltung zu einer Pulsreihenfolge zusammengeführt, welche durchschnittlich dem Modulationssignal folgt, im Vergleich zu gewöhnlicher Pulsebreitemodulation aber nur halb so hohe spektrale Peaks mit sich bringt.
Active Electromagnetic Cancellation (Kapitel 5) ist unter aktiver Filterung in der Leistungselektronik bekannt. Diese wurde auf Audioleistungsverstärker angewandt. Dessen Besonderheit ist beschrieben und ein Prototyp zeigt auf, dass sich damit das unerwünschte Spektrum um 15 dB vermindern lässt.
Ein anderer Ansatz, um das Problem anzugehen, sind alternative Leistungsstufen in Form von stromgetriebenen Leistungsschaltungen (Kapitel 6). Im Mittelpunkt dieses Ansatzes steht die Bemühung, die größten Komponenten, die Spulen, zu verkleinern. Dieser Ansatz resultiert in einer Größenreduktion der genannten Komponenten um ca. 84 %.
Ein sehr aussichtsreicher Ansatz um die Wechselwirkung von leistungselektronischen und kommunikationstechnischen Schaltungen zu unterbinden ist es, die Schaltfrequenz der Netzteile von den Frequenzen der Informationsübertragung fernzuhalten. Obwohl das elektromagnetische Spektrum ausnahmslos zur drahtlosen Kommunikation verwendet wird, kann die Situation für Audioanwendungen optimiert werden. Dies wird dadurch erreicht, dass man die Schaltfrequenz über die relevanten Kommunikationsfrequenzen setzt (Kapitel7).

Jedes Kapitel endet mit einem Absatz in Kursivschrift. Diese Abschnitte sollen das jeweilige Kapitel mit dem Rest der Arbeit verbinden und es dem Leser ermöglichen, Teile der Arbeit zu betrachten ohne die Perspektive zum Rest zu verlieren.

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Abbreviations, Terms & Definitions

AC - Alternating Current All electrical signals, which are not constant over time. (⇒ DC)

AC Mains - Alternating Current Mains AC mains is a universal term for describing the industrial and urban electrical energy distribution network.

AEC - Active Electromagnetic Cancellation Active electromagnetic cancellation is one of the described improvements in this project (⇒ chapter 5).

Audio Band The audio band is located between 20 Hz and 20 kHz. (⇒ in-band)

AF - Audio Frequency As audio frequencies lie in the range from 20 Hz to 20 kHz.

Aliasing Aliasing is the result of an under sampled signal, i.e. the sampled signal contains spectral components beyond the Nyquist frequency of a system.

AM - Amplitude Modulated (radio) Amplitude modulated radio describes not only the technical modulation topology, but also a specific frequency range from 540 kHz to 1.7 MHz [3] for transmitting radio stations across a long distance.

AV - Audio / Video Audio / video systems denote technical systems having an interface with the human ear and / or eye. It is especially used in the entertainment electronics industry.

CD - Compact Disc Compact Disc is a standardized optical storage media widely used for storage of music in the consumer domain.

CDP - Current Driven Power Stages Current driven power stages operate from current sources, rather than voltage sources (⇒ chapter 6).

DC - Direct Current All electrical signals with frequency 0 Hz are denoted direct current. (⇒ AC)

Dithering Dithering is a forced periodical, pseudo-random or random variation of a reference frequency. (⇒ Jitter)

DNR - Dynamical Range Dynamical range is the ratio between the maximum output level of a system and its noise floor. (⇒ SNR)

DUT - Device under Test Device under test refers to the equipment or system which is applied to a qualifying test.

Electromagnetic Disturbance "Any electromagnetic phenomenon which may degrade the performance of a device, equipment or system, or adversely affect living or inert matter" [4]. The disturbance is understood as the physical cause. Its physical effect is electromganetic interference.

EMC - Electromagnetic Compatibility "The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment." [5]

EMF - Electromagnetic Force EMF is a synonym for voltage.

EMI - Electromagnetic Interference "Degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance." [6] Generally understood as the physical effect of an electromagnetic disturbance.

FM - Frequency Modulated (radio) Frequency modulation is the most popular modulation topology for audio broadcasting. It is applied in the frequency range between 87.5 MHz to 108 MHz [7] in most parts of the world and from 76 MHz to 90 MHz in Japan and from 65.8 MHz to 74 MHz in Eastern Europe [8].

IC - Integrated Circuit An integrated circuit is a system implemented in one or multiple silicon dies, which are mechanically mounted within one enclosure popularly called chip.

In-band Signals having at least part of their energy within the audio band (20 Hz . . . 20 kHz) are considered to be in-band. (⇒ out-of-band)

Jitter Jitter is the variation of a reference frequency. (⇒ Dithering)

JFET - Junction Field Effect Transistor Transistors, which are normally-on devices and require a negative control voltage to get turned off. They are available with and without body diode.

MCM - Multi Carrier Modulation Multi carrier modulation is one of the described improvements in this project (⇒ chapter 4).

MOSFET - Metal Oxide Semiconductor Field Effect Transistor MOSFETs are the most common used electrical switches in power electronics in the range from mW up to several kW.

Out-of-band The energy of signals laying outside of the audio band (20 Hz to 20 kHz) are considered to be out-of-band. (⇒ in-band)

Power Electronics "The field of electronics, which deals with the conversion or switching of electric power with or without control of that power." [9]

PWM - Pulse Width Modulation A coding method, which is storing the information of a signal along the time axis, in spite of the amplitude axis, while keeping the mean value of the signal proportional with the information.

RF - Radio Frequency Radio frequencies are the spectral regions, that can be used for radio communications.

SNR - Signal-to-Noise Ratio As a synonym for ⇒ DNR, the signal-to-noise-ratio describes the relation between a systems output level with respect to its noise floor.

Switching Frequency Switching frequency is the fundamental of a carrier signal in power electronics.

THD+N - Total Harmonic Distortion + Noise A measure to describe the purity of a signal also used as a performance measure for audio devices.

TV - Television Television is a means of entertainment including both, audible and visual information, which are transmitted through a communication channel.

Symbols

C	Capacitance
d	Damping factor
η	Efficiency
f_{sw}	Switching frequency
FOM	Figure of merit
I_{out}	Output current
I_{ps}	Power stage output current
L	Inductance
P_{out}	Output power
R	Resistance
$\underline{s}$	Complex frequency
T	Period
V_{in}	Input voltage
V_{out}	Output voltage
V_{ps}	Power stage output voltage

Chapter 1

Motivation for Research

The project "Improvement of out-of-band behavior in switch mode amplifiers and power supplies by their modulation topology" was created out of a realized pain in development. Particularly it was discovered, that it is an excessive process to fulfill the electromagnetic compatibility (EMC) requirements in switch-mode power electronics. The origin of this fact lies in the high-frequent nature of switching signals in power converters which are very precisely measured in electromagnetic compatibility tests. The modulators in power converters are sources of the switching signals. These discoveries formed the title of the project.
To begin with, the phenomena EMC and switch mode power electronics will be elaborated. Both of their background and reasons for being are given. After that, the link between them will be explored and special cases will be shown.

1.1 Electromagnetic Compatibility (EMC)

A generally accepted definition of electromagnetic compatibility (EMC) is given by [5] as "the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment." More commonly used definitions of terms in conjunction with EMC are given in the section abbreviations, terms and defninitions. This section will give further insight in the relevance of EMC and its link to this project, starting out with a historical digest on EMC, popular known examples of the physical

phenomena as well as categorizing those and connecting them to relevant laws and norms.

1.1.1 History

The consideration of electromagnetic compatibility in society started with a German law "Gesetz über das Telegraphenwesen des Deutschen Reiches" (engl. "Law of telegraphy from the German Empire") in 1892 (see appendix A), restricting all rights to build transmission stations to the state. In December 1920 it happened that this technology was used to transmit the Christmas concert in the south-eastern Berlin area across a distance of about 600 m from a hill to a castle. However nearby driving automobiles interfered with the transmitted signals and the sound quality was degraded. As one of the listeners, the Chancellor of the Republic Herman Müller, was not amused by the quality of the received music, he ordered to correct the issue and the subject of EMC was born this way [10].
Although the United States Congress enacted the "Wireless Ship Act" [11] in 1910 requiring open sea passenger ships to be equipped with radio communication equipment, this law did not prevent multiple usage of the same transition frequency in the same geographical area. This lead to several interest conflicts between the U.S. Navy, private companies, and radio amateurs. Especially the later interpreted radio communication as an unlegislated area which led them to disturb life saving messages to ships. Additionally motivated by the sinking of the RMS Titanic in 1912, the United States put the "Radio Act" [12] into force later in the same year. This regulation empowered the "United States Secretary of Commerce and Labor" to restrict certain frequencies to military and security uses and allowed it to offer licenses for other frequencies to the amateur radio operators. This was the first partitioning of frequencies and separation of different frequency bands in the radio frequency range. In 1927 the usage of frequency bands was increased by broadcasting on top of the previous use for communications only. This change of utilization resulted in a new version of the "Radio Act" empowering the 1926 founded "Federal Radio Commission" (FRC) [13] to supervise the electromagnetic spectrum. The FRC was replaced in 1934 by means of "Communications Act of 1934" [14] with "Federal Communications Commission" (FCC) [15] which requires products to be labeled with the logo in figure 1.1(a).
On an international basis the "Comité International Spécial des Perturbations Radioélectriques" (CISPR) was founded in 1934 from the "International Electrotechnical Commission" (IEC) to set the rules for technical usage of various frequencies. Later on in 1984 the "Comite Europeen de Normalisation Electrotechnique" (CENELEC) was given the task to develop the standards for emission, immunity and safety in Europe [16]. The European

Union requires products sold on the european market to carry the "CE label" [17] as shown in figure 1.1(b). Among others, this labeling confirms electromagnetic compatibility.
It can be easily confused with a label commonly known as "China-Export Label", which has a smaller spacing between the two letters in the label as shown in figure 1.1(c).

Figure 1.1 Labels

(a) "Federal Communications Commission" (FCC) label [18]

(b) "CE" label for compliance of products with european rules

(c) "China-Export" label, indicating that the product is exported from China, can be easily confused with "CE"

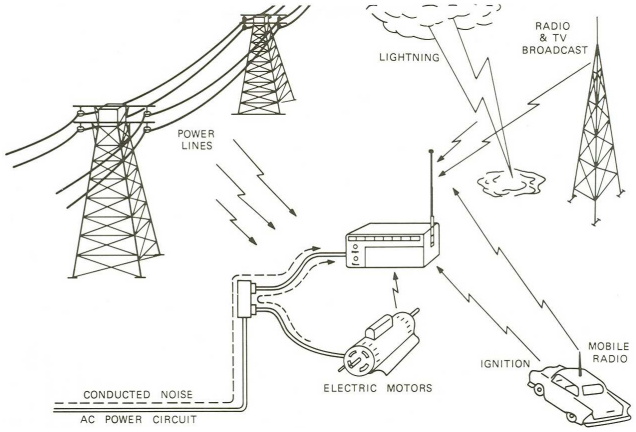
While the FCC is still in power today, its legislation from 1934 was replaced in 1996 by the "Telecommunications Act of 1996" [19]. The major change was initiated by the privatization of the telecommunication sector. Its purpose is to enable competing economical interests to share frequencies.
An overview of the most important valid EMC directives is given in [20].

1.1.2 Physical Phenomena

Similar phenomena as in the past can be found with nowadays operations of electronics. Popular examples are that flight attendants "request that all cellular phones, pagers, radios and remote controlled toys be turned off for the full duration of the flight, as these items might interfere with the navigational and communication equipment on the aircraft." A study [21] describes the technical relation between the personal electronical devices and the navigational and communication equipment of an airplane in the frequency ranges from 108 MHz to 117.95 MHz as well as from 1.2 GHz to 1.6 GHz.
Another popular example these days is the audibility of data transfer from a GSM (Global System for Mobile communications) cell phone in loudspeakers. Even operating in a high and inaudible frequency range (either 850 MHz, 900 MHz, 1.8 GHz or 1.9 GHz), the envelope of the data transfer rate is folded into the audio frequency ranges by time division multiplexing (TDMA). The resulting period of the data packages is equal to the repeti-

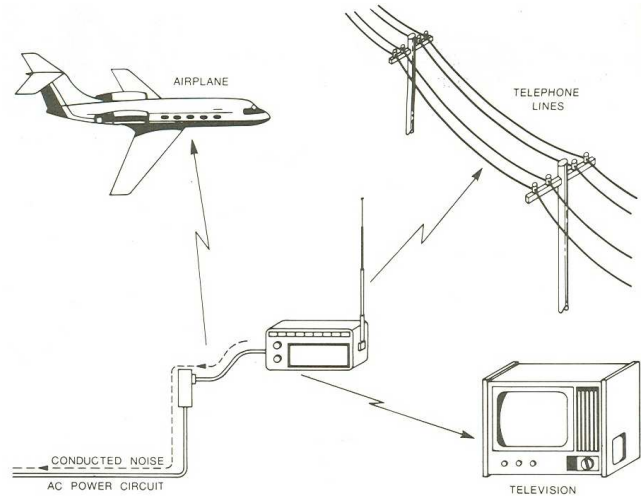
tion rate of the time slots of TDMA which are 4.615 ms apart from each other. The inverse of this period is the fundamental frequency (216.7 Hz) of the audible signal in a nearby loudspeaker.
Cell phone usage is also prohibited in hospitals. These institutions use wireless networks communicating at very low power levels, for example to transmit the heart monitor data of patients to the associated nursing stations.
Very level sensitive applications are navigation systems. According to [22], is the detection level for a receiver in GPS (global positioning system) as low as -160 dB.
Numerious other popular examples are given in [23] and spectacular happenings are countless in the internet. As the above historical essay and all of these modern examples highlight, it is now and then the comfort and even safety of peoples lives which is enhanced by fullfillment of EMC regulations.
The origins of EMC have been given in frequency ranges of interferences but nothing has been said so for about the quantative aspects. In [23] it is called the "EMC gap", that went smaller over the years. There, this gap is defined as the distance between immunity level of possible disturbed equipment from amount of emissions originating in the offending equipment. This is a major classification in EMC. Equipment and systems get commonly tested according to both criteria.
Immunity testing commonly applies a hazardous strength of a specified test signal in a defined manner on the device under test (DUT). The way and procedure how to perform the test is given in various norms and the appropriate test method needs to be decided. A widely applied test is called electrostatic discharge (ESD) applying very short pulses with high power levels but low energies to the surface or interfaces of the DUT. The relevance of these immission tests are illustrated in figure 1.2. This project does not include research in the area of immunity testing, because the existing solutions in the industry (ESD cells on chip level) are neither physically big nor expensive.

Figure 1.2 Demonstration of concrete immission problems from [1].



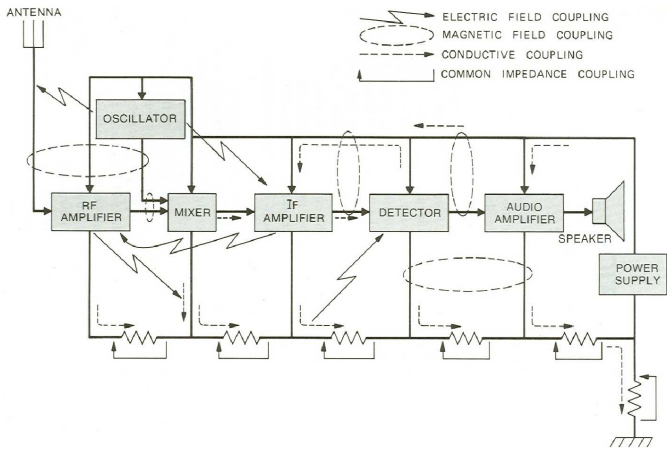
While the immission testings are focusing on the DUTs ability to function satisfactorily in its electromagnetic environment, the problematics of emission in EMC specifies the "intolerable electromagnetic disturbances to anything in that environment" according to [5]. This discipline is measuring disturbance caused by each equipment or system in a well known and isolated environment. Its further significance is visualized in figure 1.3.

Figure 1.3 Examples of descriptive emission mechanisms from [1].



The physical phenomena behind both the immunity and the emission concern are transmission of energy by means of fields. In spite of the duality of the electric and magnetic field either one of them might dominate dependent on its application. Electromagnetic fields carried in conductors are commonly decribed as “galvanic” or “conductive” coupling whereas electromagnitic energy conducted by air is further distinguished by the type of its dominating field. For predominantly electric field EMC problems the term “capacitive coupling” is widely used and magnetic field dominated challenges are named “inductive coupling”. Both origins however can never be completely separated and, dependent on the frequency range, they are of more or less interest for a given geometry and material constellation.
Despite qualitative considerations, EMC is also setting quantitative limits for disturbances. One application and its coupling paths which is mainly challenged by both, immission and emission, is an entertainment system containing both a receiver - which should not be disturbed - and switch-mode power amplifiers and supplies as shown in figure 1.4.

Figure 1.4 Block diagram of an entertainment system and its internal coupling paths from [1]



The technical specifications allow the qualifying tests to measure one signal with reference to a fixed and low ohmic ground connection to the DUT. However for product designers it might be necessary to distinguish between common mode and differential mode EMC. These two observations are undertaken for two coupling paths, respectively conductive input or outputs of devices. For a possible victim of the distributed electromagnetic energy it is irrelevant whether this energy was generated between two conductors or from two conductors to ground, for the disturbing system though, there is

a difference in terms of which elimination method to choose.

1.2 Switch-Mode Power Electronics

The field of switch-mode power electronics is concerned with the conversion of either the voltage, the current or the frequency of electrical energy by means of electrical switches in or close to saturation or cut-off operation modes. The majority of those devices called converters operate based on rectangular control signals allowing the switches to either block voltage and have only little current conducting through them or conduct current while not having an electrical potential across the conducting terminals. Further insight into the principles of power electronics can be gained from numerous literature as [24–29] as the most common representative text books in this field.

1.2.1 History

Instead of giving a complete historical overview of power electronics in general, this section is meant to concentrate on the relevant historical findings which have relevance to electromagnetic compatibility.
Five years after the german Chancellor of the Republic Herman Müller laid the fundation for the first EMC regulation as described in section 1.1.1, a first patent about a "method and apparateus for controlling electric currents" [30] was filed by Julius Edgar Lilienfeld describing a first version of a field effect transistor (MOSFET). This patent was followed three years later by a first application of these devices in an "amplifier for electric currents" [31] also by Lilienfeld.
In the Bell Laboratories - the place where later on the first working prototype of a transistor was built - Bennett derived the spectrum of a half wave rectified sine wave [32]. In 1933 - the same year CISPR was founded - he firstly used a method called Double Fourier Series, which describes a two dimensional Fourier Series for this task. Bennetts aim was to describe the spectrum of those non-sinusoidal waveforms.
Even though diodes existed already since a long time and have been used for rectification purposes it took even longer than the validity period of Lilienfelds patent, to get the first working prototype of a transistor in 1947. This accomplishment got used in many electrical engineering disciplines and set the foundation for new applications. Basic information technology evolved during this time and in 1954 Harold S. Black published an overview of modulation theories [33]. Among those modulation topologies used for information transmission, he described also pulse width modulation (PWM) which was, and still is, less popular for information coding but has a significant

impact in power electronics because the coded information is not removed from the base band, while it still allows efficient operation of switches. In his work, Black applied the mathematical tools from Bennett to PWM and first achieved an analytical description for the spectrum of this modulation form.
During the following decades, power electronics applications grew with the increase of electronics in industrial, consumer, and mobile equipment as power electronics are the interface between electric and electronic systems. Since then, the basic modulation principle hardly varied, and it is still PWM, which is the dominating modulation principle applied to power electronic converters.

1.2.2 Spectral Contents of Signals in Switch-Mode Power Converters

Blacks equations [33] showed the spectral contents of a PWM signal. The amplitude of the harmonics of a PWM signal are declining with increasing frequencies but are theoretically unlimited in their number. The main components of the spectrum is the modulation signal itself, which is the desired information to be coded in the pulse stream, a switching frequency and its harmonics as well as side bands left and right of those. The distance of the side bands to each of the harmonics is linearly dependent on the modulation signal frequency.
There are some conclusions to draw from these results. First the signal in the base band is not getting distorted intrinsically by this modulation type. This is of particular interest in audio applications as the foremost premise for amplification is not to change the signal in the audible range. Further description about the desired qualification of audio amplification is given in [34]. The importance of this is evolving out of the high sensitivity of the human ear with respect to dynamical range, distortion, and frequencies of signals and other parameters. The connection between technology and biology is given by a discipline called psychoacoustics. Blacks equations are helpful in the way to show that there are no major undesired spectral components resulting from PWM.
The switching frequency components are varying with the amplitude of the modulation signal. The higher the modulation signal is, the lower are those. The opposite is true for the side bands. Those start out to be negligible at low modulation signal and grow with emerging modulation index.

1.3 Coherence between EMC and Power Electronics

As described above, it is the ambition of EMC to keep the electromagnetic spectrum free for transmission of signals. It is of no relevance in the human audible frequency ranges and although there are other listeners in nature which have frequency extended hearing capabilities like dogs and bats, the EMC relevant frequencies are limited to technical listeners (receivers) only. The spectral components of PWM signals are inherently conflicting with major broadcasting systems like amplitude modulated radio (AM) and frequency modulated radio (FM) as well as television broadcasting [35]. Practically it had been discovered in modern applications that the spectral contents of a PWM signal are relevant up to several 100 MHz before they decline into the noise floor of the input of the receivers for those topologies.
To underline this, table 1.1 shows the performance figures of some commercially available receiver ICs. As the main focus of this project is audio applications, it includes only radio receivers. Those came on the market within the last 25 years.

Table 1.1 EMF sensitivity level of commercially available radio receivers

manufacturer	part number	AM sensitivity / µV	FM sensitivity / µV
Rohm	BH1406		5.0
Silicon Labs	Si4700		3.5
Silicon Labs	Si473x	25	2.2
ST-NXP	TDA7010		1.5
ST-NXP	TEA5711		2.0
ST-NXP	TEA5757	55	1.2
ST-NXP	TEA5766		3.0
ST-NXP	TEF6903	50	2.0

As the presented sensitivity levels, i.e. the smallest signal the receiver can detect — or can be disturbed with, stayed in the same range over a quarter of a century, it is believed that a technical limitation has been reached there and it is acceptable to assume, that there is no need to prevent the receiver from disturbances, which are below that level.
This is defining the target, which should not be disturbed. The source of disturbance is the high-level PWM signal itself. So it is the remaining energy from the PWM signal at the receivers input, which is disturbing the radio

reception, respectively generating EMC. The quantitative measures for the disturbance are:

- the scale of the disturbing source itself, i.e. the amplitude of the PWM signal,
- the worst case path from the physical location of the PWM signal to the receiver input, i.e. the transfer function of the coupling path.

To get a measure for the amplitude, the PWM signal can be decomposed by a Fourier Series. For the first approximation it is, as described in section 1.2.2, enough to model the PWM signal by a square wave. Switch-mode audio power amplifiers tend to have there switching frequency in the range of 200 kHz to 800 kHz. Out of the four areas, where those kind of amplifiers have industrial impact (professional audio, consumer, mobile and automotive), the later three are of high relevance for EMC because they tend to be installed physically close to broadcasting receivers. Their typical specifications are given in table 1.2.

Table 1.2 Typical output rating for switch-mode power amplifiers in different industries

	consumer	mobile	automotive
Power / W	100 . . . 250	0.5	25 . . . 100
Load / Ω	4 . . . 8	16 . . . 32	2 . . . 4
Voltage / V	57 . . . 126	8 . . . 11	20 . . . 57

The ratings are the peak-to-peak voltage before any EMC precautions, to achieve the stated power unclipped. Internally the power stages might operate with different voltages.
Applying now the Fourier Series of a square wave to the heights of the PWM signal, before any precaution against EMC is taken - gives a worst case signal of 80 V, 7 V and 36 V for the different industries in the AM band of the receivers. The mobile industry is not using AM reception, so it will not be considered further here. In consumer industry the fundamental of the PWM signal is about 123 dB . . . 130 dB higher than the sensitivity of the receiver ICs from table 1.1. For the automotive industry the according distance is 116 dB . . . 123 dB. The passive filters, which are usually applied at the output of switch-mode power amplifiers account for some of this difference, however not for a lot, as the corner frequencies are limited by the application: the audio signal (baseband) ranges up to 20 kHz and shall not be suppressed. The rest of the required damping has to be achieved by

shielding and physical distance.
Taking the FM-band, starting in some parts of the world at 65 MHz, into account all three industry branches are of interest. The harmonic with the highest amplitude, to be considered from the above noted switching frequency range, is around the 81st. Qualitatively this gives 1 V, 88 mV and 450 mV for the three industry types before a possible filter within the amplifier. At the output nodes of the amplifier the signal should be somewhat lower, however it is not a fair assumption, that a second order low pass, as commonly applied, is still optimally working in this frequency range. It is on the contrary very common, that the self-resonance of those filters is less than a decade beyond the corner frequency of the filter. Taking this uncertainty into account, the desired damping from the switch-mode power amplifiers output stage to the FM receivers input stage can be estimated the same way as has been done for the AM case. So the desired damping in the consumer industry is 106 dB . . . 118 dB, in the portable industry 85 dB . . . 97 dB and for the car industry 99 dB . . . 111 dB.
So most of these required insertion losses in the transfer function between the disturbance source — the power stage of the switch-mode amplifier or its power supply — and the victim sink — the input stage of the receiver — are very roughly around 100 dB. The aim of this research work is, to improve this situation, while trying to avoid bulky filter components.

This chapter explained the two background fields, namely audio power electronics and electromagnetic compatibility. Historically EMC norms were created to enable audio applications, especially broadcasting applications. On the other hand state-of-the-art audio applications, i.e. switch-mode (audio) power electronics create EMC problems. By these means the two disciplines interact with each other. Improving this situation without adding bulky filter components and degrading the audio performance is the aim of this work. The next chapter will therefore start with a focus on the influence of the signals dealt with in electromagnetic compatibility on the audio performance.

Chapter 2

The out-of-band Influence on the in-band Performance

From an electrical engineers perspective, performance is a question about characteristics of signals. It is a generally accepted principal, e.g. in introductory textbooks [36], to distinguish between sinusoidal and non-sinusoidal signals. Parameters to describe sinusoidal signals are

- offset,
- amplitude,
- frequency and
- phase.

The offset is also called mean value. T,he amplitude might alternatively be expressed in effective value (root mean square — RMS) or rectified mean value. For non-sinusoidal signals, the later ones are not correlated to the amplitude and therefore require further information about the according signal. This leads to the describing parameters

- crest factor (amplitude divided by mean value) and
- form factor (effective value divided by mean value).

Going one step further in the electrical engineering discipline, signals are considered to be inputs and outputs of systems. Considering those in dependence on each other, linear systems can be differentiated from nonlinear

systems. Then further parameters for signals can be taken into account, such as

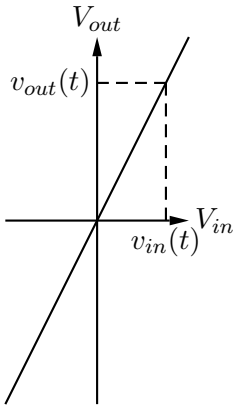
- noise (the minimum measurable signal) and
- distortion (addition of spectral components with respect to a reference signal).

These are of special relevance for systems in information technology and in systems providing some kind of interface with human beings, such as audio / video (AV) systems. The human ear, as the biological interface to the audio systems has very special behaviour as described in [37–40]. The engineering discipline dealing with audio systems has therefore developed further qualifiers for audio signals, like

- intermodulation [34] and
- perceived sound quality [41],

which are among others further described in [34, 41]. Some of them are only applicable for whole audio systems where others can be applied to parts of those. Excluding the acoustic performance, but keeping it as the definite goal in mind, distortion and noise can be taken as the ultimate first order qualifiers for switch-mode audio power amplifiers.
Distortion is generally quantified as THD+N. While the top level electrical engineering terminology is using crest factor as its equivalence, the distortion of systems is always considered to be their linearity. Linearity is given as the derivation of the input to output characteristics (gain) of a system. An exemplary gain-curve of a linear system is shown in figure 2.1.

Figure 2.1 Input to output characteristics of a system



Linearity can always only be measured within the limitations of dynamical range DNR (also SNR), which is a synonym for noise in a system with known maximum output level. Taking figure 2.1 as an example, the shown gain there is 2, which is for illustrative reasons about a factor 10 less than a typical audio power amplifier would be designed for. Assuming further, that the marked input level (about 10 mm right of the origin) can be taken as a reference to describe audio amplifiers input levels, the thickness of the gain line can be taken for a measure of noise level. To represent a decent audio power amplifier (with about 120 dB SNR) in this figure, the line — which is around 300 µm (corresponding to an SNR of about 70 dB) thick — would need to be around 1 µm in thickness (for the accumulated noise in the audio band). For comparison, this is about 10 to 100 times thinner than a human hair. This relation is meant to give an impression about the required precision for decent sound reproduction and shall serve as a quantitative reminder for the following described influences from the out-of-band behaviour of switch-mode audio systems on their in-band performance. First after the noise of the amplifier, respectively the thickness of the referenced line, is reduced to this acceptable level, the derivative of the same line, can be taken to represent the distortion, respectively the linearity of the system. The next section will describe the out-of-band influence on noise, where the second section of this chapter will deal with the impact of out-of-band signals on the linearity.

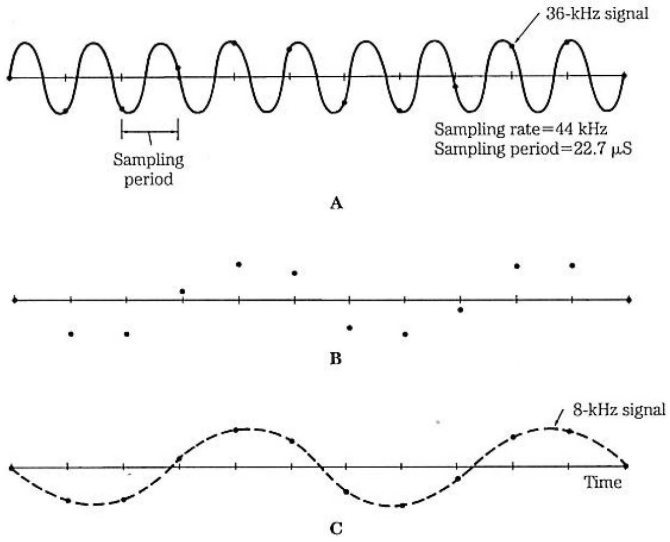
2.1 Out-of-Band Energy and its Impact on Audible Noise

Systems involving other input frequencies than in-band signals are wide spread within the audio engineering discipline. Two of the main knowledge contributing engineering parts of audio systems are signal processing and conversion systems between discrete-time and continuous-time signals. Within those parties, the terms aliasing, dithering and jitter evolved. The principle behind those three definitions are applicable and relevant for the noise performance of switch-mode audio power amplifiers. While aliasing is describing periodical out-of-band disturbances and their way into the audio band, dithering and jitter is applicable to random and quasi-random signals as well. Especially random signals are often also refereed to as noise. The main difference between the disturbance sources is that aliasing components can be distinguished by their frequency, while it is impossible or quasi-impossible to find the frequency of dithered systems.

2.1.1 Aliasing

Aliasing components arise, if a signal is under sampled [2] as shown exemplary in figure 2.2.

Figure 2.2 Undersampling leads to aliasing components in the audio band from [2]. The upper waveform shows the out-of-band disturbance and its sampling points, the middle waveform the resulting sampled data and the lower waveform the interpolated aliasing result.



The out-of-band disturbance frequency is randomly chosen there. It could as well be higher as the sampling frequency, while it is always the difference between the sampling frequency (and its harmonics) and the disturbance (and its harmonics), which is aliased into the audio band. For switch-mode audio power amplifiers the sampling frequency is equivalent with the switching frequency.

2.1.2 Dithering

While aliasing disturbances can be described with the parameters for sinusoidal and non-sinusoidal waveforms, as given earlier in this chapter, dithering disturbances are rather characterized with the probabilities of noise [42]. There has been done a major research contribution in the last decades from knowledge generation about quantizers [43–46]. One major contribution for both, audio and video application was to remove "'sticky bits"', i.e. sig-

nals falling below the minimum quantization level and therefore forcing the output of the quantizer to stick either to the positive or the negative least significant bit. This knowledge has been applied to PWM systems, as used in switch-mode audio power amplifiers, by [47]. There it has been demonstrated for a recorded music signal at standard consumer quality compact disc (CD), that the jitter on the clock may not exceed 100 ps to prevent audible artifacts. To give a perspective to the typical switching frequencies as given in section 1.3, this is equivalent to about a 10.000th to 50.000th part of the period of a practical PWM signal.
So the demand on the purity of the clock is high. To illustrate this further, figure 2.3 shows the 1 kHz wide skirts of the fundamental of a clock, used for carrier generation in a switch-mode audio power amplifier and its mirror image in the audio band — also 1 kHz wide — in figure 2.4. Note that the dynamical range of the spectrum analyzer for the out-of-band measurement was not enough to represent the whole dynamical range of the carrier. Therefore the amplitudes do not match. The in-band measurement is referenced to 1 V.
This means, that the clock frequency needs to be very stable. Frequency variations, as occurring in RC-oscillators are not acceptable and crystal oscillators or similar technologies need to be used instead.

Figure 2.3 The out-of-band performance of a clock for a switch-mode audio power amplifier ...

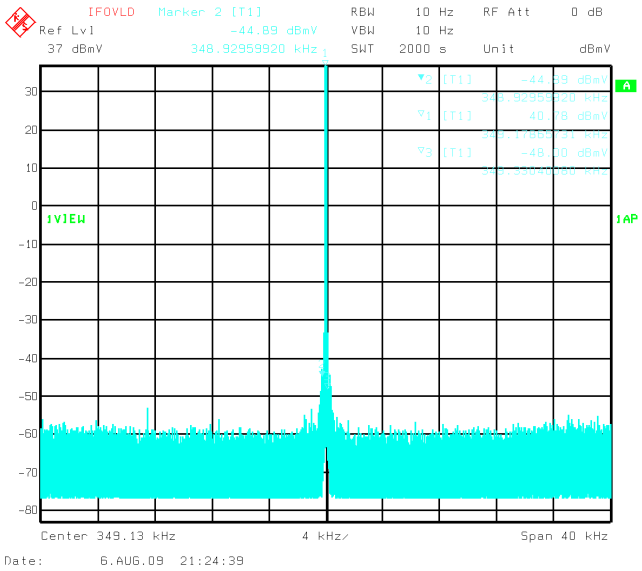
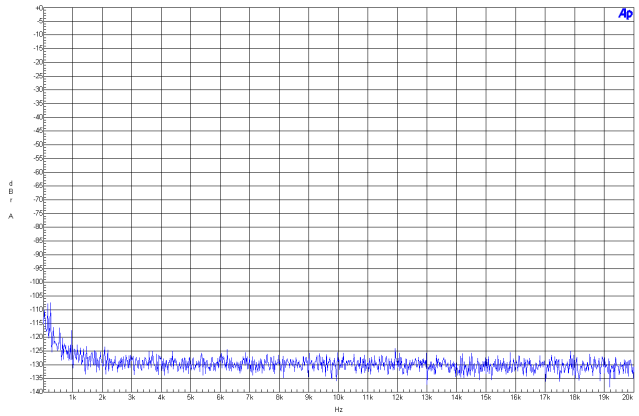


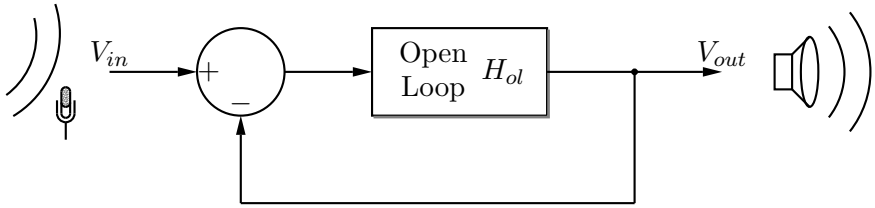
Figure 2.4 ... and its impact on the in-band performance.



2.1.3 Error Correction

Dependent on the correlation or uncorrelation of the out-of-band signals, which are folded down into the audio band, feedback (as shown in figure 2.5) around the amplifier and appropriate gain in an error amplifier can or cannot remove the audible distortion.

Figure 2.5 Control loop of an audio power amplifier



Correlated in this sense means, that the introduced disturbance at the next decision point (edge of the PWM signal) is dependent on the last one. This implies that the distortion has to have a frequency and that this frequency is lower than the switching frequency. Additionally the amplifier needs to have enough loop gain, i.e. $H_{ol} > 1$ at the frequency of the distortion signal. It cannot be generalized that a frequency is only definable for periodic signals, like the 36 kHz sine wave in figure 2.2, but also for parts of noise. Also noise can be described with an uncorrelated part and a correlated part, where the correlated part might have a different origin than the uncorrelated part. Human made noise for example mainly originates from periodic

signals and is therefore mostly correlated, whereas cosmic noise is not. More differentiation of noise behaviour can be found in [42].

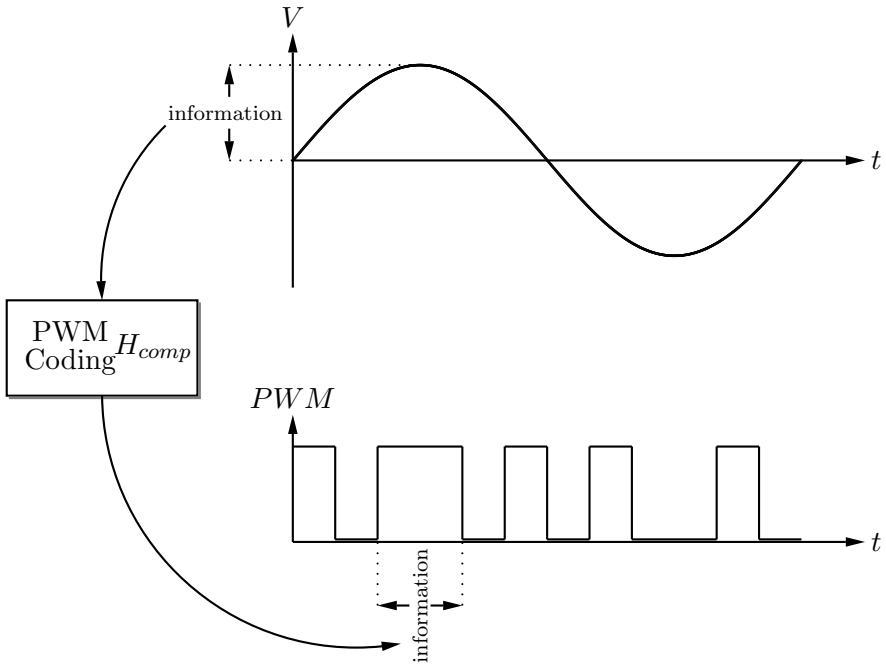
2.2 Carriers Impact on Linearity

Once the noise level of an amplifier is down to an acceptable level — 130 dB as shown in figure 2.4 are considered acceptable — the linearity (distortion) can be optimized.

2.2.1 Coding Audio to PWM

Referring back to the comparison of the thickness of the gain curve with the human hair in figure 2.1, the input signal can be drawn along a time axis as shown on top of figure 2.6. In this upper waveform (a sinusoidal shape is chosen for illustrative purposes, but not limiting generality), the thickness of the curve would need to be 10 to 100 times thinner as a human hair (20 to 200 times thinner, than it appears on a printout of this page) to represent the precision of the audio signal.

Figure 2.6 Coding the audio information (amplitude) of a signal into the pulse width of a PWM signal.

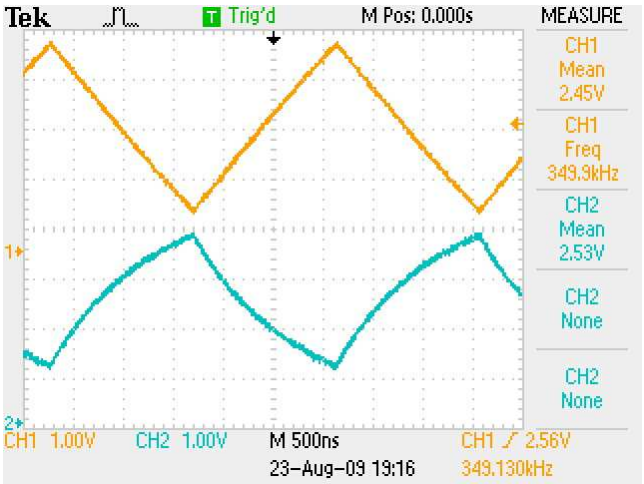


When feeding a comparator with a carrier signal and the audio reference, it toggles its output according to those two signals and codes the audio information into the pulse width of the resulting PWM signal. Again the precision of the timing of the edges needs to be within 100 ps as named above, equivalent to the comparison of the line thickness and the human hair again.

2.2.2 Forming the Open Loop to an Integrator

The PWM coding itself is a highly non-linear function. There have been major contributions to the available knowledge in science over the last two decades from [48–50] and a major contribution to the specialty of audio applications and its precision from [51–53]. The coding can only be done with the precision of its input signals. If a triangular waveform is used to map the amplitude information of a reference signal into the pulse width of a PWM signal, then its slope represents the slope of the gain curve of H_{comp}. To keep the required precision for an audio signal, there is therefore a high demand on its linearity. Figure 2.7 shows a linear and a highly nonlinear carrier.

Figure 2.7 A linear carrier and a highly nonlinear carrier to act as transfer function for the PWM coding H_{comp} in a switch-mode audio power amplifier.



The first shown carrier is generated by a highly optimized active integrator, turning a square wave into a triangle, while the second one is converting the exact same square wave into partially exponential functions by a first order RC-low-pass. The resulting difference in distortion is shown in figures

2.8 and 2.9 respectively. Note the difference between the point, where the distortion exceeds the noise floor (around 2 W) and clipping.

Figure 2.8 Resulting distortion curve for the linear carrier in figure 2.7

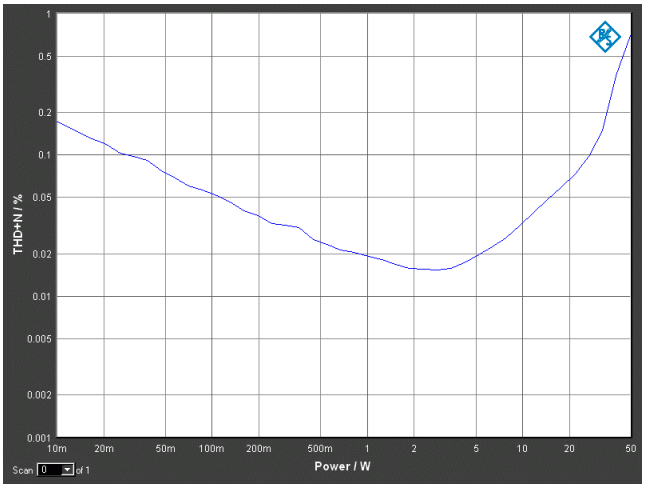
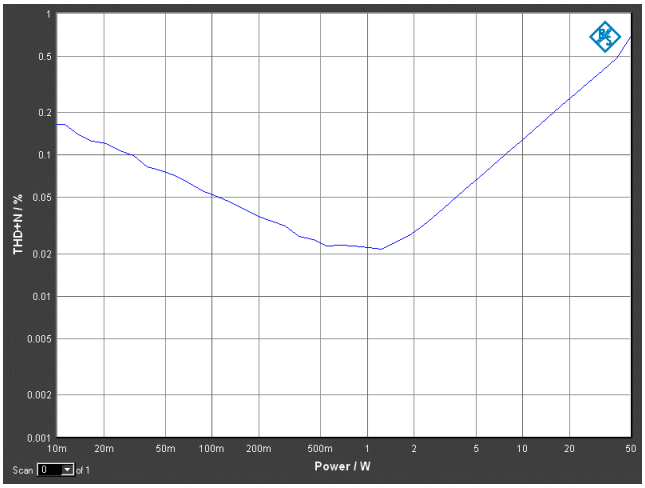


Figure 2.9 Resulting distortion curve for the nonlinear carrier in figure 2.7



Both of those carrier signals are stand-alone generated signals originated from a crystal oscillator, having the quality shown in figure 2.3. Stand-alone means, there is no other influence on the carrier. The effective carrier does not only include the pure stand-alone carrier, but also whatever high-frequency energy is fed back from the output of the amplifier into the

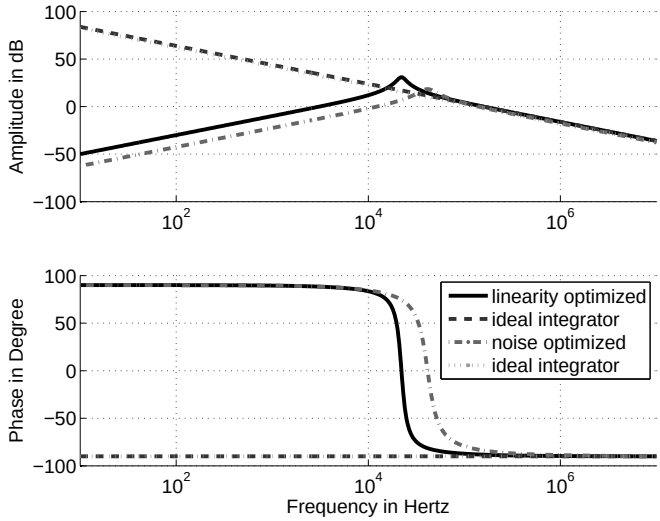
input of the coding (comparator). The out-of-band energy, originated from this phenomenon, is called ripple in power electronics terminology. Self-oscillating switch-mode power amplifiers use this as the only carrier signal, where externally clocked switch-mode audio power amplifiers combine the ripple with an externally applied carrier, as the stand-alone ones shown in figure 2.7. Independent on the origin of the effective carrier, it is representing the linearity of the whole amplifier, so also for externally clocked systems the resulting ripple at the input of the coding has to be engineered for audio quality [54]. Exactly this has been described in two different approaches by [55] and [56, 57]. While the first approach is minimizing the amplitude of the fed back ripple, the second approach is linearizing it. As the second approach is taking feedback directly from the rectangular PWM signal, the most linear transfer function for it is a pure integrator, where pure means, its single pole is at $f = 0$ Hz. That fits well with a first order integrating controller, like a PI-regulator. The principle can however be expanded to second order integrating controllers as shown in [58]. Another approach is to take the feedback after the filter, not feeding anything else than this feedback and the audio signal into the coding and utilizing the high bandwidth of this principle. This method has been described in [59, 60].
Summarizing those numerous intensive efforts to linearize switch-mode audio power amplifiers results in the desire to have an integrator as the open loop transfer function at the switching frequency and its harmonics. The high performance desire from audio applications on its electronics, as described above, requires the integrator to be as perfect as possible. That means the amplitude has to fall precisely with 20 dB per decade and the phase has to be -90 °. Any difference will cause the gain curve (figure 2.1) to be non-linear and it is the responsibility of each switch-mode audio power amplifier design engineer to judge, if the required performance can be fulfilled or not.

2.2.3 Carrier Generation for Externally Clocked Systems

While self-oscillating systems can combine this requirement with the integration slope of a controller to form an integrator for all frequencies, external clocked systems need to optimize two transfer functions.
First, the open-loop transfer function is facing the same specification as in self-oscillating systems at the switching frequency and its harmonics, but is limited by a phenomenon called ripple stability [61] in its control bandwidth. This means the fed back ripple may not have a higher slope, than the external fed carrier signal, otherwise the reference will instead of converging to a decision point, diverge and saturate the control loop.
Second the external carrier fed signal needs to be linear [62, 63]. Opposed to the open-loop transfer function it is not desired to have gain in the audio

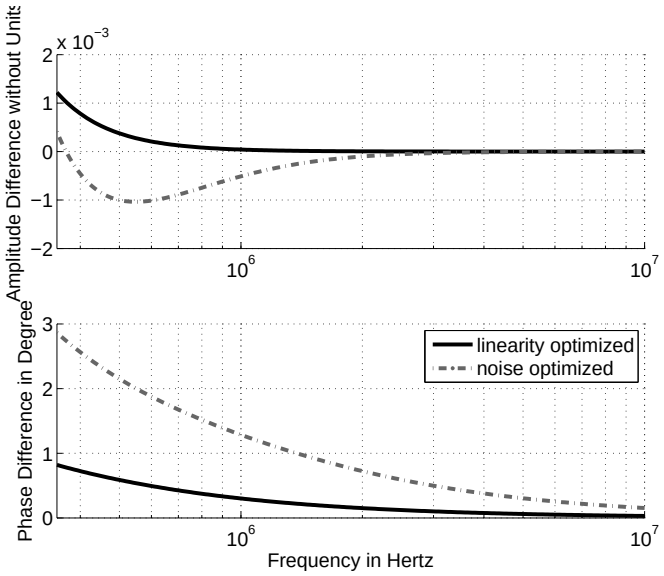
band in this transfer function as otherwise the low-frequent noise from the oscillator would be amplified. This is forcing the carrier generator to be a band-pass. Two different third order band-pass transfer functions for this purpose are shown in figure 2.10.

Figure 2.10 Band-pass transfer function to generate a triangular carrier waveform from a rectangular clock for usage in externally clocked switch-mode audio power amplifiers. Also shown are the corresponding perfect integrators, which can be used in self-oscillating systems as open-loop transfer functions.



It shows two different approaches: one optimized for linearity purposes, i.e. it minimizes the distance between the perfect integrator and the band-pass at the switching frequency and its harmonics and the other one optimized to suppress the audio band noise fed into the system through the clock. The commonly used bode plots, as the one used in figure 2.10, do not reveal precise enough data to judge about the usability for audio system purposes. Instead the comparison between the real transfer function and the optimum — which are the perfect integrators — are shown in figure 2.11.

Figure 2.11 The difference between perfect integrators and the optimized band-pass transfer functions on a linear y-axis at the switching frequency and beyond.



The noise optimized carrier generator leads to the decent linearity as has been shown in figure 2.8.

Chapter two connected the shape of a carrier signal in switch-mode audio power amplifiers with the amplifier's resulting audio performance. It was shown, that the carrier signal, even though it is laying beyond the audio band, has an influence on the audio measures. The next chapter will examine the influence of the carrier frequencies properties on communication channels of broadcasting systems.

Chapter 3

Previous Solutions

The main problem, as described in section 1.3 is rather dealing with the out-of-band parameters of audio systems only, while chapter 2 was a brief excursion, pointing out the requirement on precision and the various influences of out-of-band signals on the in-band performance. While the latter one was mainly described by rather new research results, is the problem of receiver disturbance and various solutions for it not new at all. In fact one of the most well known companies in the industry was founded based on their cutting edge solution to the radio receiver disturbance phenomenon from other alternating signals. Bang & Olufsen "was founded in 1925 by Peter Bang and Svend Olufsen, whose first significant product was a radio that worked with alternating current, when most radios were run from batteries" [64]. The reason for operating radio receivers at that time from batteries was the AC mains direct influence on the in-band performance of audio systems. The two named gentleman solved this problem by filtering. While the most significant origin of the problem is nowadays no longer located in-band, but out-of-band, filtering is still the first approach to deal with it. For field coupled disturbances, shielding has been a standard solution since many decades. Despite those generally known principles, widely described in textbooks like [23], a group of other published and industrially implemented solutions will be described in this chapter. Each section ends with a table summarizing the advantages and disadvantages of the method as well as an arrow diagram showing the trade-offs, which need to be considered by the design engineer, when implementing the respective technology.

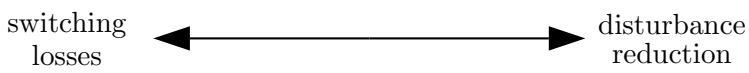
3.1 Limited Speed of Edges

A wide spread approach is to decrease the slope of the PWM signal in switch-mode electronics. This is simply done by decreasing the drive of the power stage, by increasing the resistor between the drive stage and the power stage. The result is that the frequency, where the PWM signal needs to be modeled as trapezoid instead of a rectangular waveform, is dropping. The impact of this is analytically well described and experimentally verified in [65]. Noticeable is the fact that a trapezoid has spectral zeros, whereas the envelope of a rectangular waveform is falling continuously. Even though the trapezoid does not exceed the spectrum of the rectangular at any frequency, the drive speed of the power stage, which is adjusting the spectral zeros, can still be used to foreseeable minimize the spectrum at those frequencies, where the application has the toughest demands. While this principle is a well known method in power electronics, it certainly also holds for switch-mode audio power amplifiers [66].

Table 3.1 Characteristics of limitation of switching edges

advantages	disadvantages
• simple to implement • cheap • generally applicable in power electronics	• causing losses • works only for high frequencies, e.g. FM band • often implemented by nondeterministic approach • sensitive to tolerances

Figure 3.1 Trade-offs when limiting the edges of a power stage.



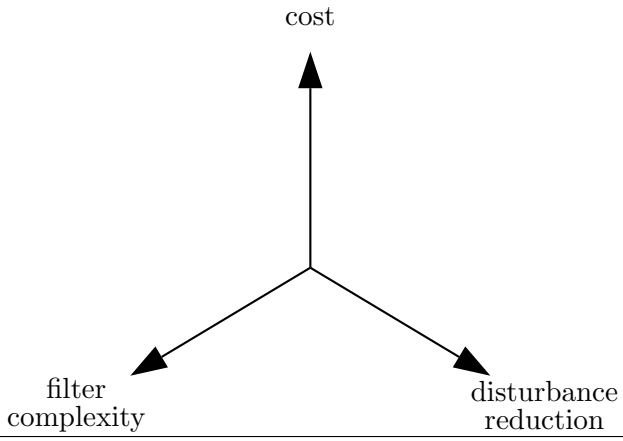
3.2 Parasitic Cancellation

Even though it is best practice to locate the source of EMC and eliminate it there, like the approach described in the last section, it might not be the best trade-off between increasing the losses in the circuit and the elimination of EMC. When having no further degree of freedom in edge limitation, the undesirable out-of-band energy can either be shielded or filtered.
Shielding is the first approach to return undesired fields to its origin and damping the coupling path to the victim. Common practice for this solution is described in [26].
Filtering is applied within devices to keep the out-of-band-energy off the cables connecting the device with the surroundings. This prevents both, direct coupling into the electronic device on the other end of the cable as well as radiation through fields from the cables — from a communications engineers perspective, the cables act as antennas. Building filters with perfect components (inductors and capacitors), allows damping up to the level limited by the order and coefficients of the filter only. But perfect components are not available. In practice it is hard to measure 40 dB of damping per decade for a typical second order low-pass filter with a gain-phase analyzer, because the first self-resonances of the filter components are not sufficient high enough in frequency. The impact of the parasitics of the filter components is for example described in [67–69]. This leads to the need of a combination of various different filter elements. An intensive study [70] has been done lately on the optimal combination of various filter components, so that their parasitics can be utilized. The described methods are based on the undesired fields, radiated by the filter components and combine those in a way, that several of them cancel out. These approaches are called parasitic cancellation.

Table 3.2 Characteristics of parasitic cancelation

advantages	disadvantages
• utilizes parasitic components • generally applicable in power electronics • does not necessarily introduce insertion loss	• works only for high frequencies, e.g. FM band • very sensitive to tolerances

Figure 3.2 Considerations, when implementing parasitic cancelation.



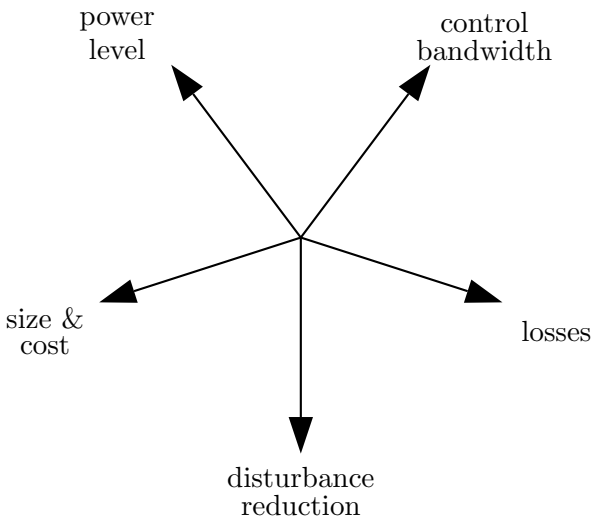
3.3 Interleaved Operation

Another way to decrease the out-of-band energy, which is leaving the chassis of the switch-mode audio power amplifier through the output connectors is to cancel some of the harmonics and their sidebands. This can be done by operating two or more output stages with opposite or phase shifted carrier signals [62] and applying the resulting outputs differentially across the load [71]. This way a number of harmonics of the switching frequency and the respective sidebands are suppressed differentially across the load [72]. Therefore the out-of-band energy across the load is lowered.
The suppressed frequencies are not gone, but transfered into common mode energy at the outputs of the power stages. They have equal polarity and therefore return through a common reference path of the power stages (in most cases ground). So the energy is returning on parasitic paths to their source, turning the impedances on its way into radiating antennas.

Table 3.3 Characteristics of interleaved operation

advantages	disadvantages
• effectively reduces the out-of-band energy across the load • works frequency independent • doubles control bandwidth • allows high power levels	• doubles the minimum amount of components in power stage • introduces common mode disturbances

Figure 3.3 Trade-offs for interleaved operation.



3.4 Frequency Hopping

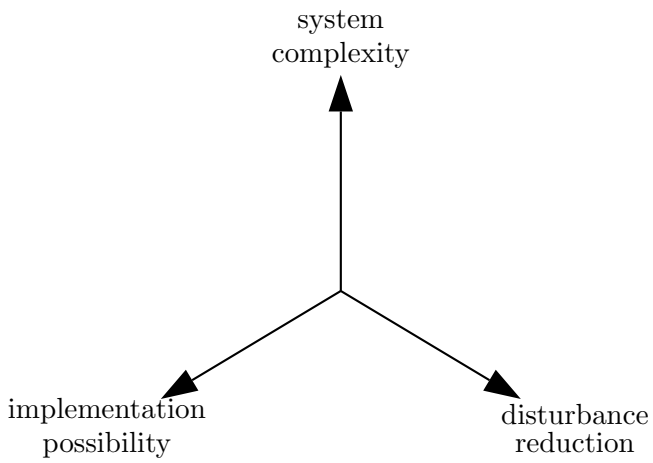
Some applications include both, switch-mode power electronics and communication receivers. In those the physical way from the source of the problem to the victim is short and coupling impedances are low. Therefore these are one of the most challenging applications with respect to EMC. Fortunately those applications come with a specific advantage: the frequency range, which the receiver is tuned to, is known at any time within the system. This information can be used to adjust the switching frequency in a manner, that neither its fundamental nor its harmonics overlap with the receivers tuned frequency. The fundamentals for allowing the change of the carrier frequency during operation of a modulator were set by [73]. At this time the carrier frequency hopping was used to hide the transmitted information away from others, which did not have the knowledge about the carrier frequency sequence. In [74] the principle of adjusting the switching frequency was applied to sound systems. Another way to dynamically detect a preferred carrier frequency for the involved power electronics circuits is shown in [75]. This system is constantly monitoring the intermodulation products of the actual carrier frequency and the receivers tuned frequency and moving the carrier frequency in a manner to minimize them.
Despite the required interaction between the receiver and the power electronics, this principle comes with another limitation for products in the higher quality segment and several mobile applications. Those often include antenna diversity and contain multiple tuners, i.e. two equivalent inputs to the receivers. While one of the tuners provides the signal to the following

decoder, the other tuner is continuously scanning the whole input band to search for both, stations transmitting the same information but delivering a higher level and stations transmitting other information. The latter one is used to give the user the option to look ahead what program material is available on other channels without interrupting the ongoing replay of the actual tuned station.
Another disadvantage occurs, when the spacing between the relevant sidebands of two adjacent harmonics of the switching frequency is lower than the required high-frequency bandwidth of the communication system. For AM radio the bandwidth is twice the base band (either 4.5 kHz or 10 kHz), so 9 kHz or 20 kHz according to [7]. For FM radio the base band is broader, because the program material is transmitted in stereo. Therefore each channel is requiring a minimum high frequency bandwidth of 75 kHz. This lead to a channel separation of 200 kHz in the United States of America [3] and 300 kHz in Europe [7], which is setting the limits for modulation depth of the FM signal. Using the described frequency hopping methods must therefore ensure, that the sidebands of the carrier and the harmonics are sufficiently suppressed within the actual tuned station. While this can be done for the relatively low frequent AM band, it is difficult to satisfy this condition in the FM band. Besides the higher bandwidth of the transmitting channel, the growing sidebands of the switching frequency harmonics [66] is a limiting factor. The picture is getting even clearer when taking also TV applications into account. The high frequency bandwidth of those applications is 7 MHz [7], which makes it practically impossible to achieve an undistorted signal reception by means of frequency hopping.

Table 3.4 Characteristics of frequency hopping.

advantages	disadvantages
• reliably avoids disturbance of a specific receiver • invariant to tolerances	• requires information exchange between receiver and power electronics • works only for specific communication technologies • limited to specific applications

Figure 3.4 Balance between properties of frequency hopping.



3.5 Dithering

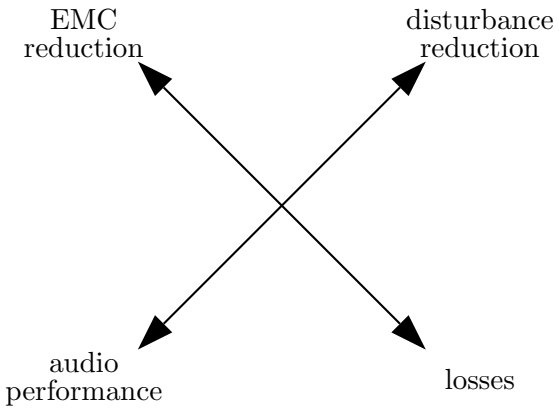
Instead of hopping between discrete switching frequencies, a continuous movement of the carrier was introduced and described in [76–84] and got industrialized by [85–87]. This technique is generally known by the names: spread spectrum, dithering and FM-PWM and, brought into connection with modulation, based on chaos theory and randomization. While the negative impact of dithering on the audio performance was described already in section 2.1.2, this section will deal with the influence on the reception of a broadcasting signal at the input of a communication receiver.
To link dithering with EMC, the function of EMC instruments, namely EMC measurement receivers must be understood. While EMC measurement receivers are specified to be used in normative measurements, spectrum analyzers work in a similar way. The major difference of those two types of instruments is their high frequency input. It is quite undesired to build an excessive amount of circuitry for high frequency operation, as components for this usage are expensive. In conjunction with measurement instruments, which are operating in a broad frequency range, the components need to be usable over a wide frequency range. While the EMC measurement receivers have an adjustable bandpass at the input to suppress everything but the energy in the actual measuring band, a spectrum analyzer immediately mixes the input signal into a lower frequency band. So the spectrum analyzer only has one high frequency circuit – the mixer – while the EMC measurement receiver has an adjustable bandpass and a following mixer. The disadvantage of the spectrum analyzer is, that it would also mix intermodulation and image components resulting from its own local oscillator into the interme-

diate frequency range, where it can not be separated from the original high frequency signal, which should be the only information in this stage of the analyzer. The EMC measurement receiver is suppressing everything, but the desired measurement band, before feeding the first mixer. This filter needs to be configurable in bandwidth to account for differences in EMC norms and the center frequency of the window must be adjustable to measure in the desired band. To account for the transient effect of the filter, the mixer input is closed, while the window is moved and is settling. Therefore an EMC measurement receiver can only be stepped discretely through a certain band, while a spectrum analyzer can be swept continuously. Practically the band-passes are realized by more than one circuit and according to the desired measurement frequency, one of them is activated by relays. Independent on the choice of instrument, which is used for measuring the high frequency energy, the instrument only stays for a limited amount of time at one frequency point. During this time the measurement value for the center frequency of this point is derived by integrating the energy within the measurement window and afterward, the instrument is moving on to process the next measurement point.
Dithering is usually applied in a matter, that the total frequency variation is exceeding the normative window, which is mainly 9 kHz or 120 kHz [88]. This is narrower than the communication receivers bandwidth described in section 3.4. Therefore the EMC measurement is detecting less energy than the communication receiver is getting disturbed with. Additionally the measurement instrument is moving on with time, while the communication receivers stay tuned until they either are forced by the user or by antenna diversity to change the sensitivity band. Both the EMC measurement receivers input filter bandwidth and its measurement time for one data point set the criteria for a dithering signal: The dither must spread outside of the input filter and ideally not be periodic (especially relevant for quasi-random signals), before the measurement receiver has left this actual measurement point. However the bandwidth of the communication receiver would be higher than a typical dither spread and it stays tuned for ways longer than the maximum repetition time of typically used repetition times. Therefore dithering has not only a negative effect on the audio performance of switch-mode audio power amplifiers as described in section 2.1.2, but also prevents optimal signal reception of communication receivers, even though it is improving normative measurement results.

Table 3.5 Characteristics of dithering.

advantages	disadvantages
• lowers EMC • excessively described in literature	• keeps receiver disturbance • impact on audio performance • increases losses

Figure 3.5 Trade-offs for dithering.



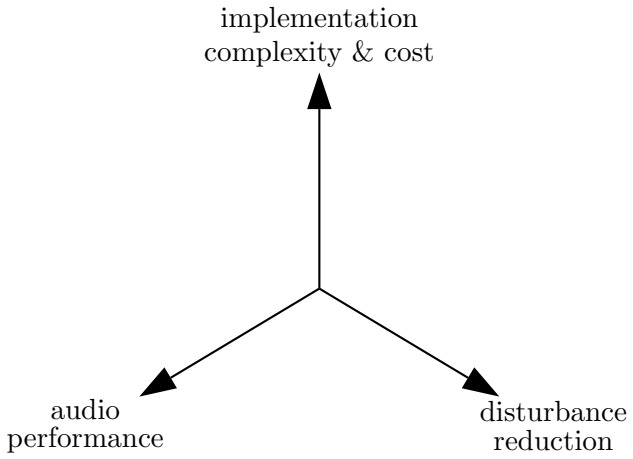
3.6 Predistorted Pulse Width Modulation

A method to remove the energy at a specific switching harmonic to a certain amount was presented in [89] and extended to a complete removal of a switching frequency harmonic by [90]. Both of the presented methods require a high order nonlinear computation of the program material. While the first method - called selective harmonic spreading - acts like a static dithering, i.e. it avoids all the disadvantages named in section 3.5 and really lowers the energy of some spectral components, it is creating intermodulation distortion in the audio band. The second method, named harmonic elimination spectra, keeps the audio performance, but is not capable of lowering more than one spectral component. The choice of this component is fixing the design and the high order nonlinear precomputation, so it cannot be changed online.

Table 3.6 Characteristics of predistorted PWM.

advantages	disadvantages
• addresses specific frequencies • invariant to tolerances	• requires excessive computational power • impact on audio performance • increases complexity

Figure 3.6 Trade-off choices when implementing predistorted PWM.



The third chapter provided an overview of several used technologies at the state-of-the-art to avoid EMC problems and showed their trade-offs. The next chapter will show the first attempt how to deal with this given problem in another way, which was inspired by the described techniques in this chapter.

Chapter 4

Multi Carrier Modulation

Inspired from the existing technologies and their trade-offs as described in chapter 3, multi carrier modulation (MCM) strives to overcome some of the described disadvantages. This chapter will describe the original idea, the boundaries for its realization and the evolution of the realization. The implementation itself has been described in publications as a product of this research work and will be briefly summarized here. To conclude, the achieved results will be summarized and some open chances and challenges within multi carrier modulation will be described.

4.1 Fundamentals

The basic idea of MCM is to lower the out-of-band spectrum by utilizing the frequencies between harmonics and their sidebands of a PWM signal. As opposed to frequency hopping (3.4) and dithering (3.5), the newly introduced spectral components shall be used continuously to avoid a negative impact on the audio performance (2.1.2). The resulting spectrum shall use more frequencies, but all of them at a lower level than PWM. The overall out-of-band energy may be invariable. In contrast to interleaving (3.3), this alternative modulation topology shall be applicable to half-bridge power stages. This way there is no question arising about trade-offs between common mode and differential mode.
Taking this framework into account, it appears natural to split the energy of one PWM spectrum into two PWM spectra, with two different carrier frequencies. This is e.g. done by comparing one reference signal (program

material minus error) with two triangular signals. Both of those comparators are providing a PWM signal at each of their outputs. The implementation is now bounded by the argument, that it should be possible to drive a single half-bridge power stage. Therefore the two PWM signals need to be combined in a manner, which is not affecting the audio performance. Therefore a logic circuit has been developed, that combines these two PWM streams into a single signal [91, 92]. Parts of these combination have been inspired by the commutator from [90] and the whole circuit was implemented in programmable logic by [93].
Further on it was proven, that the same topology can be used for various topologies of power converters [94].

4.2 Properties of Multi Carrier Modulation

MCM enables a reduction of the peaks of the out-of-band spectral components by 6 dB. This energy is not removed, but split into two spectral components, each of them having sidebands. Additionally intermodulation components of them appear. It is desirable to keep the intermodulation components away from the output filters resonance frequency. The spectral location and the corresponding amplitudes of all frequencies where simulated in [95]. In [93], these where analytically proven, and it was shown, that this way of combining two or more PWM signals does not have a negative intrinsic impact on the audio performance.
So far these approaches considered the spectral behaviour of MCM. Another way to analyze this modulation scheme with respect to PWM can be done in the time domain. Here the number of switching instances can reveal further properties of the technology. A numerical approach revealed, that the resulting MCM stream has a higher number of transitions than the underlying PWM streams. The MS-MCM combination of a 200 kHz and a 235 kHz based PWM signal (those have 400.000 and 470.000 transitions per second respectively) has around 625.000 transitions per second. A more thorough investigation for different MCM frequency combinations and an analytical analysis can give a better understanding of the effective switching frequency.
PWM is coding a given signal level into a proportional pulse width at any given instance in time, as illustrated in figure 2.6. This is not generally true for MCM. MCM is approaching this behaviour, when approaching the extrema of the modulation range (average duty cycle close to 0 % or 100 %). Inbetween, the pulses of an MCM signal are in average proportional to the input level, however not necessary proportional at any instance of time. This means that a low input signal, which would generate approximately 50 % duty cycle in a PWM stream, can result in very short or very long pulses temporarily like in pulse density modulation.

An MCM pulse stream is repetitive with the lowest period of the lowest intermodulation frequency of the carriers.

4.3 Outlook

The above described properties have not been included in [91–95]. However they are of interest for a power electronics designer. The link to the qualifiers of switch-mode audio power amplifiers and power supplies is provided in this section.

4.3.1 Challenges

The short peaks, also known as spikes, in an MCM stream can lead to a decrease in audio quality, when the rest of the amplifier is not carefully designed for the reception of those. Each output of a circuit has an output impedance and each input has an input capacitance. These parasitic components lead to a low-pass, which limits the edge of the pulses. When the pulse width of a spike is getting lower than this rise time, the receiving circuit might not trigger and the spike is overseen. This happens in the case of PWM streams, when duty cycles close to 0 % and 100 % occur, which happens only close to clipping of the amplifier. The information in pulses, which are skipt by this phenomenon, is lost and therefore audio quality is degraded. As this degradation is happening for PWM streams close to clipping it is of lower importance, while for MCM streams it can occur at lower listening levels. The two protoypes developed in [91, 93, 95] where suffering from this limitation and therefore had worse audio performance than PWM. For future designs it is recommended to account for this effect.
An open point of this technology is, to find a definite relationship its effective switching frequency compared to other modulation topologies.

4.3.2 Chances

On the other hand, MCM is offering more correction possibilities for the control loop, as it has more switching instances than PWM. Every time a transition happens, the controller can correct for the error at the output, so the increased transition number is offering a higher bandwidth of the control loop than PWM. The implementation of these principles was described in [96]. This possibility was not utilized in [91, 93, 95] either.
The reduction of disturbances of communication receivers was verified by the mentioned MCM designs. Therefore it can be concluded, that the out-of-band behaviour of MCM is 6 dB better than a comparable PWM de-

sign. This also holds for comparison with other popular modulation topologies, like self-oscillating and delta-sigma designs as their out-of-band spectral peaks are as high as the ones in PWM. This was shown in [97].

4.4 Summary

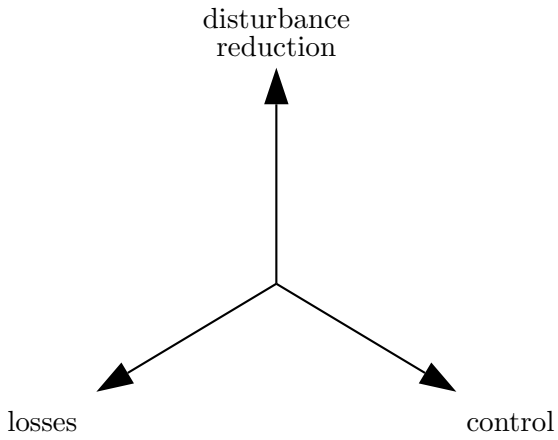
The described characteristics of MCM, to improve the interference situation between switch-mode power electronics and communication receivers results in pros and cons, which are given in table 4.1.

Table 4.1 Characteristics of multi carrier modulation.

advantages	disadvantages
• halving disturbance • higher bandwidth • invariant to temperature changes • invariant to component tolerances	• information coded in narrow spikes • causing losses • introduces out-of-band intermodulation components

The resulting trade-offs for industrialization of this solution are summarized in figure 4.1.

Figure 4.1 Trade-offs for multi carrier modulation.



Being inspired from the techniques described in the last chapter, this chapter provided a different approach to deal with the given problem of this project. While the solution space was limited to the modulation principle here, it was decided to broaden the view for the following work and include other parts of the circuit in the research. Therefore the next approach described in the next chapter is targeting the power stage and output filter.

Chapter 5

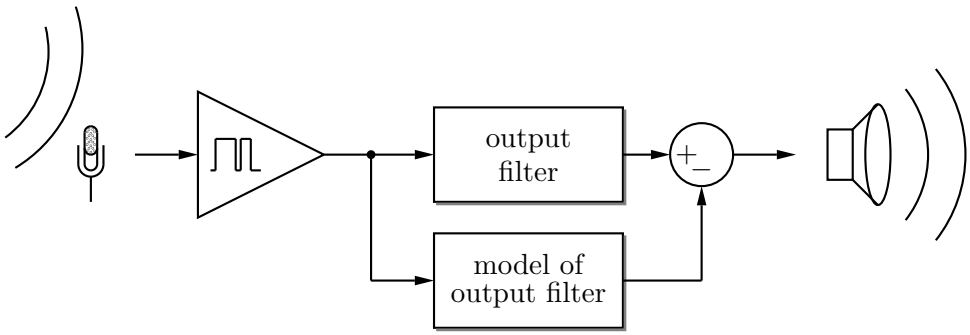
Active Electromagnetic Cancellation

As opposed to the research based on the modulation topology in the last chapter, the approach for improving the out-of-band behaviour in power electronics circuits described here is meant to take other parts of switch-mode designs into account. The most obvious ones are the parts, where the disturbances originate, i.e. the power stage, and the most common coupling path for high frequent energy, i.e. the output. The transfer function from power stage to output are classically described by low-pass filters, which are meant to remove the out-of-band energy. Despite passive approaches, active approaches have been known for several applications [98–105]. Implementation of those principles in switch-mode audio power amplifiers comes with an extra challenge. While the known active EMI filters mainly work for DC-DC power supplies in steady state and saturate during transition times, the filters for AC-DC applications have a couple of decades between the passband (mostly 50 Hz / 60 Hz) and the switching frequency, which is supposed to be filtered. This situation is different in switch-mode audio power applications. As the pass-band is reaching up to 20 kHz there is typically only one decade to the switching frequency, which is meant to be suppressed.

5.1 Fundamentals

The basic idea behind active electromagnetic cancellation (AEC) is shown in figure 5.1.

Figure 5.1 Block diagram of the idea behind active electromagnetic cancellation (AEC).



The program material, represented by the input through the microphone in the figure, is amplified by a switch mode audio power amplifier. At its output, the program material is passed through the output filter to drive the transducer, while the undesired switching residuals are canceled by the active filter, represented by a model of the output filter.
The model of the output filter reconstructs the ripple, which is expected to occur at the output. Having this signal available, it can be subtracted from the output, so that the resulting ripple is zero.

5.2 Properties of Active Electromagnetic Cancellation

There are various requirements for the circuit model of the output filter. In the audio band, the filter shall not act, i.e. the audio needs to be suppressed as much as possible. Out-of-band, the signal needs to have the same shape as the switching residual after the output filter of the switch-mode audio power amplifier. Including the minus sign of the summation block, sets another requirement: the phase of the prototype filter needs to be inverted with respect to the output filter. To match all those requirements, a similar design method as described above (section 2.2.3) was used in [106]. There, a couple of different filter realizations, starting with ideal filters and ending with characteristics of real filters, are suggested for this purpose, and the most practical one was implemented. The implementation proved the theory and showed a disturbance reduction of 15.1 dB. Furthermore the reduction was proven to be in the range of 12.7 dB and 20.9 dB over a typical range of production tolerances.
The active cancellation was realized by a separate amplifier. This amplifier

drives the same load as the main audio power amplifier and has to provide the ripple voltage across this load. Depending on the dimensioning of the passive part of the filter, the active one has to provide more or less output energy, which leads to additional losses in the active filter part.

5.3 Outlook

Even though the technique of AEC was profen to be quite effective in removing undesired out-of-band signals, there are both challenges and chances left to explore in future.

5.3.1 Challenges

To suppress the contents material in the active filter, a high pass functionality is required. This can be realized by a series blocking capacitor or a parallel shunt inductor. If the DC output of the switch-mode audio power amplifier is not exactly zero, the blocking capacitor or shunting inductor respectively will integrate this offset and saturate. This disables the active filter. A possible way to deal with this, is to introduce leakage in the capacitor (parallel resistor) or a serial resistor in the inductor. Even more advanced versions could sense the signal across the blocking capacitor or the shunt inductor and remove DC actively by means of local feedback. This is creating another chance for the whole system, as the active correction system can be used as a servo amplifier to remove also DC from the main audio amplifier.
Comparing the efforts described in section 2.2 with AEC, it is clear, that these two efforts are counterproductive. While section 2.2 describes how to design the control loop of a switch-mode audio power amplifier to form an optimized carrier, AEC is removing parts of this signal. So both, the closed loop transfer function from the switch-mode audio power amplifier and the prototype of the output filter need to be developed with respect to each other. There might be trade-offs arising between audio performance and removal of out-of-band energy. However the latter one is not intrinsically contrary to loop shapping efforts, as a complete removal of the switching residuals would also remove the impact of the carrier through feedback and the modulator would get a signal at its input, similar to a linear amplifier. While this is no problem for switch-mode audio power amplifiers with external carriers, the oscillation criterion [107] in self-oscillating amplifiers is impacted.

5.3.2 Chances

AEC opens also further possibilities. The linear output stage of the active filter can be used for driving parts of the audio signal. The advantage of linear amplifiers is, that they allow for more gain in the error amplifier as they are not restricted by sampling ($1/\pi \cdot f_{sw}$ for two-level modulated amplifiers and $2/\pi \cdot f_{sw}$ for three-level modulated amplifiers according to [61] and f_{sw} for self-oscillating amplifiers [107]). This means the AEC approach needs to be combined with the approach in [108]. However the more signal driven through the linear amplifier, the more energy losses it will create there. When combining these methods, it needs to be taken into account, that the cancellation stage needs to fulfill the audio performance specifications as has been described in chapter 2.
To further improve the cancellation of out-of-band energy, the signal can be sensed behind the summing block and fed into the active filter as an error signal. In this case an error amplifier can help removing even more disturbing signals. The further improvement is limited by the gain in the out-of-band range and might be practically limited by the bandwidth of the active prototype of the output filter.

5.4 Summary

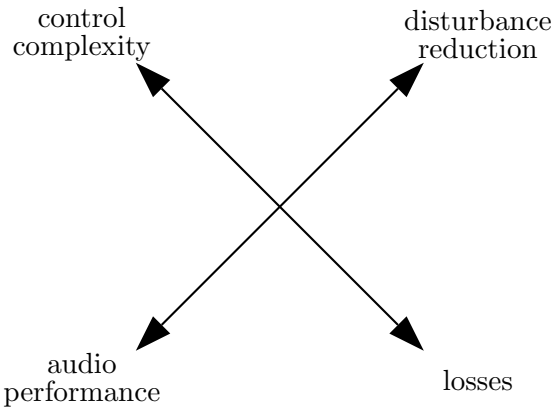
These properties result in the validation of AEC as a solution to receiver disturbance as given in table 5.1.

Table 5.1 Characteristics of active electromagnetic cancellation.

advantages	disadvantages
• excessive disturbance reduction • allowing higher bandwidth	• saturation effects due to DC offset need to be taken into account • sensible to component tolerances

When implementing this solution, power electronics designers need to weight the arguments given in figure 5.2.

Figure 5.2 Trade-offs for active electromagnetic cancellation.



The previous and the actual chapter where focusing on the improvement of the problem between switch-mode power electronics and EMC by alternative approaches with a focus on the involved signals. As the preventive measures against EMC problems are building the limit for size shrink in switch-mode audio power applications, the next chapter will primarily focus on the minimization of the circuits. This is one of the major desired advancements from this project.

Chapter 6

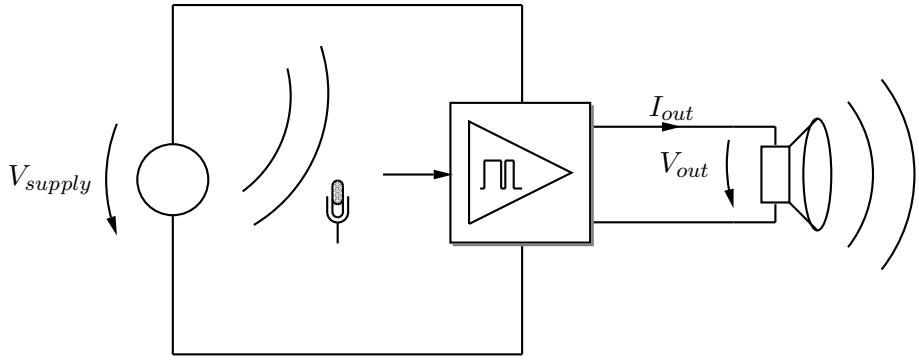
Current Driven Power Stages

While the previous two chapters where targeting different parts of a block diagram of switch-mode power converters, the alternative approach presented in this chapter will question the converters principles. This is done to explore the major show stopper for minimizing the circuits, i.e. the size of the output filter. The only purpose of the output filter is to reduce the disturbance of communication receivers. For all other qualifiers of switch-mode (audio) power electronics — like efficiency, audio quality, cost and size — the output filter is rather cumbersome.

6.1 Fundamentals

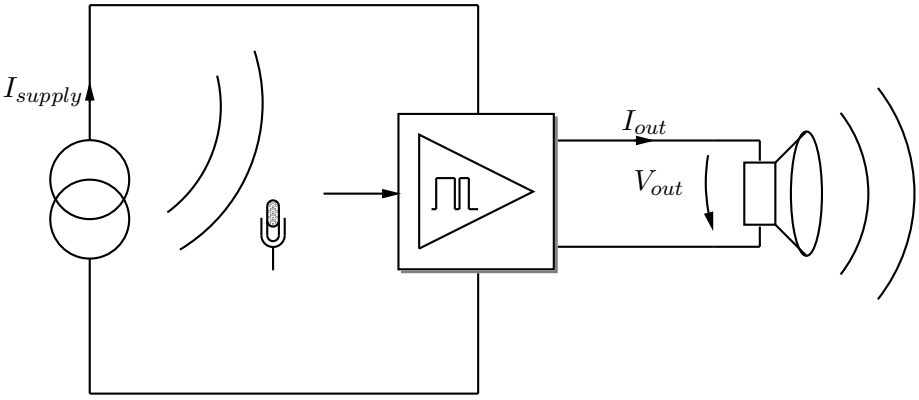
Nearly without exception, power supplies and amplifiers are built to operate from a voltage source, which might consist of DC, AC or a mixture of both. The idea of current driven power stages (CDP) arose from moving the output filter over some nodes in a typical voltage driven power stage (VDP). The block diagram of such one is shown in figure 6.1.

Figure 6.1 Principle supply-to-load configuration in conventional voltage driven power stages



The CDP, as in figure 6.2, must fulfill the same specifications as its voltage driven counterpart.

Figure 6.2 Principle supply-to-load configuration in current driven power stages



However the circuit realization is different as described in [109]. The major difference is the realization of the output filter. While keeping the load R, the damping factor d and the period of the resonance frequency T_r for both filters constant, the components, realizing the low pass, change in value from L_v and C_v to L_i and C_i as given in 6.1.1.

Equation 6.1.1 Equivalent filter components in CDPs.

$$\begin{aligned} L_i &= R^2 C_v \\ C_i &= \frac{L_v}{R^2} \end{aligned}$$

This leads to the relations as given in

Equation 6.1.2 Relation between filter components and their energy between VDPs and CDPs.

$$\frac{E_{i_L}}{E_{v_L}} = \frac{L_i}{L_v} = \frac{1}{4d^2} \qquad \frac{E_{i_C}}{E_{v_C}} = \frac{C_i}{C_v} = \frac{L_v}{L_i} = 4d^2$$

For practical realizations this results in a lower inductance and higher capacitance value for CDPs compared to VDPs. While the total amount of energy, stored in the filter components for a given signal is equal in both configurations, its distribution is different. For CDPs, the energy stored in the electrical field of the capacitor is higher, than the energy stored in the magnetic field of the inductor. According to practical informations in [110], it is less space consuming to store energy in capacitors than in inductors as long as the inductor is not operating under superconducting conditions, which are still impractical for many applications. Gathering information about components, which are enabling CDPs and comparing them with the available components for VDPs results in a volume reduction of the output filter by a factor of 6.

6.2 Properties of Current Driven Power Stages

When turning a power electronics circuit from voltage driven to current driven, each series connection turns into a parallel connection, an inductor turns into a capacitor and a voltage source turns into a current source. Considering a half-bridge voltage driven power stages, where the switches have to withstand twice the supply voltage, while they carry once the load current, a current driven half-bridge has to withstand only once the output voltage but twice the supply current.
As it can occur in VDPs that the switches in the power stage are exposed to both positive and negative currents while conducting, it also can happen, that the power switches in CDPs have to block both positive and negative voltage drops across their power terminals.
To avoid a phenomenon called shoot through, which means shorting the

supplies of a VDP, switch-mode power electronic designers introduce a state — called dead time — in the control of VDPs. During this time neither one of the switches is conducting. For CDPs approximately the same amount of time is needed as an overlap time to prevent the voltage across the power stage from rising.

6.3 Outlook

The described features of CDPs result in different challenges and chances for the practicing power electronics developer. This section is giving the details of those, again with respect to the broadly known VDPs.

6.3.1 Challenges

The majority of power switches on the market are designed for rather high voltages than currents. Taken into account, that CDPs have to conduct twice the supply current but only once the output voltage, the choice of components is limited.
A further limitation on the selection of power switches is the fact, that the power devices in CDPs have to block both, forward and reverse voltages. This puts the demand on the power switches to be bidirectional and therefore excludes commonly used components like MOSFETs. Realization possibilities for those have been given in [111]. Another way to realize those are JFETs [112], which are available both with and without body diode. JFETs come with an additional advantage for this topology, because those are normally-on devices. This means that they are conducting as long as there is no control voltage applied to them. This is desirable for CDPs and is naturally generating the required overlap as long as the control circuit is in turn-on and turn-off transitionss. Recent developments in the power semiconductor industry brought silicon carbide (SiC) devices to the market. The default version of those fulfill these requirements.

6.3.2 Chances

When overcoming the above mentioned drawbacks, CDPs ease a couple of design challenges known from VDPs.
Many applications come with relatively long supply cables as the energy source is located far away from its sink. These wiring harnesses or cables have a high parasitic inductance, which turns them into equivalent current sources. To avoid high voltage peaks in VDPs, power engineers use de-

coupling capacitors to clamp the voltages. Besides the above mentioned inductors, those capacitors are the physically biggest components in VDPs. By using CDPs, the parasitics of the cabling can be used as current coupling and it is desired to have as low capacitance as possible on the energy input terminals. This removes the bulky decoupling capacitors completely.
Another excellent current source are solar cells. While conventional converters for solar cell applications turn the equivalent current source of the cell into a voltage source by clamping the voltage with capacitors or batteries, CDPs can be used to directly convert the solar energy into the desired output signal waveform. It is then only limited by the specifications of the solar cell and the amount of sunlight.
Other realization possibilities, based on conventional power electronic circuits are described in [113]
Within integrated power electronics it is desired to prevent circuits from destruction by overload. This can both occur as voltage or current overdrive. While it is relatively unproblematic to implement voltage sensing and act upon certain trigger levels via security mechanisms, it is difficult to measure the current in series with VDPs. In CDPs, this is simple to implement. The corresponding voltage sensing is not getting any more complicated, than it is in VDPs, which overall allows for more effective protection circuitries.

6.4 Summary

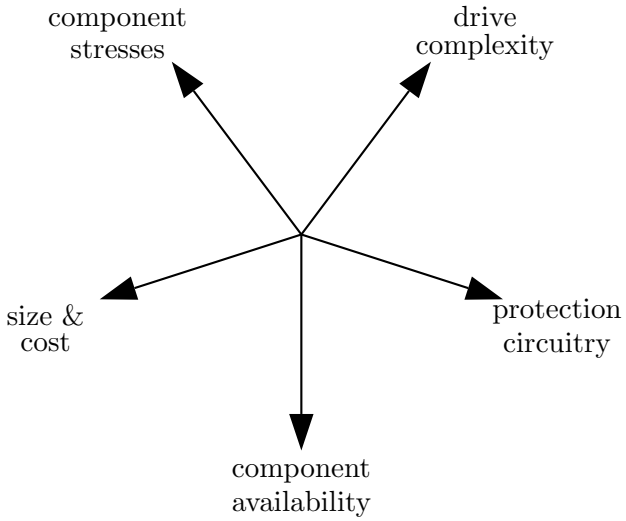
Suppling power electronic circuits with currents instead of voltages leads to different properties as given in table 6.1.

Table 6.1 Characteristics of current driven power stages.

advantages	disadvantages
• decreasing size of filters	• complexity of switches
• can remove decoupling components	• non standard driver circuits required
• directly applicable to solar cells	• no disturbance reduction
• decreasing complexity of protection circuits	

For product realization with CDPs, the trade-offs in figure 6.3 need to be considered.

Figure 6.3 Trade-offs for current driven power stages.



While the previous two chapters where dealing with parts of power converters, this chapter took the whole system into account. Focusing on the physical minimization of the power circuits, which is mainly prevented by EMC filtering components, an alternative topology was described in this chapter. While this approach did not target to change the spectral contents of the relevant signals, the next chapter will strive for even further size reduction by doing so.

Chapter 7

Radio Frequency Switch-Mode Power Electronics

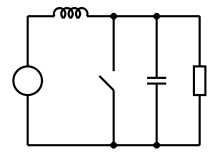
While the thoughts for chapter 4 where dominated by signal considerations, the ideas behind chapters 5 and 6 where driven by system and especially circuitry thinking. The approach in this chapter is rather motivated by signal considerations, again especially in the spectral domain. Focusing on audio applications and considering the communication receivers as described in 1.3 it can be concluded, that it is most desireable to avoid AM and FM band distortion. The reason, why the AM band is placed at relatively low radio frequencies, is that very long distance communications can be established in this frequency range in real time. This is not possible with discrete time systems, as those are suffering from latency times. As long as real time distribution of information is of interest for society, the AM band will be used for it.
This chapter is exploring the chances to completely avoid disturbance of those frequency bands by simply putting the switching frequency beyond the FM band. This can result into removal of the bulky filters in switch-mode power electronics. Rather than a realized solution, this chapter is pointing toward future possibilities and setting the fundamentals for that.

7.1 Possibilities with Radio Frequency Switch-Mode Power Electronics

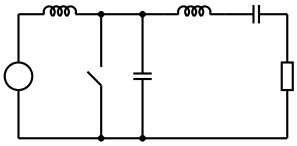
Increasing the switching frequency of power electronics equates the strive of records. So far, the academical approaches for high frequent power stages

[114–124] and their control strategies [125] led to various topologies as shown in figure 7.1.

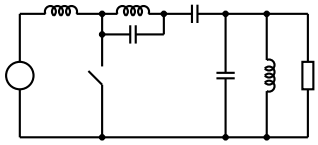
Figure 7.1 Topology overview of radio frequency amplifiers and their evolution to radio frequency power supplies.



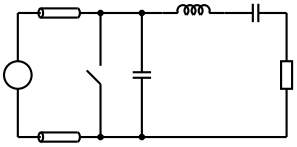
(a) Class-C amplifier [114]



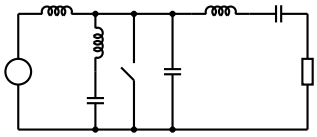
(b) Class-E amplifier [115]



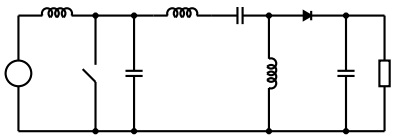
(c) Class-F amplifier [116–118]



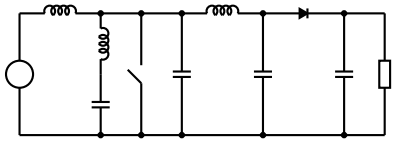
(d) Class-Φ amplifier [119]



(e) Class-Φ_2 amplifier [120]



(f) Class-E^2 converter [121]



(g) Resonant Boost converter [124]

To find a quantitative comparison between the presented converter types, two figures of merit (FOM) are provided. FOM_1 provides a handle to compare the output power level P_{out} and switching frequency f_s, while FOM_2 is further taking the efficiency η (defined between 0 and 1 for this purpose) into account. A third figure of merit would be useful for comparing also the possibility of utilizing the absolute maximum ratings of the required switches compared to the supply values. However most of this data have not been provided in the referred references.

Equation 7.1.1 Figures of merit (FOM) to allow comparison of radio frequency switch-mode power supplies.

$$\begin{aligned} FOM_1 &= P_{out} \cdot f_s \\ FOM_2 &= FOM_1 \cdot \eta \end{aligned}$$

The quantitative achievements of the above explained amplifiers and converters are shown in table 7.1.

Table 7.1 Comparison of measured achievements with the above described topologies.

Topology	P_{out} W	f_s MHz	FOM_1 GHzW	η %	FOM_2 GHzW	Reference
Class-C	180	—	—	89	—	[114]
Class-E	26	3.9	0.1	96	0.1	[115]
Class-E^2	10	1	< 0.1	80	< 0.1	[121]
Class-E^2	1	1	< 0.1	82	< 0.1	[122]
Class-Φ	178	15.7	2.8	75	2.1	[119]
Class-Φ_2	500	30	15	92	13.8	[120]
RF-Boost	6000	2.5	15	—	—	[123]
Resonant RF-Boost	110	23	2.5	87	2.2	[124]
Resonant RF-Boost	17	50	0.9	74	0.6	[124]
Resonant RF-Boost	50	22	1.1	78	0.9	[125]

Many of the advances have been summarized in [126], which is on the other hand also giving plenty of resulting challenges. Despite the ones mentioned there, it appears that control over a wider operating temperature range, component tolerances in the circuits and similar practical considerations have not been explored by the above mentioned research approaches. Also control techniques for the radio frequency switch-mode power circuits are not adequately explored yet.
As has been mentioned in the last chapter, new advances in power semiconductors like [127, 128] allow power electronics circuits to be designed for switching frequencies beyond the FM band. This is changing the demands on filtering: instead of the bulky filters to remove energy in the AM band, the focus has to be set on filtering in the FM band. Components for these requirements have been possible and available since long time, as these are the components to build the transmitters for broadcasting applications.
The possibilities allowed by those techniques and components have been exploited in [129].

7.2 Outlook

Radio frequency switch-mode power electronics have been explored in academics and recent developments in power components allow their industri-

alization in near future. This section is briefly summarizing the challenges and chances advancing from this technology.

7.2.1 Challenges

Through the high rate of transitions, radio frequency switch-mode power supplies naturally come with increased switching losses. The evolution of power semiconductors is helping to keep those down to a decent level, however they must be considered by the practicing engineer as a major design parameter.
Conducting power in circuits from one path to the other is also dependent on the speed of the power devices. The recent developments in removal of reverse recovery times of diodes through SiC devices is one way of allowing high switching frequencies.
Another important qualifier is the voltage and current stress of the power semiconductors. As these circuits are not operating with rectangular waveforms, other crest factors than one – which is ideal in conventional power electronics — emerge. This is putting extra stress on the components, while this headroom cannot be utilized for higher power conversion levels.
As the above described topologies mainly operate in resonant modes, other modulation and control schemes than pulse width modulation are of interest. This can be pulse density or pulse frequency modulations.
For resonant operation, the presented radio frequency designs rely on impedance matching circuits over a broad frequency range. To achieve this, parasitic components are included. The available processes, allowing high frequent power operation, come with unacceptable high tolerances, so the resonant operation can not be achieved by design yet.

7.2.2 Chances

On the other hand the application of these control schemes can be designed to higher loop gains for comparable order regulators. Reason for that is the advances in control bandwidth, which is limited by switching frequency as described in section 5.3.2.
Relating radio frequency switch-mode power supplies back to the disturbance of receivers, there switching frequency can be placed in a manner to avoid interference with the low frequent broadcasting services. This allows a major shrink in size by removing the bulky filter components. Further research toward industrialization of those circuits is therefore strongly recommended.

7.3 Summary

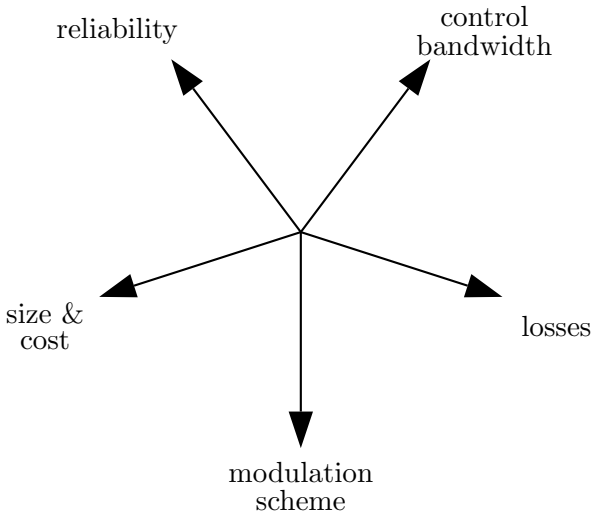
Several arguments point toward radio frequency switch-mode power supplies as a solution for receiver disturbance avoidance and other advantages, however there are also negative sides. This is discussed in table 7.2.

Table 7.2 Characteristics of radio frequency switch-mode power electronics.

advantages	disadvantages
• size reduction	• higher component stresses
• higher bandwidth	• causing losses
• disturbance removal in AM band	• different modulation schemes required
	• temperature sensitive
	• component tolerance sensitive

For the practicing power electronics designer in industry, the following arguments need to be taken into account, when using radio frequency switch-mode power supplies in products.

Figure 7.2 Trade-offs for radio frequency switch-mode power electronics.



While the previous chapter provided a possibility toward shrinking the size of the filtering components, this chapter has been giving an outlook to topologies, which remove the bulky filter components. Increasing the switching frequency beyond the broadcasting frequencies of AM and FM radio does not simply lead to a scaling in circuits, but rather into different topologies, which have been researched during the last decades. Recent advances in power semiconductors allow for realizing those, while there are still unresolved practical issues, like component tolerances. Taking the enormous advantages of those topologies into account it is desirable to put further research efforts on overcoming the drawbacks.

Chapter 8

Conclusion

This work addresses the interference of switch-mode power electronics with receivers used in communication technologies. This is commonly known as electromagnetic compatibility (EMC).
The thesis first describes the history of EMC and the evolution of switch-mode power electronics. It is recalled, that the purpose of EMC is to allow communication systems to operate without getting influenced. The reason, why switch-mode power electronic circuits are especially critical in this sense, is given when exploring the coherence between EMC and power electronics. The improvement of the link between those on the power electronics side was defined as the target of this project. A special focus is set on audio applications.
Before exploring ways to improve this, another correlation involved by the questioned signals is summarized. The work of others is linking the EMC critical signals resulting as residuals from the switch-mode nature of power electronics to the audio performance of switch-mode audio power amplifiers. The background of audio performance and the influence from switch-mode signals are given.
Switch-mode audio power applications have been industrialized since many decades and the problem of EMC decoupling has been solved in those. The characteristics of the major existing solutions and their trade-offs for the practicing engineer are described. It is found, that the generally accepted solutions in industry involve physically big filter components, which set a boundary for further size limitation and therefore limit the possible application range of switch-mode power circuits. The summary of those implemented solutions was taken as the basis for improving the interference from

power electronics to communication receivers and evolved into four suggested solutions for improving the situation. Those are

- Multi Carrier Modulation (MCM)
- Active Electromagnetic Cancellation (AEC)
- Current Driven Power Stages (CDP) and
- Radio Frequency Power Electronics (RF SMPS).

These four solutions are described in technical detail in this work and its linked publications. The major achievements are

- halving the spectral peaks through MCM
- 15 dB output ripple reduction through AEC
- an output filter size shrink of 84 % through CDPs and
- complete avoidance of interference through RF SMPS.

The impact on design considerations for the practicing product designer are given in this work. Besides those improvements, further questions arise.

- For MCM, a deterministic relationship between the used carrier frequencies and the resulting effective switching frequency is missing. The answer to this question would allow further insight into extended control capabilities in relation with MCM.
- MCM is generating short pulses for any modulation index. This resulted into glitches. For limiting their effect on the audio performance, the use of full-bridge power stages in conjunction with MCM is suggested. The validation of this solution has to be done.
- The implemented MCM where realized with two carriers. The behaviour and further improvement with more than two carriers is an open question.
- Closing a loop around AEC is suggested to help for both, the filter saturation problem through DC as well as further enhanced cancellation performance. Validation of these arguments is representing room for further research.
- The impact of AEC on the in-band performance has to be investigated.

- Implementation of CDPs with components, which have been recently introduced in the market, shall allow for high efficiency implementations. A demonstrator for this argument has to be built.
- CDPs have an impact on their energy source. While solar cells can be directly used, power supplies need to be reconfigured. One of the major changes is the removal of the bulky capacitive energy storage components on their outputs. Further power supplies have to be built, to demonstrate this.
- The ease of overload protection schemes in CDPs with respect to VDPs has to be prototyped.
- RF SMPS rely on soft switching for keeping the switching losses down to an acceptable level. A study of the fulfillment of those conditions versus temperature variations and component tolerances is missing.
- High control bandwidths, through high switching frequencies are expected, but have not been demonstrated yet.

The four presented solutions appear promising, but some more efforts in research and development have to be made, to allow final product realizations.

The problem between EMC and power electronics has been historically recalled, the connection to the audio performance of amplifiers was given and the existing solutions have been revised. Based on those, four suggestions for improving the out-of-band behaviour of switch-mode audio power amplifiers and power supplies were given, where the first one is an advancement through their modulation topology, the second one through active filtering, the third one through different power stages and the last one through complete avoidance of the problem by removing all spectral components away from the critical bands. This leads to merging the field of radio frequency electronics and power electronics. It is highly recommended to pursue further research toward industrialization of those solutions.

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Appendix A

Gesetz über das Telegraphenwesen des Deutschen Reichs

(engl. "Law of telegraphy from the German Empire")
vom 6. April 1892 (Reichsgesetzbl. S. 467)

§1 [1]Das Recht, Telegraphenanlagen für die Vermittelung von Nachrichtung zu errichten und zu betreiben, steht ausschließlich dem Reich zu. [2]Unter Telegraphenanlagen sind die Fernsprechanlagen mit begriffen.

§2 (1) Die Ausübung des im §1 bezeichneten Rechts kann für einzelne Strecken oder Bezirke an Privatunternehmer und muss an Gemeinden für den Verkehr innerhalb des Gemeindebezirks verliehen werden, wenn die nachsuchende Gemeinde die genügende Sicherheit für einen ordnungsgemäßen Betrieb bietet und das Reich eine solche Anlage weder errichtet hat, noch sich zur Errichtung und zum Betriebe einer solchen bereit erklärt.
(2) Die Verleihung erfolgt durch den Reichskanzler oder die von ihm hierzu ermächtigten Behörden.
(3) Die Bedingungen der Verleihung sind in der Verleihungsurkunde festzustellen.

§3 Ohne Genehmigung des Reichs können errichtet und betrieben werden:
1. Telegraphenanlagen, welche ausschließlich dem inneren Dienste von Landes- oder Kommunalbehörden, Deichkorporationen, Siel- und Entwässerungsver-

bänden gewidmet sind;
2. Telegraphenanlagen, welche von Transportanstalten auf ihren Linien ausschließlich zu Zwecken ihres Betriebes oder für die Vermittelung von Nachrichten innerhalb der bisherigen Grenzen benutzt werden; 3. Telegraphenanlagen
a) innerhalb der Grenzen eines Grundstücks,
b) zwischen mehreren einem Besitzer gehörigen oder zu einem Betriebe vereinigten Grundstücken, deren seines von dem anderen über 25 Kilometer in der Luftlinie entfernt ist, welche diese Anlagen ausschließlich für den der Benutzung der Grundstücke entsprechenden unentgeltlichen Verkehr bestimmt sind.

§4 Durch die Landes-Zentralbehörde wird, vorbehaltlich der Reichsaufsicht (Art. 4 Ziffer 10 der Reichsverfassung), die Kontrolle darüber geführt, dass die Errichtung und der Betrieb der im §3 bezeichneten Telegraphenanlagen sich innerhalb der gesetzlichen Grenzen halten.

§5 (1) Jedermann hat gegen Zahlung der Gebühren das Recht auf Beförderung von ordnungsmäßigen Telegrammen und auf Zulassung zu einer ordnungsmäßigen telephonischen Unterhaltung durch die für den öffentlichen Verkehr bestimmten Anlagen.
(2) Vorrechte bei der Benutzung der dem öffentlichen Verkehr dienenden Anlagen und Ausschließung von der Benutzung sind nur aus Gründen des öffentlichen Interesses zulässig.

§6 (1) Sind an einem Orte Telegraphenlinien für den Ortsverkehr, sei es von der Reichs-Telegraphenverwaltung, sei es von der Gemeindeverwaltung oder von einem anderen Unternehmer, zur Benutzung gegen Entgelt errichtet, so kann jeder Eigentümer eines Grundstücks gegen Erfüllung der von jenen zu erlassenden und öffentlich bekannt zu machenden Bedingungen den Anschluss an das Lokalnetz verlangen.
(2) Die Benutzung solcher Privatstellen durch Unbefügte gegen Entgelt ist unzulässig.

§7 [1]Die für die Benutzung von Reichs-Telegraphen- und Fernsprech-Anlagen bestehenden Gebühren können nur auf Grund eines Gesetzes erhöht werden. [2]Ebenso ist eine Ausdehnung der gegenwärtig bestehenden Befreiungen von solchen Gebühren nur auf Grund eines Gesetzes zulässig.

§8 Das Telegraphengeheimnis ist unverletzlich, vorbehaltlich der gesetzlich für strafgerichtliche Untersuchungen, im Konkurse oder in civilprozessualis-

chen Fällen oder sonst durch Reichsgesetz festgestellten Ausnahmen. Dasselbe erstreckt sich auch darauf, ob und zwischen welchen Personen telegraphische Mitteilungen stattgefunden haben.

§9 Mit Geldstrafe bis zu eintausendfünfhundert Mark oder mit Haft oder mit Gefängnis bis zu sechs Monaten wird bestraft, wer vorsätzlich entgegen den Bestimmungen dieses Gesetzes eine Telegraphenanlage errichtet oder betreibt.

§10 Mit Geldstrafe bis zu einhundertfünfzig Mark wird bestraft, wer den in Gemäßheit des §4 erlassenen Kontrollvorschriften zuwiderhandelt.

§11 [1]Die unbefugt errichteten oder betriebenen Anlagen sind außer Betrieb zu setzen oder zu beseitigen. Den Antrag auf Einleitung des hierzu nach Maßgabe der Landesgesetzgebung erforderlichen Zwangsverfahrens stellt der Reichskanzler, oder die vom Reichskanzler dazu ermächtigten Behörden. [2]Der Rechtsweg bleibt vorbehalten.

§12 Elektrische Anlagen sind, wenn eine Störung des Betriebes der einen Leitung durch die andere eingetreten oder zu befürchten ist, auf Kosten desjenigen Teiles, welcher durch eine spätere Anlage oder durch eine später eintretende Änderung seiner bestehenden Anlage diese Störung oder die Gefahr derselben veranlasst, nach Möglichkeit so auszuführen, dass sie sich nicht störend beeinflussen.

§13 [1]Die auf Grund der vorstehenden Bestimmung entstehenden Streitigkeiten gehören vor die ordentlichen Gerichte. Das gerichtliche Verfahren ist zu beschleunigen (§§198, 202 bis 204 der Reichs-Zivilprozessordnung). [2]Der Rechtsstreit gilt als Feriensache (§202 des Gerichtsverfassungsgesetzes, §201 der Reichs-Zivilprozessordnung).

§14 Das Reich erlangt durch dieses Gesetz keine weitergehenden als die bisher bestehenden Ansprüche auf die Verfügung über fremden Grund und Boden, insbesondere über öffentliche Wege und Straßen.

§15 Die Bestimmungen dieses Gesetzes gelten für Bayern und Württemberg mit der Maßgabe, dass für ihre Gebiete die für das Reich festgestellten Rechte diesen Bundesstaaten zustehen und dass die Bestimmungen des §7 auf den inneren Verkehr dieser Bundesstaaten keine Anwendung finden.

Appendix B

Publications

B.1 Multi Carrier Modulator for Switch-mode Audio Power Amplifiers, 124th AES Conv., 2008, Amsterdam, Netherlands, linked to chapter 4

B.2 A novel Modulation Topology for Power Converters utilizing Multiple Carrier Signals, PESC Conf., 2008, Rhodes, Greece, linked to chapter 4

B.3 Comparison of three different Modulators for Power Converters with Respect to EMI Optimization, ISIE, 2008, Cambridge, England, linked to all

B.4 Active Electromagnetic Interference Cancellation for Automotive Switch-Mode Audio Power Amplifiers, 36th AES Conf., 2009, Detroit, USA, linked to chapter 5

B.5 On the Myth of Pulse Width Modulated Spectrum in Theory and Practice, 126th AES Conv., 2009, Munich, Germany, linked to all

B.6 Multi Carrier Modulation Audio Power Amplifier with Programmable Logic, 37th AES Conf., 2009, Hillerød, Denmark, linked to chapter 4

B.7 Investigation of switching frequency variations in self-oscillating class D amplifiers, 127th AES Conv., 2009, New York, USA, linked to all

B.8 Modeling Distortion Effects in Class-D Amplifier Filter Inductors, 128th AES Conv., 2010, London, England, linked to all

B.9 Electrical Load Detection Apparatus, US020100019781A1

B.10 Power Distribution Arrangement, US020100027169A1

B.11 Controllable Circuit, US020100039084A1, linked to chapter 4

B.12 Internal Report: Current Driven Power Stages, Technical University of Denmark, DTU 92501-10, 2010, linked to chapter 6

B.13 A Self-Oscillating Control Scheme for a Boost Converter Providing a Controlled Current, Submitted for review at IEEE Transactions on Power Electronics, TPEL-2010-07-0641, 2010, linked to chapter 6

B.1 Multi Carrier Modulator for Switch-mode Audio Power Amplifiers

124th AES Conv., 2008, Amsterdam, Netherlands, linked to chapter 4

Audio Engineering Society

Convention Paper

Presented at the 124th Convention
2008 May 17–20 Amsterdam, The Netherlands

Multi Carrier Modulator for Switch-mode Audio Power Amplifiers

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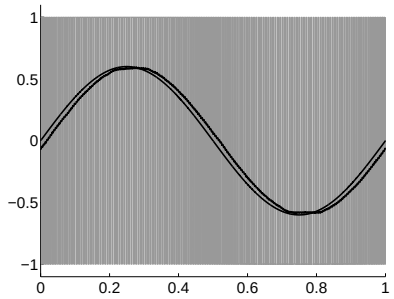
ABSTRACT

While switch-mode audio power amplifiers allow compact implementations and high output power levels due to their high power efficiency, they are very well known for creating electromagnetic interference (EMI) with other electronic equipment, in particular radio receivers. Lowering the EMI of switch-mode audio power amplifiers while keeping the performance measures to excellent levels is therefore of high general interest.
A modulator utilizing multiple carrier signals to generate a two level pulse train will be shown in this paper. The performance of the modulator will be compared in simulation to existing modulation topologies. The lower EMI as well as the preserved audio performance will be shown in simulation as well as in measurement results on a prototype.

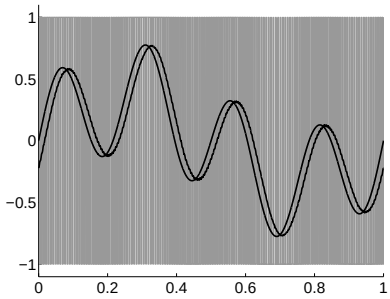
1. INTRODUCTION

Switch-mode audio power amplifiers are well known for their high efficiency but also for their electromagnetic compatibility (EMC) problems. The causality of electromagnetic measurements are mainly to avoid interaction between electronic equipment. The test levels are dominantly determined by the very high sensitivity of broadcasting receivers like amplitude modulated (AM) and frequency modulated (FM) radio. As switch-mode audio power amplifiers are located in close proximity to those receivers by the nature of their purposes, the coupling between them is eased. For good signal reception it is therefore highly desirable to create as low disturbance signals as possible in their sensitivity bands.
Nonlinear modulators, as used in switch-mode audio power amplifiers are responsible for creating signals in such frequency ranges. The spectral content is required to drive switch-mode power stages at a high power effective level.

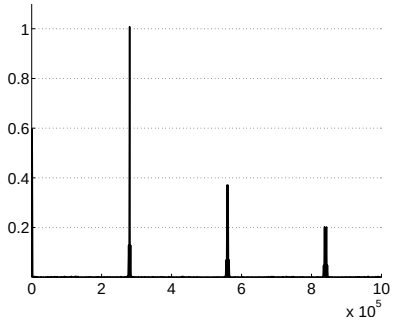
Fig. 1 PWM waveforms and spectra: left side shows a single sine wave input and right side shows the superposition of two sine waves. The spectral plots are the FFT of the two level PWM signal on linear and logarithmic scales.



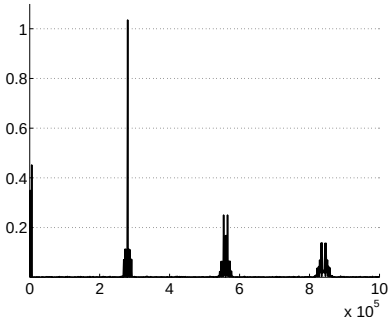
a) single tone waveforms



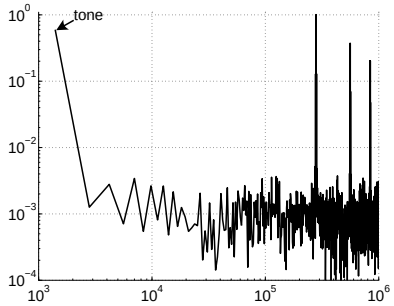
b) two tone waveforms



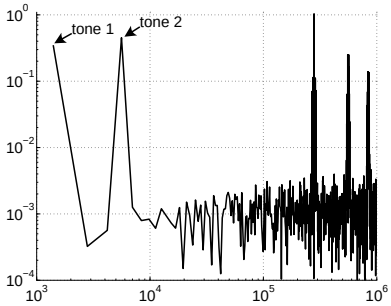
c) single tone spectrum on linear scale



d) two tone spectrum on linear scale



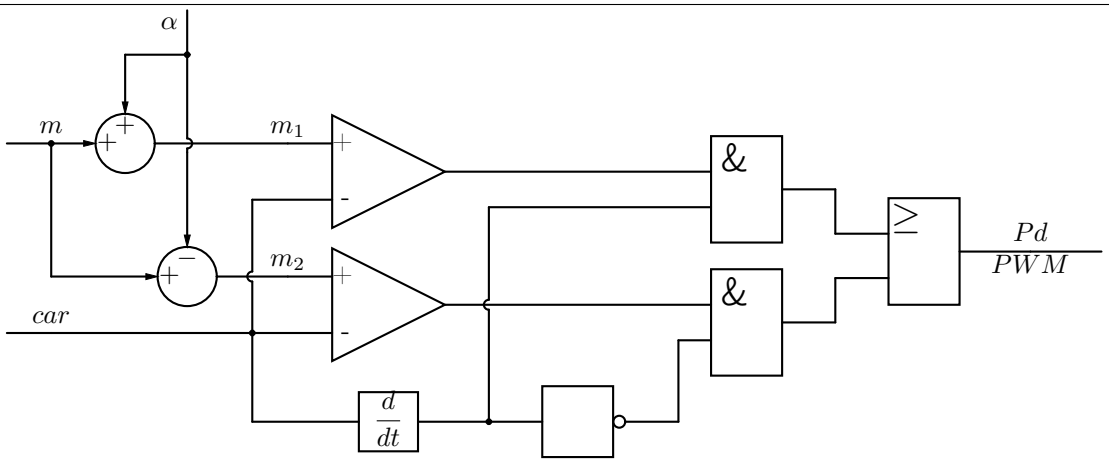
e) single tone spectrum on logarithmic scale
$x = 0.6 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$



f) two tone spectrum on logarithmic scale
$x = 0.35 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4 \text{ Hz} \cdot t)$

One common known technique is a two level, double side pulse width modulation (PWM). Figure 1 shows waveforms and spectra of the output of such a modulator. The time domain diagrams 1 a) and b) show the input signal and the output signal of the simulated amplifier. The output signal is overlaid by ripple and is delayed in time. The grey background waveform shows the two level PWM signal. Figures 1 c) and d) illustrate the EMI challenge while on the logarithmic plots e) and f) the reproduction of the audio signal without any further audible signals after the modulator is best visible. Note that the dynamical range of the simulation was limited to necessary dimensions to obtain practical simulation times.

Fig. 2 Block diagram of a Predistorted PWM according to [1]



Analytical derivations of these spectra can be obtained by using the method of a double Fourier series [2], which was applied to PWM by [3].
While such traditional modulation topologies use mechanical shielding and passive filtering only for dealing with EMI challenges, more recent approaches try to affect the spectral shape at its source. Therefore recent endeavors in improvement of switch-mode audio power amplifiers started to concentrate on the out-of-band behavior. A way to influence specific single spectral components was shown in [1] and [4] with predistorted PWM (Pd-PWM). Here, the audio input reference signal r to a modulator was additive and subtractive superimposed by a correction term α and generated two new reference signals m_1 and m_2 as shown in equation 1.1.

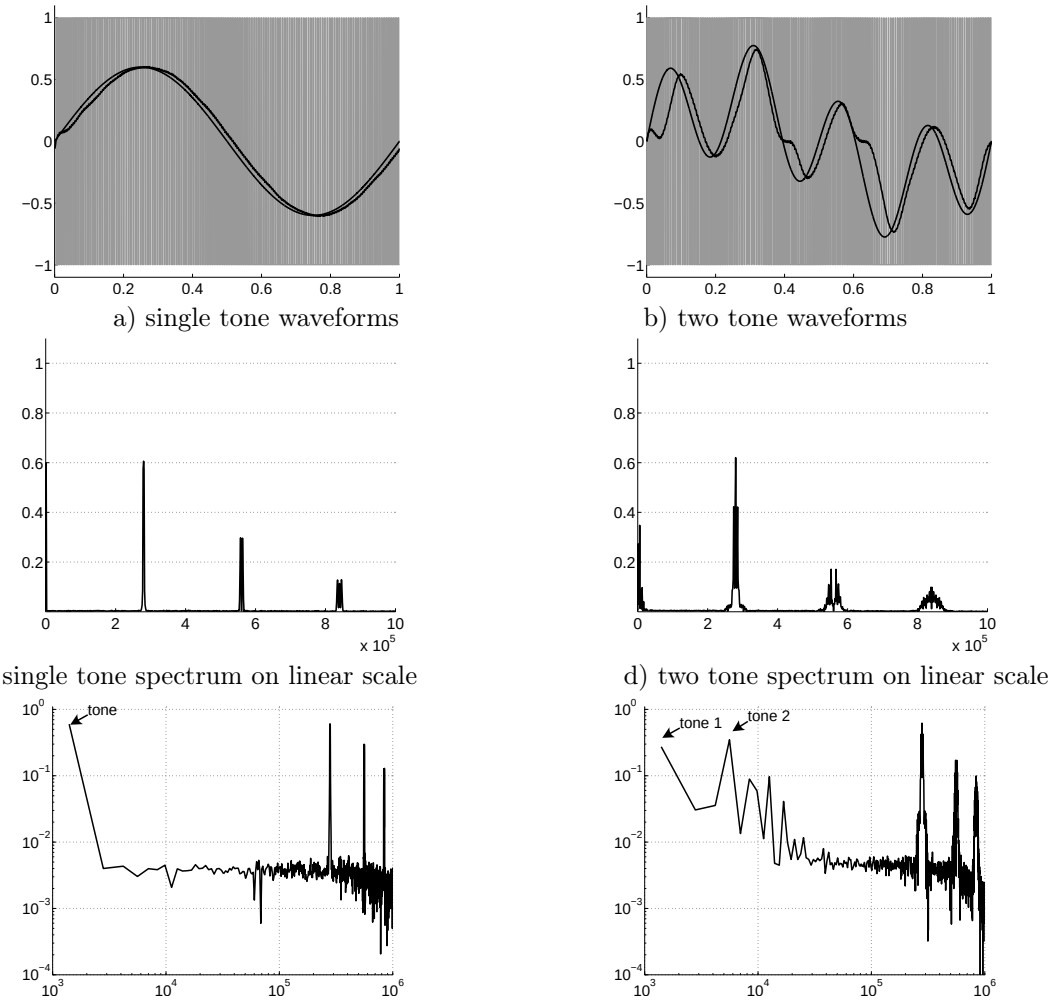
Equation 1.1 Predistortion equations

$$m_1 = r - \alpha$$

$$m_2 = r + \alpha$$

The new reference signals m_1 and m_2 are compared with a carrier and fed into a commutator. The correction term α allows to eliminate single components in the spectrum. Figure 2 shows the complete modulator and commutator.
Different versions (Switching Harmonic Spreading (SHS) and Harmonic Elimination Spectra (HES)) allow different resulting spectral shapes. However both versions come with a high computational effort as the correction term α is a higher order representation of the original reference signal r. While SHS adds intermodulation distortion does HES not correct the peaks in the carrier frequency and its harmonics.
Figure 3 shows diagrams for an SHS Pd-PWM comparable to figure 1. The EMI peaks, as illustrated best in figure 3 c) and d) are lower than the ones shown from a conventional modulator, however there are some undesired tones in the audio spectrum, when applying a two tone input to the modulator (figure 3 f)).
The series of those calculations is extended to the HES Pd-PWM in figure 4. Here the intermodulation distortion (figure 4 f)) is nearly as low as shown above in case of a PWM modulator, however also the EMI peaks at the switching frequency are back to unity (figure 4 d)). The main advantage of this modulation principle is to lower specific peaks in the EMI spectrum which can be seen in the same figure.
This paper describes a new modulator, which is capable of lowering all spectral out-of-band components while keeping the full audio performance. The modulator will be described in section 2 and the theoretical methods as used above will be applied to the new principle in section 3 also taking the described techniques in perspective to the new modulator. A prototype of the proposed technique was built and

Fig. 3 Predistorted PWM waveforms and spectra: Switching Harmonic Spreading (SHS). The two tone column shows intermodulation distortion.



$x = 0.6 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$

$x = 0.35 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t) + 0.45 \cdot \sin(2 \cdot \pi \cdot 4 \text{ Hz} \cdot t)$

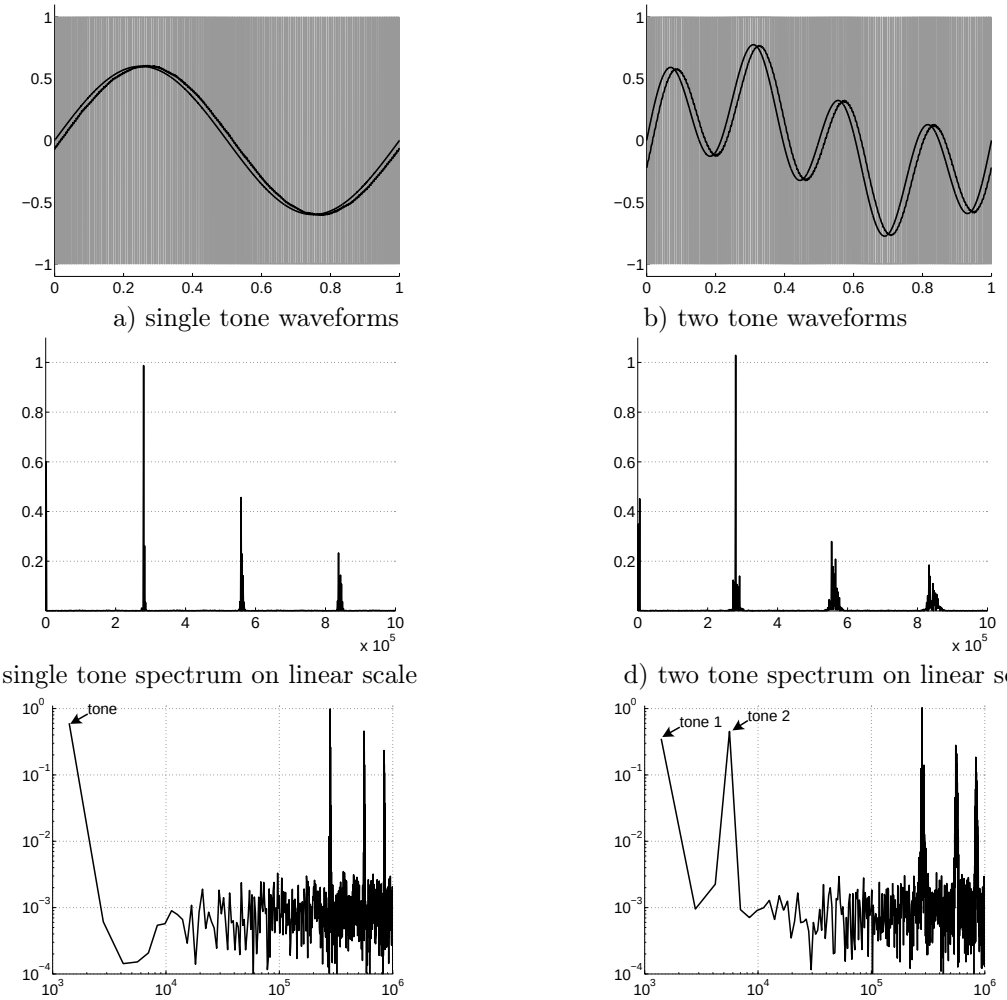
validates the simulations in section 4. After showing the measured audio performance of the model in section 5, the paper concludes with section 6.

2. MULTI CARRIER MODULATOR

The new modulator utilizes two or more different carrier frequencies which are applied to the input of the modulator. A carrier is a triangular waveform which is fed into a comparator together with the audio signal. This procedure creates a two level representation of an audio signal to drive a power stage at a very high efficient level. Such a Multi Carrier Modulator (MCM) is shown in figure 5.

The reference signal r is fed into multiple comparators. Triangular or saw tooth shaped signals $carN$ are applied to each of the other inputs of the comparators. Each of those carrier signals is based on

Fig. 4 Predistoted PWM waveforms and spectra: Harmonic Elimination Spectra (HES). The intermodulation distortion from SHS is gone, however the high peaks from a PWM are also back.



a) single tone waveforms

b) two tone waveforms

c) single tone spectrum on linear scale

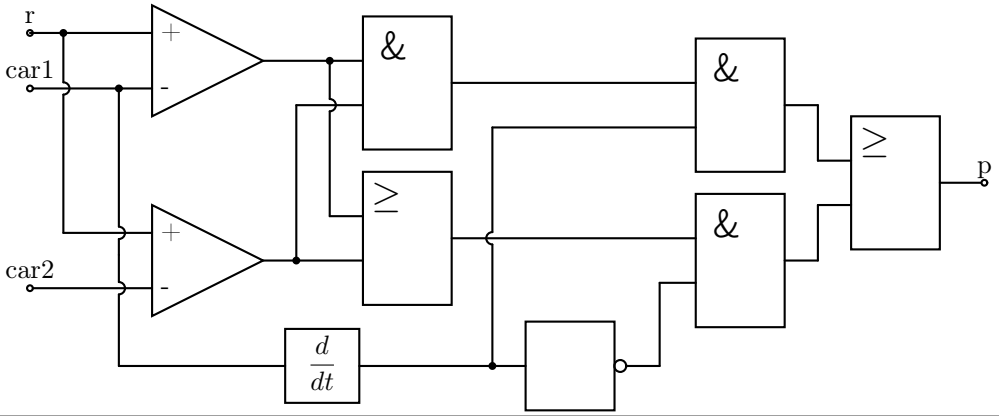
d) two tone spectrum on linear scale

e) single tone spectrum on logarithmic scale
$x = 0.6 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$

f) two tone spectrum on logarithmic scale
$x = 0.35 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4 \text{ Hz} \cdot t)$

a different frequency. Beat tones are avoided by deriving those carrier frequencies from a common high frequency clock. The outputs of all comparators are fed into an AND gate and an OR gate and the level of one of the applied clocks (master clock) determines which of the two gates output signal is commutated to the power stage. The resulting bit stream p is a linear transformation of the audio input within the audio band but consists only out of two levels which makes it useable for a highly efficient drive of a power stage. The commutator is identical to the one used by [4]. It selects, dependent on a master clock, if either the output of the above described AND gate or the output of the above described OR gate is passed on to the power stage. It also assures that at any time only one of those outputs is commuted via sig-

Fig. 5 Block diagram of a Multi Carrier Modulator MCM



nal p. Practically the carrier signals are derived by integrating a square wave. Instead of differentiating this signal again to obtain the square wave used as master clock, the original square wave can be used.

3. SIMULATION RESULTS

For best comparison the same input signals where applied to the MCM as shown above. Results are shown in figure 6.

An MCM shows a different ripple behavior. The signal at the output after a low pass shows the audio signal overlaid with all switching frequencies and their intermodulation products. This additional ripple phenomenon can best be seen in figures 6 a) to d). However the audio band is not altered by the modulator as shown in both 6 e) and f) for a single sinusoidal input as well as a two tone simulation. Both of those diagrams give additionally an overview of the intermodulation frequencies outside the audio band.

To compare the performance of a switch-mode audio power amplifier to kinds of measures are important: the performance within the audio band (in-band) and the performance above the audio band (out-of-band). The facts for all shown modulators within the audio band are taken into perspective in table 1.

HD_{2nd} and HD_{3rd} denote the second and third harmonic distortion and $IIM-$ as well as $IIM+$ represent the negative and positive in-band intermodulation components.

The out-of-band behaviour is compared in table 2 by the out-of-band peak OPK and the negative and positive out-of-band intermodulation components $OIM-$ and $OIM+$. The simulations where carried out with a two carrier modulator model.

Table 1 In-band performance comparison

	HD_{2nd}	HD_{3rd}	$IIM-$	$IIM+$
PWM	0.21 %	0.46 %	0.08 %	0.32 %
SHS	0.67 %	0.72 %	10.19 %	3.77 %
HES	0.10 %	0.02 %	0.56 %	0.15 %
MCM	0.85 %	0.51 %	0.12 %	0.38 %

Table 2 Out-of-band performance comparison

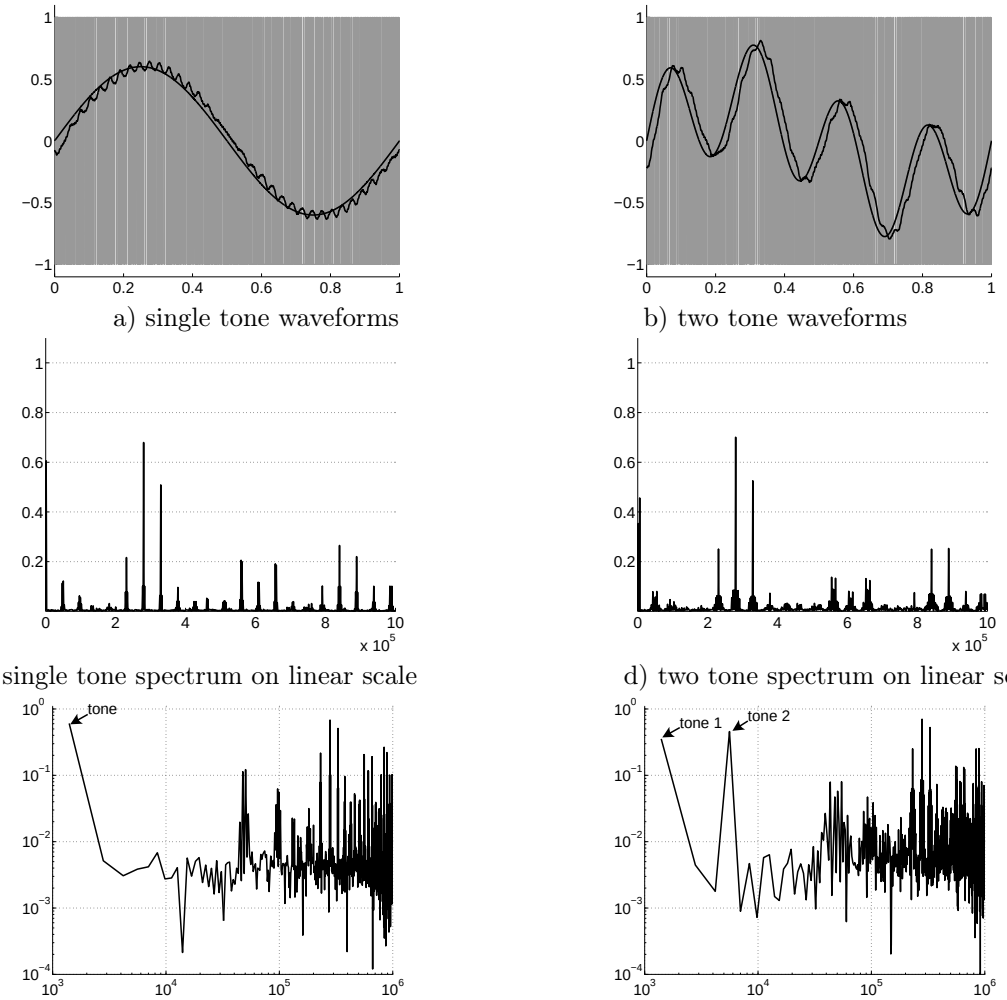
	OPK	$OIM-$	$OIM+$
PWM	1.01	− − −	− − −
SHS	0.61	− − −	− − −
HES	0.99	− − −	− − −
MCM	0.68	0.003 [1]	0.004 [2]

4. VALIDATION

A prototype (figure 8) of an MCM with two carriers was built and applied to a single ended power stage followed by a second order low pass. A PI-controller was used to correct for nonlinearities in the level shifter, power stage and output filter. The first switching frequency f_{sw1} was set to 333 kHz and the second switching frequency f_{sw2} was set to

[1] side bands: 0.113 and 0.122
[2] side bands: 0.117 and 0.116

Fig. 6 Simulation of a Multi Carrier Modulator. The EMI peaks are lowered while no audio harmonics or intermodulation products are inserted in the audio band.



a) single tone waveforms

b) two tone waveforms

c) single tone spectrum on linear scale

d) two tone spectrum on linear scale

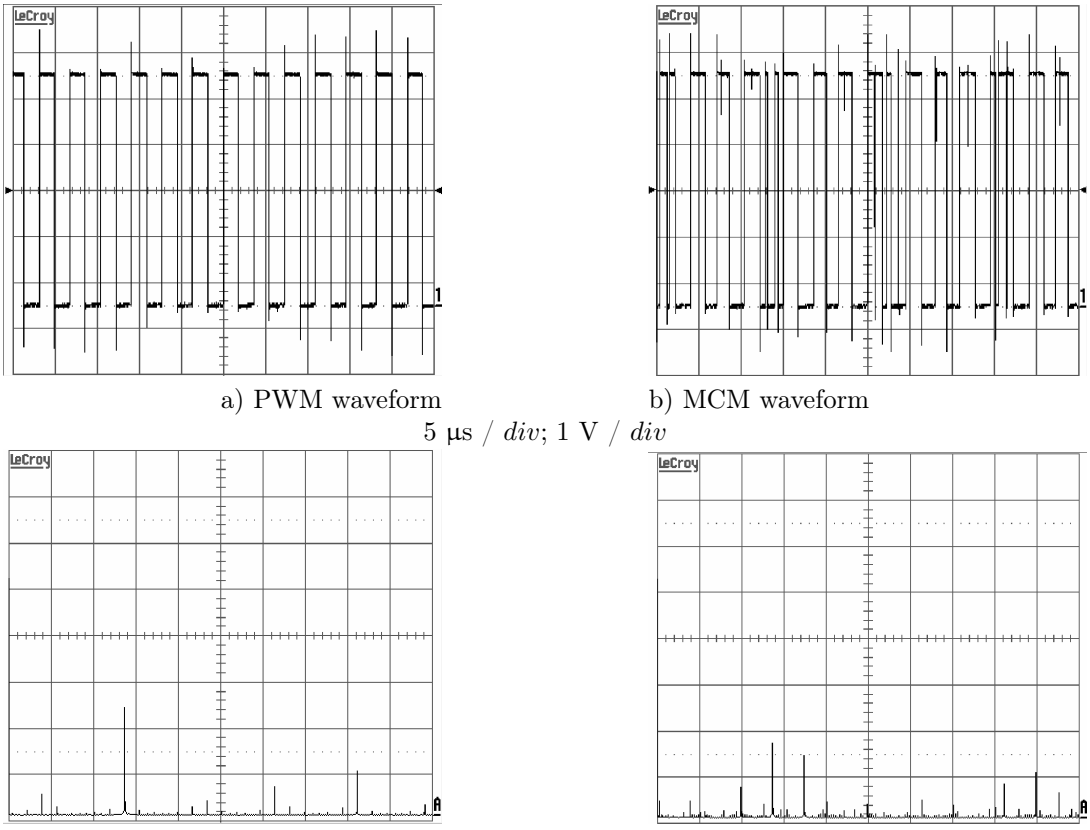
e) single tone spectrum on logarithmic scale
$x = 0.6 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$

f) two tone spectrum on logarithmic scale
$x = 0.35 \cdot \sin(2 \cdot \pi \cdot 1 \text{ Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4 \text{ Hz} \cdot t)$

250 kHz. Both carriers where derived from the same crystal oscillator and integrated to triangles.
Figures 7 a) and 7 c) show a conventional PWM signal without modulation in time and frequency domain. The same scope shots where taken on the output of the MCM prototype and figures 7 b) and 7 d) show the difference. Note that also those show the modulator during idle.

As predicted by simulation the peaks are lower with MCM and out-of-band intermodulation components occur. Practically these intermodulation components are lower than the peaks of a PWM signal and the lowest out-of-band intermodulation component is still outside the audio band. Therefore there are none of the undesired spectral components from an audio or an EMI perspective.

Fig. 7 PWM and MCM signals in time and frequency domain



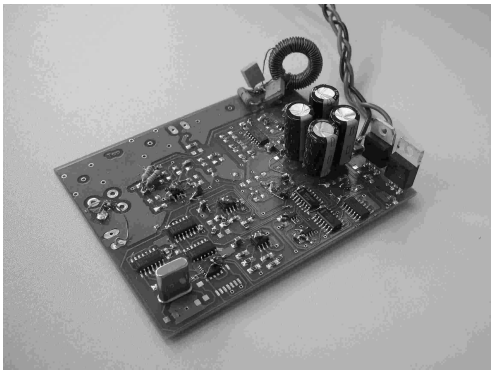
a) PWM waveform b) MCM waveform

5 µs / *div*; 1 V / *div*

c) PWM spectrum d) MCM spectrum

0.1 MHz / *div*; 1 V / *div*

Fig. 8 Picture of prototype



5. AUDIO RESULTS

The audio performance of the amplifier driven from an MCM was measured according to [5]. The spectral plot 9 captured by a 256 kbit FFT with Hanning window from a UPL (Rohde & Schwarz) shows the output of the MCM with no audio input. The signal to noise ratio (SNR) stays below 110 dB. The reference of the plot is the maximum unclipped output signal of the power stage which is 11.2 V_{pk}. The same plot was taken with nominal output signal and is shown in figure 10 which represents a total harmonic distortion including noise $THD + N$ around 0.1 %. Figures 11 and 12 show amplitude and phase response respectively with no load attached.

Fig. 9 Noise measurement of the prototype

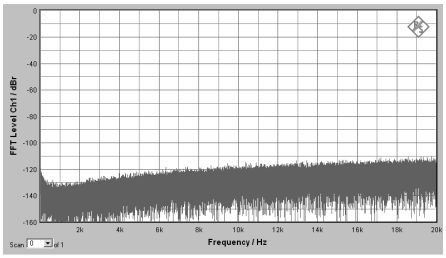


Fig. 10 Distortion measurement result of the prototype

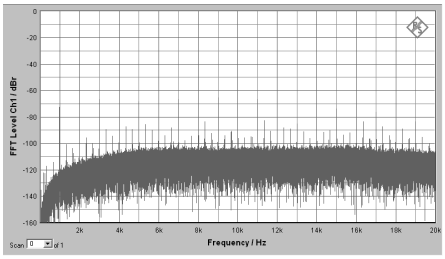


Fig. 11 Amplitude response of the prototype

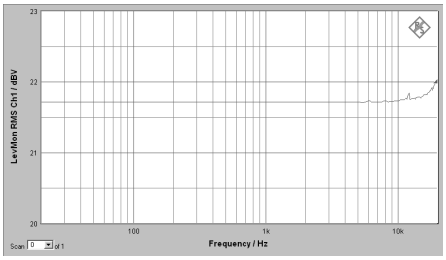
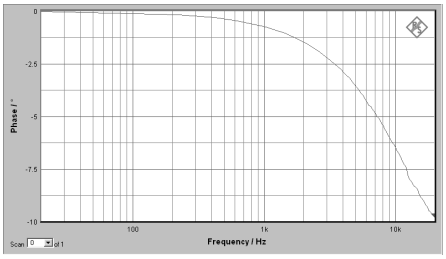


Fig. 12 Phase response of the prototype



6. CONCLUSION

A modulator utilizing multiple carrier signals was shown. This modulator lowers the out-of-band spectrum of a switch-mode audio power amplifier while keeping its audio performance. The simulation results where compared with existing modulators and a prototype was built to verify the audio performance. Distortion levels are around 0.1 %, the amplitude response shows a derivation lower than 0.2 dB. The phase response differs by 10 ° in the audio band. A dynamical range around 110 dB was measured. The new modulator is easy to implement and does not require computational effort.

7. REFERENCES

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[3] Harold S. Black. *Modulation Theory.* van Nostrand Reinhard Company, 1953.

[4] Xin Geng. *Design and Analysis of Pulse-Width Modulation Techniques for Spectrum Shaping.* PhD thesis, University of Illinois at Urbana-Champaign, Urbana-Champaign, Illinois, USA, 2007.

[5] Audio Engineering Society Inc. AES standard method for digital audio engineering - Measurement of digital audio equipment. Standard AES17, AES Standards, March 1998.

B.2 A novel Modulation Topology for Power Converters utilizing Multiple Carrier Signals

39th PESC Conf., 2008, Rhodes, Greece, linked to chapter 4

A novel Modulation Topology for Power Converters utilizing Multiple Carrier Signals

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***Abstract*—Power converters are known to generate spectral components in the range of interest of electromagnetic compatibility measurements. Common approaches to manipulate some selected components in these frequency ranges are shown here. These approaches add components to the input signal of the modulator to derive a slightly varied spectrum. To achieve a rectangular output signal, those modulators use a triangular or saw tooth carrier signal. A novel family of modulators is shown here, using more than one carrier signal to obtain a completely changed spectrum while maintaining the rectangular shaped waveform at the output.**

The multiple carriers are fed into multiple comparators and their outputs are intelligently combined by logic gates to get a single signal to drive one power stage of any type of converter. This commutation distinguishes between the four members of the novel family: the first one uses an or-gate to combine the signals; the second one utilizes therefore an and-gate. The third modulator combines the outputs of those two and switches between the or-output and the and-output after each pulse. The last described modulator is commutating one of the described outputs dependent on the state of a master clock.

The nonlinear operation of all modulators is described with nonlinear algebra in conjunction with Boolean algebra. The benefits for electromagnetic compatibility of the new schemes are presented, all modulators are examined in terms of steady state operation, dynamic behavior, maximum modulation range and added distortion. Finally the implementation of one of the modulators in a switch-mode power supply is presented. Experimental results are verifying the simulation.

***Index Terms*—Modulation, Pulse width modulated power converters, Electromagnetic compatibility**

I. Introduction

Error amplifiers for power converters consist of an error amplifier subtracting the output signal y from the input signal x and integrating the result. This is used as a reference signal r for a modulator, which is comparing it to a given carrier c. The pulse signal p drives a power stage to achieve the desired output power, voltage and current of the converter y. Figure 1 shows this generalized operating principle as block diagram of a power converter. The high degree of nonlinearity of comparators is used within pulse width modulators (PWM) to achieve rectangular signals. These rectangular signals p ensure a high efficient operation of power stages. Due to the nature of nonlinearity, several spectral components are added to the reference signal r and compromise the electromagnetic compatibility (EMC) performance of the system.

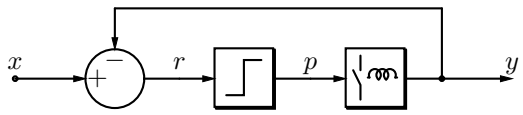


Fig. 1. Principal block diagram of a power converter

The transformation from reference r via carrier c to a PWM signal p_{PWM} is described by the simple nonlinear operation

$$p_{PWM} = \begin{cases} 1 \ \forall \ r < c \\ 0 \ otherwise \end{cases} \quad (1)$$

The spectral components of PWM can be described by the method of a double Fourier series (DFS) from Bennett [1], which was applied to pulse width modulation (PWM) by Black [2]. An important result in those derivations is, that a PWM signal consists out of spectral components in the pass band and sidebands around the switching frequency and its harmonics.

In switch-mode power converters the pass band can either be DC, AC or a mixture of both depending on the application. DC-DC converters in their steady state operation mode have a constant reference r fed into the comparator and therefore generate a constant duty cycle in the pulse stream p. As soon as line or load variations, input voltage or current perturbations or other disturbances are taken into account, the reference signal r starts to vary. DC-AC converters in contrast get an AC signal as input x which results in a constantly adjusting duty cycle of the pulse stream p. Figure 2 shows the signal and spectra of a commonly used, straight forward PWM for different input signals x. To cut out the effects of the modulation technique, the regulation loop was not closed and therefore $r = x$. Figures 2a, 2c, 2e and 2g show the signals x (solid black line), p_{PWM} (grey) and y_{PWM} (solid black line with ripple) and figures 2b, 2d, 2f and 2h show the spectrum of p_{PWM}. The output of the converter y is derived by applying a damped second order filter to the pulses p. This filter is dominating the step response and the time delay. The peaks to the right of the spectral

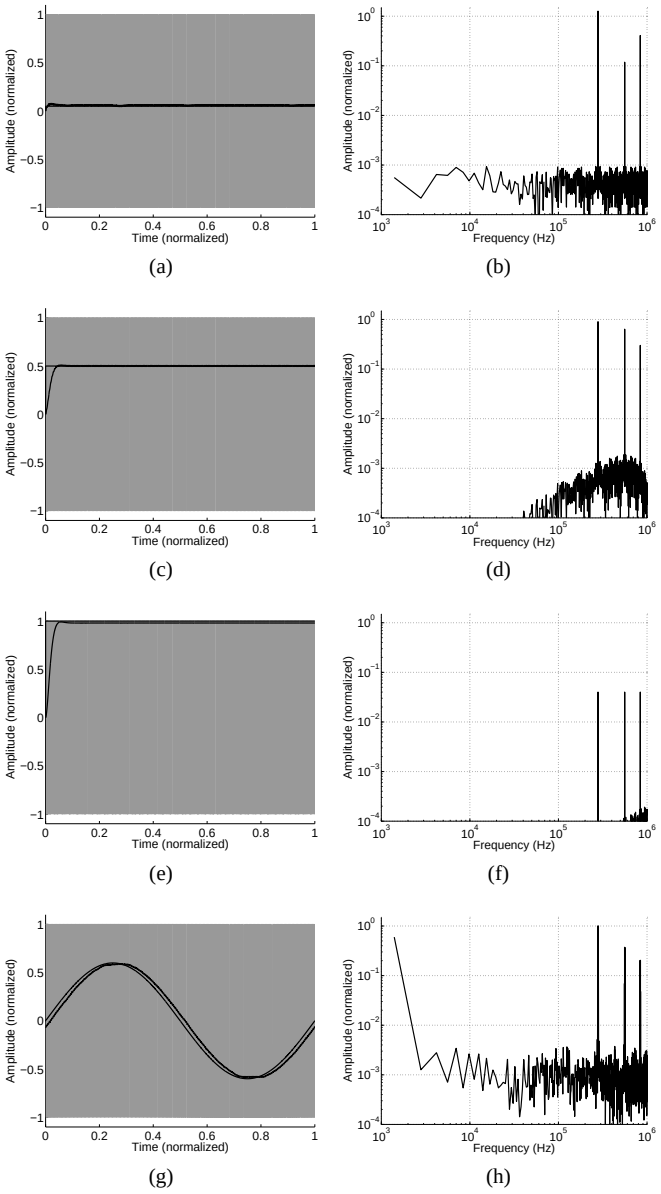


Fig. 2. Signals x, y_{PWM} and p_{PWM} (left) and spectra p_{PWM} (right) of a PWM with varying input signals ($x = 0.05$, $x = 0.5$, $x = 1$ and $x = 0.6\ \sin(2\pi t)$ from top to bottom).

plots represent the EMC problems.

To ensure a proper design to meet the stringent requirements of EMC specs, straight forward approaches try to break the coupling path from the source – the modulator and the power stage – to the sink, i.e. the measurement equipment of EMC setups. For detaching the galvanic coupling paths inductors and capacitors are used as passive filter elements. To achieve best decoupling results with those elements, even their parasitic elements have been widely used [3], [4], [5] and [6]. A common used technique to suppress the radiated coupling paths is to use mechanical shielding around critical components. It is however better to effect the spectral shape at its source. Specific spectral components have been canceled by [7] and [8]. Therefore the input signal r to the modulator has been changed to new modulator references $r_1 = r - a$ and $r_2 = r + a$ where a correction term a was used. The correction term a allows to eliminate single components in the spectrum. Different versions (Switching Harmonic Spreading and Harmonic Elimination Spectra) allow different resulting spectral shapes. However both versions come with a high computational effort as the correction term a is a higher order representation of the original reference signal r.

A novel approach is shown here which requires no computational power and targets the conglomeration of frequencies in the bands of electromagnetic compatibility interest. The proposed family of modulators uses multiple carrier frequencies as inputs to multiple comparators while maintaining the reference signal. The mathematical background is changing from a double Fourier series to a multidimensional problem, i.e. a triple Fourier series. These modulation schemes use gaps in the spectrum which had not been used before while lowering the extensive peaks which are the qualitative targets for EMC measurements. The pass-band performance will be revised and it will be shown that it does not suffer from the improvement out of band. Section II will describe the block diagram and explain the operation of the new modulators in theory, while section III will put simulation results to them. In an experiment one of the modulators was applied to a push-pull type supply and the specialty for this supply will be shown as well as measurements on the waveforms. Section V summarizes and concludes this paper.

II. Novel Approach utilizing Multiple Carriers

Where traditional modulators applied to power converters use one carrier frequency the new approach utilizes multiple of them. These carriers c_n – either triangular or sawtooth signals – are fed into one comparator each and are compared with the common reference signal r. Multi carrier modulation (MCM) is referred to such a novel system in this paper. To allow the new principle to drive a single power stage, the outputs of several comparators need to be combined intelligently to result in a single rectangular shaped signal p. Four possible principles are shown in this section and their atributes are given.

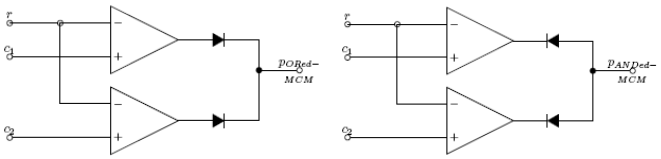
A. ORed MCM and ANDed MCM

A simple decision rule for combining the outputs of the comparators is a logical OR or a logical AND resulting into a ORed-MCM and an ANDed-MCM respectively. The mathematical operation to obtain those pulse trains are given in 2 and 3 respectively, where the decision conditions are written in Boolean algebra:

$$p_{ORed-MCM} = \begin{cases} 1\ \forall\ r < c_1 | r < c_2 \ldots r < c_n \\ 0\ otherwise \end{cases} \quad (2)$$

$$p_{ORed-MCM} = \begin{cases} 1\ \forall\ r < c_1 \& r < c_2 \ldots r < c_n \\ 0\ otherwise \end{cases} \quad (3)$$

The operator $|$ is representing a logical OR while $\&$ is representing a logical AND. The directions of the



(a) (b)

Fig. 3. Block diagrams of an ORed-and an ANDed-MCM with two carriers

in_1	in_2	out
0	0	0
0	1	1
1	0	1
1	1	1

mean value = 75 % ones

in_1	in_2	out
0	0	0
0	1	0
1	0	0
1	1	1

mean value = 25 % ones

TABLE I
STATISTICAL DISTRIBUTION OF ZEROS AND ONES IN LOGICAL OR AND AND GATES

inequation signs are of no importance to the modulation. Swapping them would cause the modulator to be inverting.

The block diagram of an ORed-MCM and an ANDed-MCM is shown in figures 3a and 3b respectivly. These two modulators distribute the energy of one peak as in PWM into two peaks, and therefore have two equally high peaks in the spectrum. Additionally they create an intermodulation component of those two frequencies. Due to the unbalanced distribution of zeros and ones in OR and AND gates, as shown in their truth tables I, the output signal of the modulator will have a DC offset. As the mean value of the bit stream is supposed to represent the input signal, it should be centered around $50\ \%$ ones, an ORed-MCM has an offset of $+25\ \%$ and an ANDed-MCM has an offset of $-25\ \%$ with respect to the full range of the modulator. This limits the modulation range in both cases to a maximum of $75\ \%$. As a further effect of the nonlinear operation in the pass band, both modulators are creating even order distortion.

B. ORANDing MCM

To overcome the disadvantages of very high nonlinear operation, the commutated signal to the power stage p can be switched from an ORed- to an ANDed-MCM after each pulse. The logical background for the decision time of the pulse signal p therefore is

$$p_{ORANDed-MCM} = \begin{cases} 1 & \forall\ p^{-1} = p^{-1}_{ORed-MCM} \& \\ & (r < c_1 \& r < c_2 \ldots r < c_n) \\ 1 & \forall\ p^{-1} = p^{-1}_{ANDed-MCM} \& \\ & (r < c_1 | r < c_2 \ldots r < c_n) \\ 0 & otherwise, \end{cases} \tag{4}$$

where p^{-1} denotes the previous pulse.

The block diagram (figure 4) of an ORANDed-MCM shows a realization of the commutation principle described above. This commutation scheme modulates the ORed- and the ANDed-MCM with each other, what reflects into the quadrature of the distortion and therefore changes even order distortion into odd order distortion. Furthermore an ORANDed-MCM has intrinsically gain, which is linear enough to allow nearly $100\ \%$ utilization of the dynamical range.

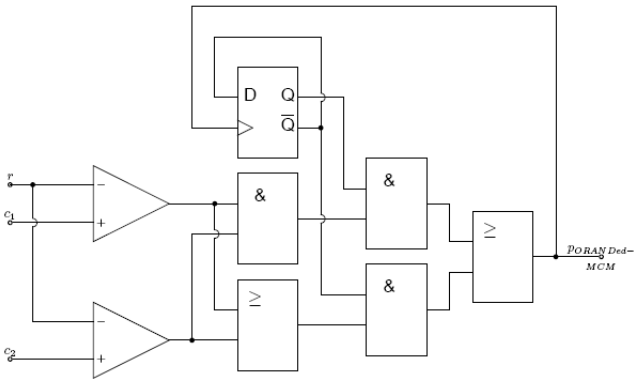


Fig. 4. Block diagram of an ORANDed-MCM with two carriers as an alternating commutation of an ORed-MCM and an ANDed-MCM to the power stage.

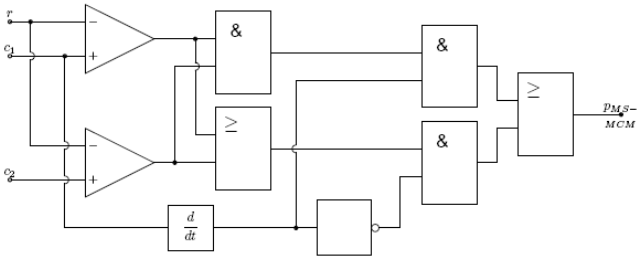


Fig. 5. Block diagram of a MS-MCM with two carriers, commutating the ORed-MCM and the ANDed-MCM in dependency of the state of the master clock.

C. Master Slave MCM

The odd order distortion can be removed when commutating the ORed- and ANDed-MCM outputs in dependency of a master clock (MCLK), which either can be one of the time basis for the carriers or any other rectangular waveform. A $50\ \%$ duty cycle clock is required here. Equation 5 gives the decision law for this modulator.

$$p_{MS-MCM} = \begin{cases} 1 & \forall\ MCLK = 1 \& \\ & (r < c_1 \& r < c_2 \ldots r < c_n) \\ 1 & \forall\ \overline{MCLK} = 1 \& \\ & (r < c_1 | r < c_2 \ldots r < c_n) \\ 0 & otherwise, \end{cases} \tag{5}$$

A modulator following this decision rule is called master slave MCM (MS-MCM) here. Figure 5 shows a MS-MCM which is deriving its master clock from one of its carrier inputs by integrating it.

A MS-MCM distributes the energy into multiple peaks in the spectrum, which are no longer equal in amplitude (as is in ORed- and ANDed-MCM). The signal path is linear in the pass band and can be used up to a modulation index of $100\ \%$.

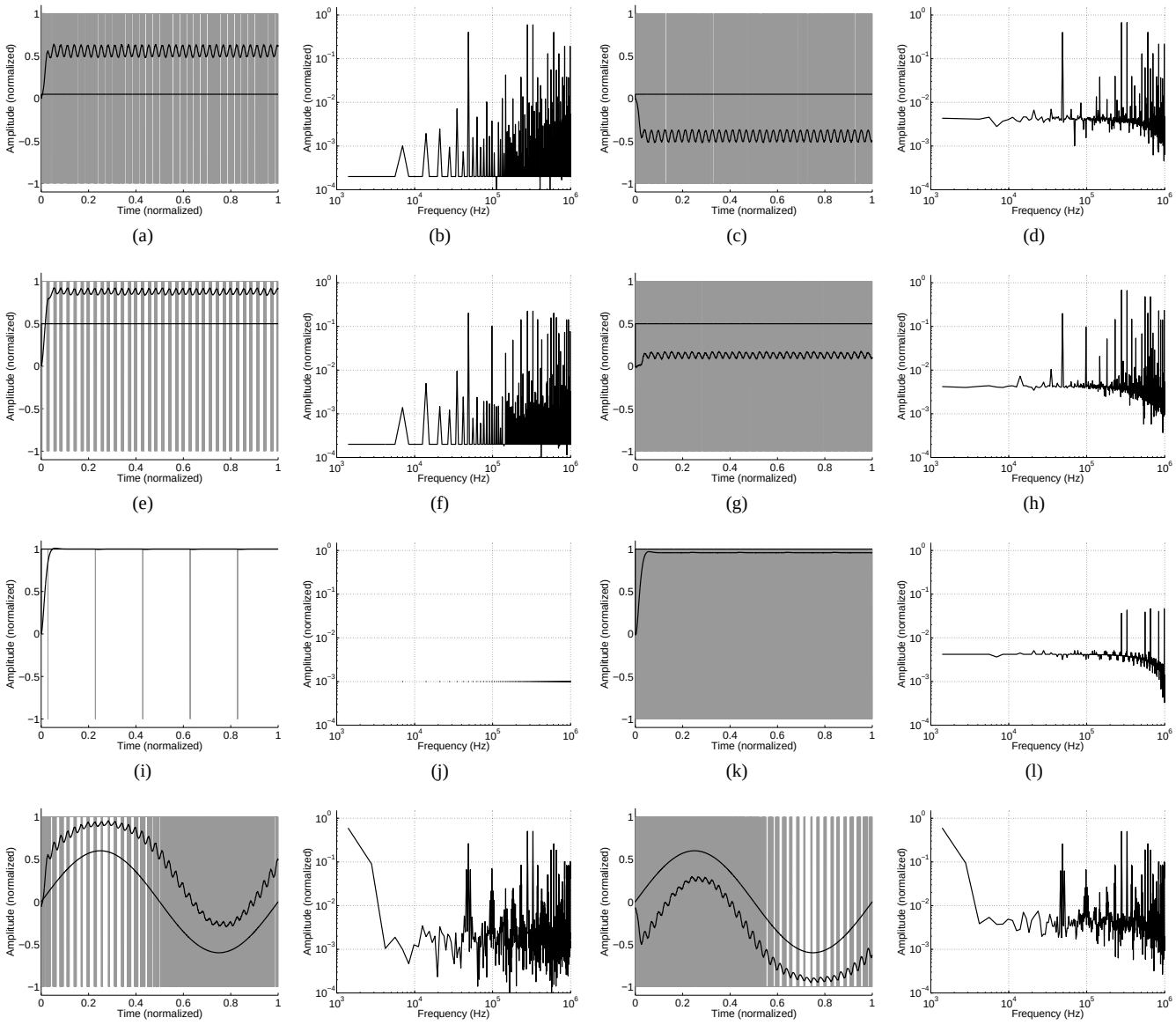


Fig. 6. Signals x, $y_{ORed-MCM}$, $y_{ANDed-MCM}$, $p_{ORed-MCM}$ and $p_{ANDed-MCM}$ as well as spectra of a ORed-MCM $p_{ORed-MCM}$ (left) and ANDed-MCM $p_{ANDed-MCM}$ (right) with varying input signals ($x = 0.05$, $x = 0.5$, $x = 1$ and $x = 0.6\ \sin(2\pi t)$ from top to bottom).

III. Simulation Results

Section II explained the static and dynamic operation of the described MCMs as well as there advantages for EMC. This section will put numbers as results from simulations to them, where all plots are directly comparable to figure 2. The models are based on the equations from section II. The simulation signals with $x = 0.05$, $x = 0.5$, $x = 1$ and $x = 0.6\ \sin(2\pi t)$ were taken on both edges of the input range to show the behavior in case of very small and excessive high inputs as well as in the middle. The center of the input range is commonly used as steady state operating point under nominal conditions. The dynamic behavior of the modulators was verified with the sinusoidal input to verify the usage also for DC-AC converters, motor drives and switch-mode amplifiers. The additional ripple in figure 6 in time domain represents the intermodulation frequencies. The figures 6i and 6k verify the above described limited modulation to $75\ \%$ in case of ORed- and ANDed-MCM. The second order distortion is less than $10\ \mathrm{dB}$ below the fundamental as can be seen in 6n and 6p respectively. The reduction of the EMC peaks to the right of the spectral plots compared to those of a PWM is $50\ \%$.

The results of the ORANDed simulation model (figure 7, left two columns) proof the removal of the DC offset by alternation between ORed- and ANDed MCM while keeping the advantage in EMC. Also the removal of even order distortion is visible and the suppression of the odd order distortion is higher than $10\ \mathrm{dB}$. For unclipped usage of the full input swing, the gain factor of the modulator must result in a lower input signal. The condition with

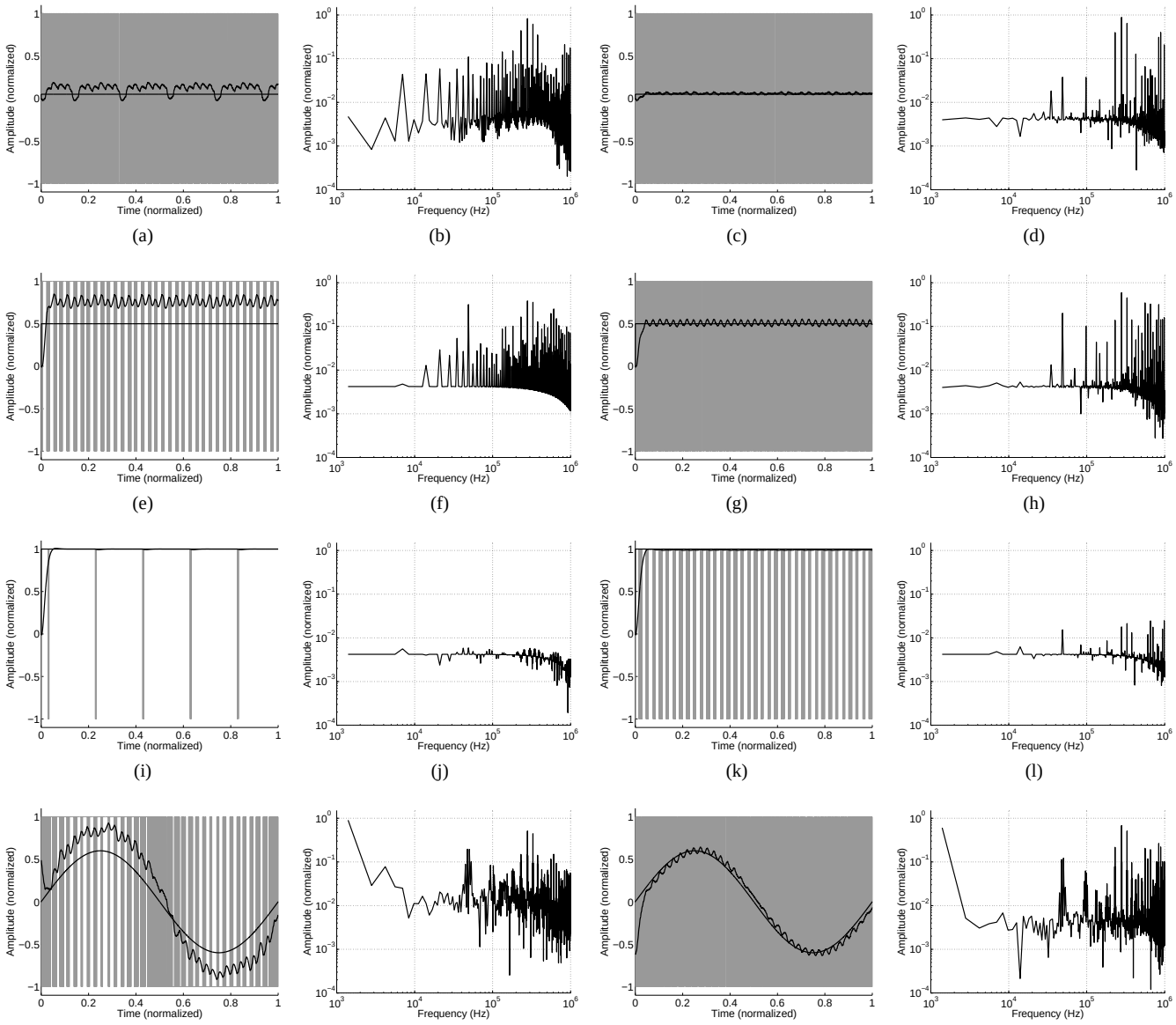


Fig. 7. Signals x, $y_{ORANDed-MCM}$, y_{MS-MCM}, $p_{ORANDed-MCM}$ and p_{MS-MCM} as well as spectra of an ORANDed-MCM $p_{ORANDed-MCM}$ (left) and a MS-MCM p_{MS-MCM} (right) with varying input signals ($x = 0.05$, $x = 0.5$, $x = 1$ and $x = 0.6\ \sin(2\pi t)$ from top to bottom).

full input signal therefore represents an over modulated system in case of the ORANDed model. A MS-MCM has insignificant higher EMC peaks than the modulators shown before. As can be seen from figure 7 (right two columns) the gain is unity as in PWM, the DC offset is zero, also as in PWM and all EMC peaks but the intermodulation components stay below the spectrum representing PWM. Especially at full modulation the MS-MCM provides the highest difference between PWM and MS-MCM.

In practice in all MCM a negligible time delay (resulting from the propagation delay of the logic gates) is expected. As this delay is practically no longer than $t_{pd} = 9$ ns in modern logic circuits. ORANDed and MS-MCM have three of them in series resulting in a total delay of $t_d = 27$ ns. This would result in stability issues of the closed loop at a frequency $f_o = 1/t_d \approx 37$ MHz. This is at least twenty orders higher than practical switching frequencies with existing power semiconductors and magnetic components. Therefore the switching frequency is the first limitation in terms of closed loop stability and the contribution of the time delay of the logic gates is in the noise.

IV. Experiment

The MS-MCM with two clocks was applied to a voltage fed push-pull converter. For further reading on this type of converter please refer to [9], [10] or [11]. A push-pull power stage expects two alternating rectangular signals, where in voltage fed types at no time both of them are allowed to be high. A further logic signal forming was done to the pulse stream p_{MS-MCM} therefore. Dependent on

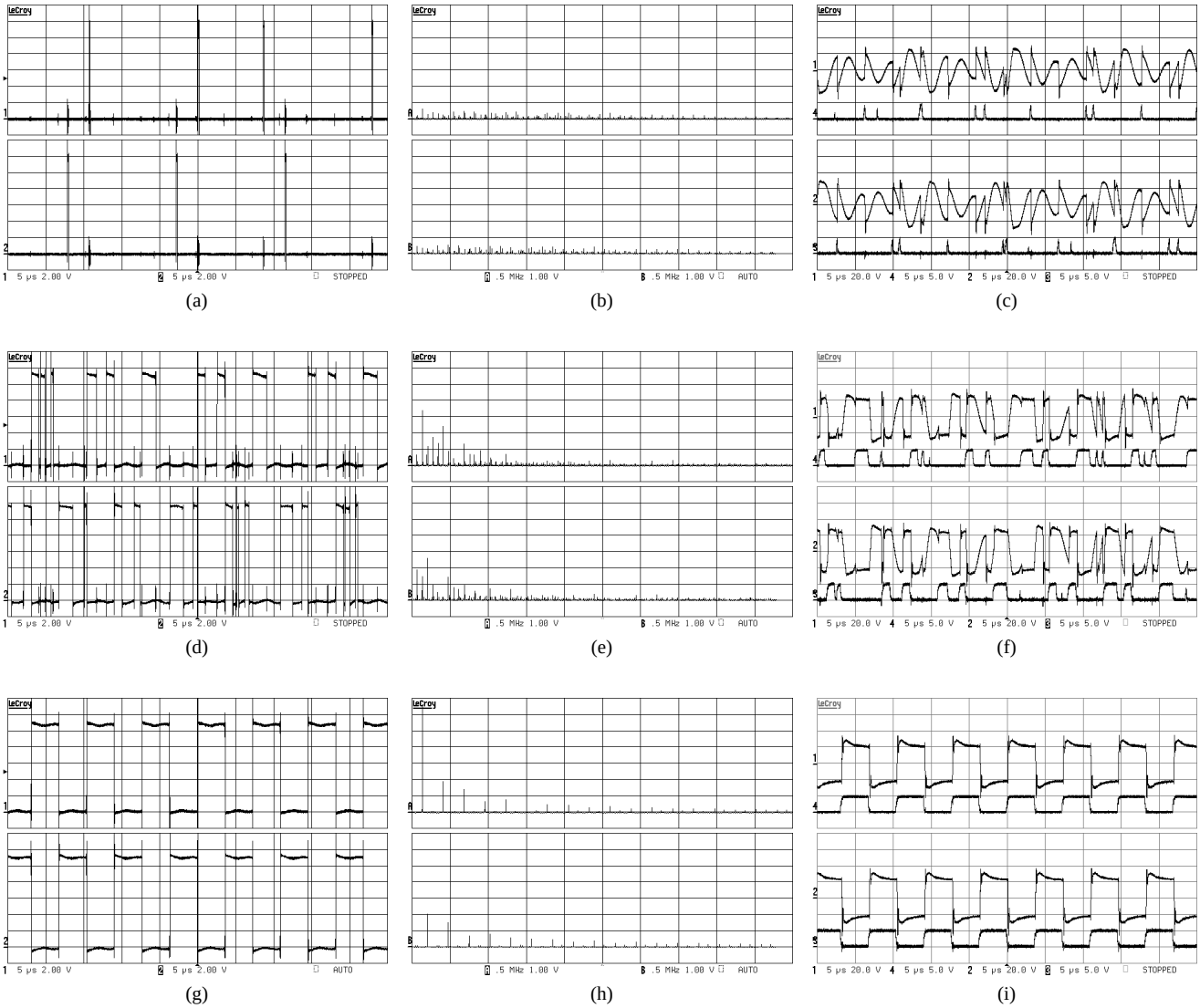


Fig. 8. Waveforms and spectra of the prototyped push-pull converter utilizing MS-MCM: 8a, 8d and 8g show the gate drive signal after the gate driver (5 µs / div, 2 V / div) and 8b, 8e and 8h the according spectra (500 kHz / div, 1 V / div). 8c, 8f and 8i show the unloaded secondary side of the transformer (first and third waveform from top, 5 µs / div, 20 V / div) and the input to the gate driver (second and fourth waveform from top, 5 µs / div, 5 V / div.)

the MCLK state p_{MS-MCM} was commuted to one or the other of the gate drivers for the MOSFET switches.

Nominal input voltage was defined to be 12 V and a transformer with turn ration $1:1:2:2$ was used to obtain two output voltages of $+24$ V and -24 V. Both clocks were derived from a crystal oscillator (7.68 MHz) by clock division circuitries. One was divided by a factor of 28 down to $f_{c_1} \approx 275$ kHz, which was also used as MCLK and the other one was divided by a factor of 22 down to $f_{c_2} \approx 350$ kHz. Both clocks were integrated to triangles giving the carriers c_1 and c_2. The input x was applied from laboratory instruments. To capture the MS-MCM signals on the push-pull converter without regulation influences the loop was not closed for taking the measurements as shown in figure 8. The sum of the two waveforms in each measurement in the left column is a MS-MCM output p_{MS-MCM}. For the push-pull converter it got separated into two signals. At low modulation indices, pulses occur in a not repeating manner as can be seen from the second and third pulse of the upper signal in 8a. The spectrum is close to a spectrum of repeating Dirac pulses, but here both carrier frequencies occur. The transformer only gets magnetized for short periods of time and freewheels between the pulses. With increasing modulation index MS-MCM occurs in form of two pulses in one switching period of one MOSFET, where the average over time is the same as in PWM. The spectrum shows the two carrier frequencies now clearer. The transformer freewheels again between the two pulses. At full modulations the MCLK takes precedence and overdrives MS-MCM, resulting in two 50 % duty cycle pulses which are out of phase. The transformer is getting magnetized all the time, but in alternating directions. Figure 9 shows a picture of the prototype.

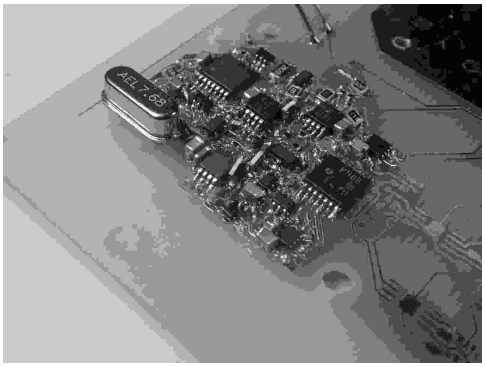


Fig. 9. Photograph of the prototype

MCM-type	Advantages	Disadvantages
ORed and ANDed	lowest EMC lowest complexity lowest cost	offset even order distortion limited dynamical range
ORANDed	low EMC no offset full modulation gain	odd order distortion
MS	low EMC no offset full modulation	highest complexity

TABLE II
OVERVIEW OF THE ATTRIBUTES OF THE FOUR NOVEL MODULATORS

V. SUMMARY AND CONCLUSION

After describing PWM as a reference point, a new family of modulators for switch-mode power supplies was introduced. The common attribute to all of them is, that they use more than one carrier frequency to lower EMC peaks. The functionality of the four members of this family was described with nonlinear algebra combined with Boolean algebra. The principle of all modulators was shown in block diagrams. The describing algebra was used to create models of all four modulators and simulation results in dependency of modulation index were shown. Within this environment special attention was given to the DC functionality to ensure stable and correct bias point operation and AC behavior to validate the dynamic responses. One of the modulators was implemented in a push-pull supply, which was described and measurements on its signals were shown.

The four novel modulators, ORed-MCM, ANDed-MCM, ORANDed-MCM and MS-MCM, principally can be applied to any kind of converter. However they have individual properties as shown in table II, which makes one of them more suitable for one application and another one for a different kind of application. ORed- and ANDed-MCM is therefore best applicable in high volume, highly sensitive and low performance DC-DC converters with regulation and high EMC demands. It can also be used for DC-AC converters where distortion is of no interest. ORANDed-MCM is preferable used in DC-DC converters with tight regulation and EMC requirements and lower demands in dynamic performance or in DC-AC converters with regulation for medium requirements on distortion. In switch-mode amplifiers or DC-DC converters with very precise load and line regulation demands it is best to use MS-MCM.

ACKNOWLEDGMENT

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B.3 Comparison of three different Modulators for Power Converters with Respect to EMI Optimization

ISIE, 2008, Cambridge, England, linked to all chapters

Comparison of three different Modulators for Power Converters with Respect to EMI Optimization

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***Abstract*—Switch-mode Power Converters are well known for emissions in the band of electromagnetic interference (EMI) interest. The spectrum shape depends on the type of modulator and its purpose. This paper gives design guidelines to choose the optimum topology depending on requirements of different applications. Spectral measurements on prototypes of a pulse width modulator (PWM), a $\Delta\Sigma$-modulator and a hysteretic self-oscillating modulator are shown, which are verifying their simulations, with respect to different EMI challenges.**

I. Introduction

Modulators for power converters transfer a reference signal into a switching signal with a discrete number of levels, which is in many cases high and low only. By doing this conversion, the modulator is adding much energy above the frequency of the reference signal. This energy is distributed over a wide range of frequencies, which are measured in EMI tests. The standards for EMI (i.e. [1]) give especially low limits in the sensitivity bands of receivers of broadcasting technologies, such as AM radio, terrestrial TV and FM radio. Due to the high required dynamical range and - depending on the location - weak signal strengths, these limits are very low.

One of the most interesting scenarios are therefore applications, where the switch-mode power converter is very close to the receiver and the coupling path from the converter – as an EMI source – to the receiver – as an EMI sink – is very low ohmic. Both of those conditions are fulfilled in cars: the separation of the source and the sink is only a few meters, resulting in enhanced radiated coupling. Common supply lines, electrical communication lines as well as the chassis give good conduction conditions. Additionally it is a primary design goal for the receivers to reach very low sensitivity levels, because the antenna can not be set up in an optimized way and kept there as in consumer applications due to the movement of the vehicle.

There are two different worst case situations for tuners: one is the seek mode and the other one is a low input signal. In the seek mode, tuners are sweeping the sensitivity window as fast as possible through their input band and try to detect a carrier of a broadcasting station. If there is any single frequency component emitted from a power converter, the tuner is likely to lock into this frequency but unfortunately the side bands are not the program material from a radio or TV station, but the sidebands of the distortion signal. In the second case, the tuner has already locked to a station, but has only weak signal. If the broadband noise from a power converter is overdriving the sidebands of this carrier, the broadcasted program material is again lost and the noise of the converter in this band is displayed on the screen or played through the audio system. Actual receiver input characteristics, frequency bands and their related noise levels have been described in [2] and [3]

An interesting application, which by itself have an EMI source as well as an EMI sink, as described above, close to each other are automotive audio amplifiers. Many of those either comprehend a switch-mode power supply or the amplifier itself is a Class-D type or both of those are combined. In case of audio amplifiers another frequency band is of high interest: the audio band from 20 Hz to 20 kHz. The performance measurements in this band are given by [4], where the according measurements results are highly competitive.

Other applications in many consumer, industrial or automotive products like DC/DC-converters, motor drives or switch-mode power amplifiers deal with the same EMI sinks. The comparison shown in this paper is applicable to those without change. Figure 1 shows a typical block diagram of a Class-D amplifier, including an error amplifier, a modulator, level shifter and gate driver, a power stage and a fourth order output filter.

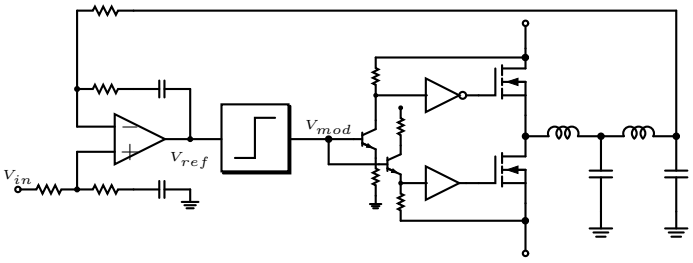


Fig. 1. Block diagram of a typical realization of a switch-mode power amplifier

In many realizations a fourth order output filter and shielding is required to fulfill the EMI requirements. The fourth

order filter significantly decreases the performance in the audio band, adds cost, board space and weight to the application. The shields to return the stray fields of the modulator, power stage and inductors usually cause a trade-off between thermal optimized mechanical design and EMI. Some of the electromagnetic fields can be annihilated by parasitic cancellation in the filter components. These techniques have been described in [5], [6], [7] and [8].
A practical approach to change the high frequency energy distribution is called randomized PWM and EMI investigations on DC-DC converters for automotive use are shown in [9]. These technologies are not considered here because they are known to introduce the randomized noise also in the audio band and therefore significantly decrease the performance.
A typical EMI measurement result on a converter according to the block diagram in figure 1 and optimized component selection and layout is shown in figure 2. The measurement is the worst case measurement within a series of differential and common mode EMI measurements in various distances between the current probe and the output of the converter. The measurements where done in accordance to the current method in [1] as well as to the specification of one car manufacturer. The car manufacturers limits are more stringent in the receiver bands and mandatory to fulfill in the original equipment manufacturer market (OEM). Similar measurements aligned with the voltage method described in CISPR25 [1] are shown in [10].

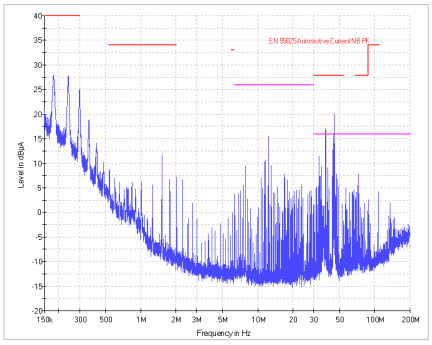


Fig. 2. Common Mode EMI measurement (current probe method) on the output lines of an automotive audio power amplifier

While many design approaches concentrate on the removal of the EMI noise, this paper will concentrate on the modulators, which are adding the high frequency energy to the system. It first explains the three different modulator topologies in section II. Simulation results with respect to the out-of-band behavior based on functional description models of these modulators are shown in section III. As an experiment prototypes of the modulators have been built and the spectra where measured which are shown in section IV. Section V compares the spectra of the modulators and different modulation indices in perspective to the relevant criteria for optimized broadcasting service reception and section VI concludes the behavior of an optimized modulator for all relevant tuner scenarios.

II. Modulator Topologies

Following is a description of the functionality of a PWM, a $\Delta\Sigma$ modulator and a hysteretic self-oscillating modulator. Common requirement to all modulators is the capability of accepting an audio frequency input signal and modulate it into a discrete level output signal while maintaining the input signal. The modulators must not add energy within the audio frequency range and the switching frequencies at the output are supposed to be configurable to a range between 200 kHz and 800 kHz. This is assumed to be a frequency range where the power stages consisting of MOSFETs and the output filters can operate in an efficiency optimized region.

A. Pulse Width Modulator

Figure 3 shows the block diagram of a PWM. It consists of an oscillator, an integrator and a comparator. The oscillator needs to generate a square wave clock, which is integrated to a triangle or a sawtooth. This signal is compared to a reference signal which is the output of the differential error amplifier in figure 1. Depending on which of these two signals is higher, the output of the comparator is either high or low.

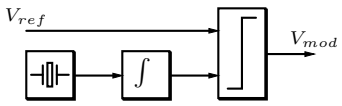


Fig. 3. Block diagram of a PWM

The reference signal determines between natural PWM (continuous time input signal) and uniform PWM (discrete time input signal). Two levels at the output are described in the literature [11] as AD modulation, while three output level signals are described as BD modulation. A triangle as carrier input to the comparator results in a double side PWM, while a sawtooth creates a single side PWM. For simulation and experiment a natural sampled AD two side modulated PWM (NADD PWM) is used.
The decomposition of an NADD PWM output signal into its spectral components by a double Fourier series (DFS) as described in [12] gives an expectation of the PWM spectrum as shown in equation 1

$$PWM(t) = k + \frac{M}{2}\cos(\omega_{ref}t) + \sum_{m=1}^{\infty}\frac{\sin(m\omega_{clk}t)}{m\pi} - \sum_{m=1}^{\infty}\frac{J_0(m\pi M)}{m\pi}\sin(m\omega_{clk}t - 2m\pi k) - \sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\sin(m\omega_{clk}t + n\omega_{ref}t - 2m\pi k - \frac{n\pi}{2}) \quad (1)$$

where k is the offset of the signal, M is the modulation index, ω_{ref} the radian frequency of the sinusoidal reference signal,

J_n the n-th order Bessel function of the first kind and ω_{clk} the radian frequency of the carrier signal and m and n are integer numbers.

B. Delta-Sigma Modulator

The $\Delta\Sigma$ modulator block diagram is shown in figure 4. The Δ-stage subtracts the output from the reference, which is again the output of the differential error amplifier as shown in figure 1, the Σ-stage is an integrator summing up the difference signal and feeding a comparator. This comparator is changing its output in dependency of the integrator signal being higher or lower as a constant reference. A latch, i.e. a D-type flip-flop, is transferring the comparator output pulses triggered by a rectangular clock signal derived from an oscillator. The oscillator frequency with a $50\ \%$ duty cycle is adjusting the main switching frequency. The main switching frequency is expected to be half of the clock frequency, when using a positive edge triggered flip-flop.

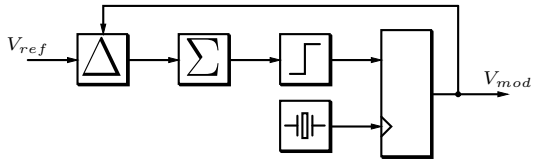


Fig. 4. Block diagram of a $\Delta\Sigma$ modulator

C. Hysteretic Self-Oscillating Modulator

The hysteretic self-oscillating modulator is described in [13]. Compared to the PWM and $\Delta\Sigma$ it does not require an external clock but deriving its switching frequency by operating at the stability boundary. The reference signal from the error amplifier is summed and integrated together with the output signal and fed into a hysteretic comparator. A block diagram is shown in figure 5.

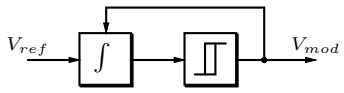


Fig. 5. Block diagram of an hysteretic self-oscillating modulator

The switching frequency of a hysteretic self-oscillating modulator is determined by M, the time constant of the integrator τ_{int}, the hysteretic window H and the propagation delay of the forward path τ_{pd} as shown in equation 2.

$$\omega_{sw} = \frac{1 - M^2}{8\pi(\tau_{int}H + \tau_{pd})} \tag{2}$$

III. Simulation

The simulation of the described modulators was carried out in the time domain with linearized blocks, followed by a Fourier transformation calculated by MATLAB. The switch-mode elements where modeled as discrete two level outputs and no edges where taken into account. Within the considered frequency range, this is a valid assumption. For optimal comparison of the three modulators, the clock frequency was set to the same frequency $f_{clk} = 270\ \mathrm{kHz}$. The supply voltage was $5\ \mathrm{V}$ for ideal comparison with the measurements in the experiment shown in section IV.

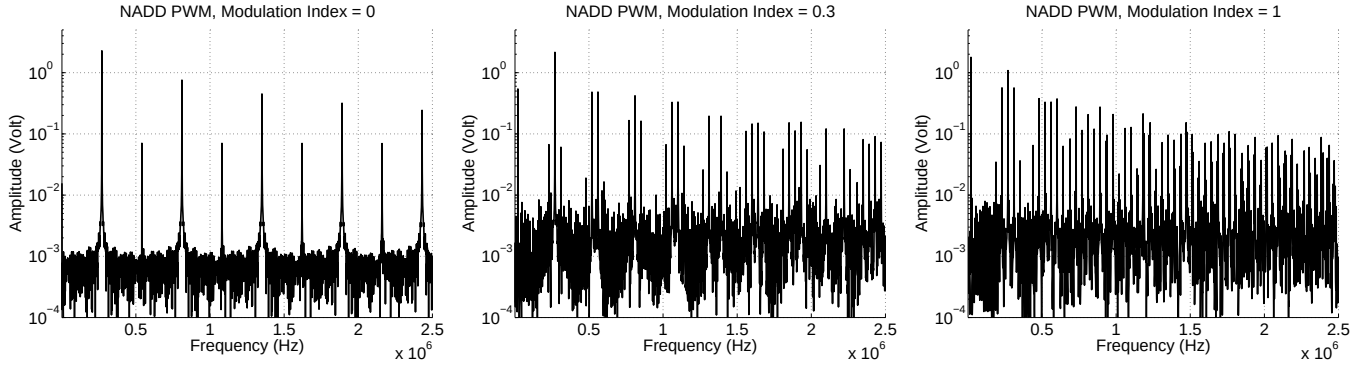
Figure 6(a) shows the simulated spectrum of an NADD PWM with the modulation indices $M = 0$, $M = 0.3$ and $M = 1$. As expected from equation 1 side bands with distance f_{ref} are growing around the switching frequency f_{clk} with increasing modulation. The spectral components are situated at discrete frequencies, which reflects the repetitive nature of a PWM bit stream in time domain. The noise level of the simulation is limited to the timing precision of the simulation which was chosen to a compromise between simulation time and resolution in the results.

The comparable results for a $\Delta\Sigma$ modulator are shown in figure 6(b). The decision points of a $\Delta\Sigma$ modulator are based on the input signal as well as on the noise fed back from the output. This noise is modeled as white noise [14]. This noise is uncorrelated and therefore the bit stream pattern of a $\Delta\Sigma$ modulator is non repetitive in time domain which results in a continuous spectrum shape. As the basic shape in time domain at $M = 0$ is close to a rectangular waveform with $50\ \%$ duty cycle and the height of these pulses is - as in the PWM - limited by the supply voltage of the output stage. Therefore the peaks stay at the same level, and the side bands are filled with energy, while the inherent noise shaping nature of the modulator removes noise between the harmonics. At higher modulation indices the minima in the spectrum remain but the side bands are continuously filled with energy. The overall energy in the out-of-band noise of a $\Delta\Sigma$ modulator is therefore higher than the noise of a PWM.

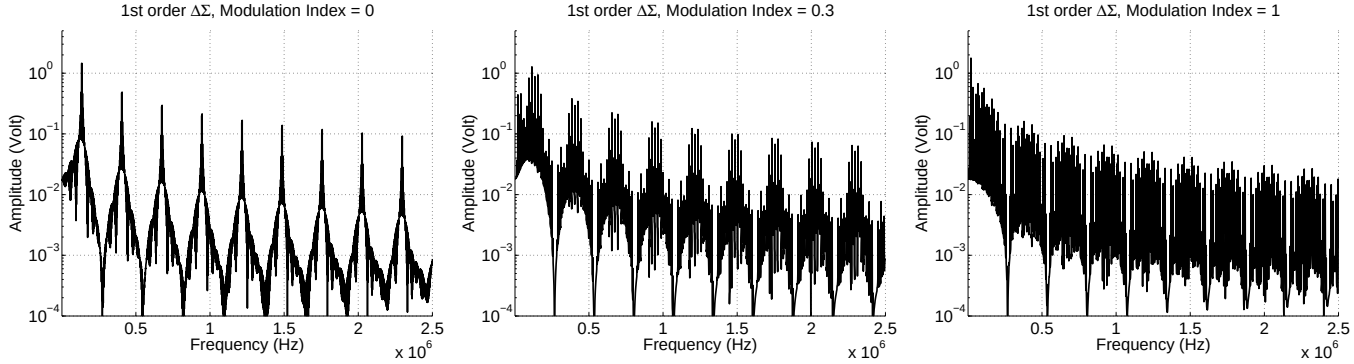
The simulation results of a hysteretic self oscillating modulator is shown in figure 6(c). In case of $M = 0$, no source is applied to the modulator and no quantization noise is added. The peaks in the spectrum are equivalent to a stable rectangular signal with $50\ \%$ duty cycle - as in the PWM case - while the spectral resolution is limited to the Fourier transformation. With increasing modulation index sidebands around the carrier occur and the inherent feedback shows a portion of the same noise shaping effect as seen by the $\Delta\Sigma$ modulator. A full level input signal shifts the switching frequency towards the input frequency and creates harmonics based on the new fundamental.

IV. Experiment

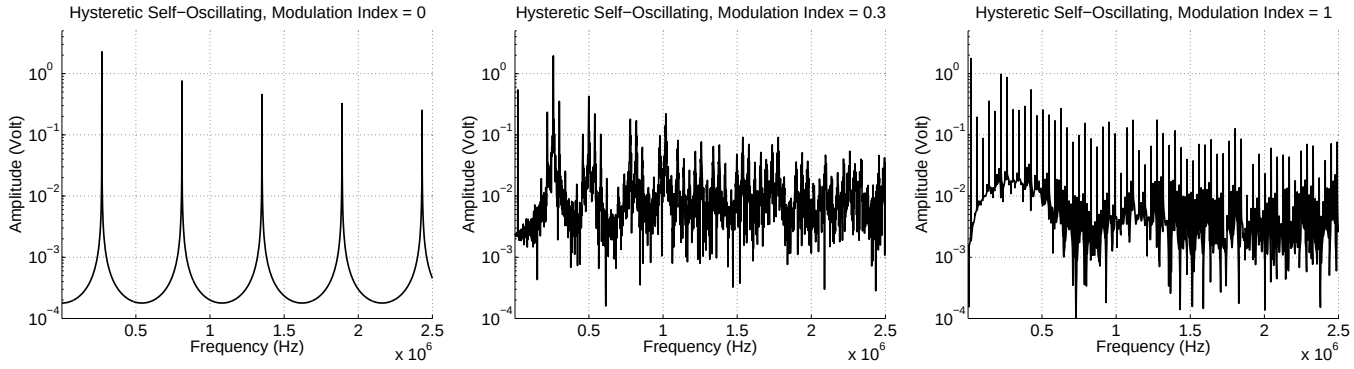
This section will take the simulation in perspective to measurements on prototypes of the modulators as shown in figure 7. All measurements where taken with a Rohde & Schwarz ESI17 EMI test receiver in spectrum analyzer mode. The measurement bandwidth was $500\ \mathrm{Hz}$, number of taken points was 500. The clocks and the reference signals were fed into the modulators from function generators. The outputs of the modulators where actively divided by $40\ \mathrm{dB}$ because the modulator outputs where not designed to drive the $50\ \Omega$ inputs of the analyzer. For best comparison with simulation the results were plotted, after recovering the $40\ \mathrm{dB}$ correction factor, with MATLAB. During the measurements



(a) NADD PWM



(b) $\Delta\Sigma$ modulator



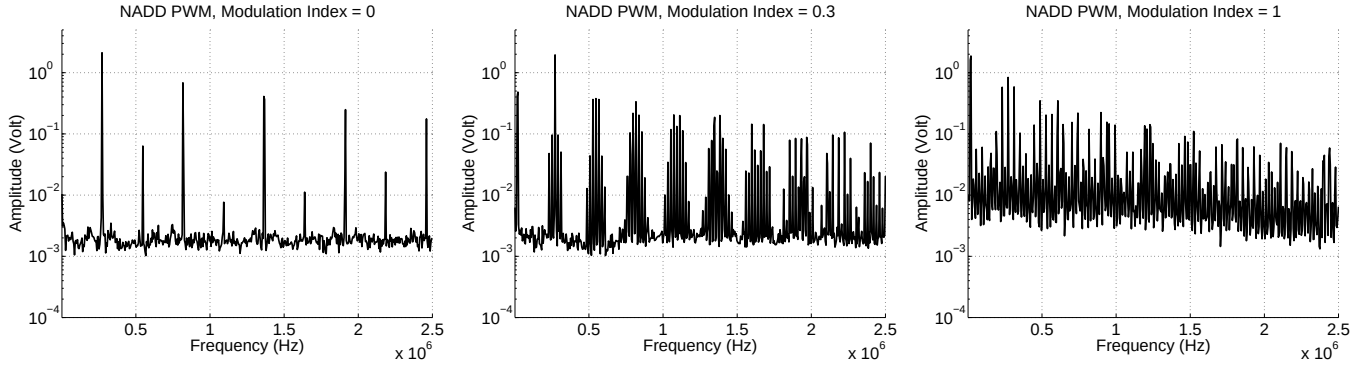
(c) Hysteretic Self-Oscillating

Fig. 6. Simulated spectra

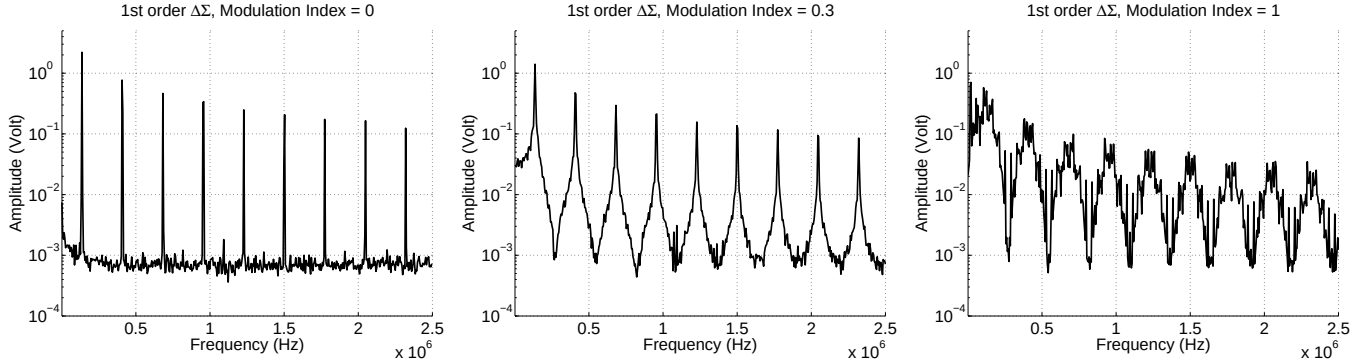
the rectangular signals as well as all inputs were supervised in time domain with an oscilloscope.

Figure 8(a) shows the measurement results on the PWM. As predicted by simulation, the spectrum contains discrete components only. The even harmonics at $M = 0$ are an artifact of the imperfect symmetry of the triangular carrier. The measurements show the discrete side bands rising with increased modulation. The peak height is well aligned with the simulation results.

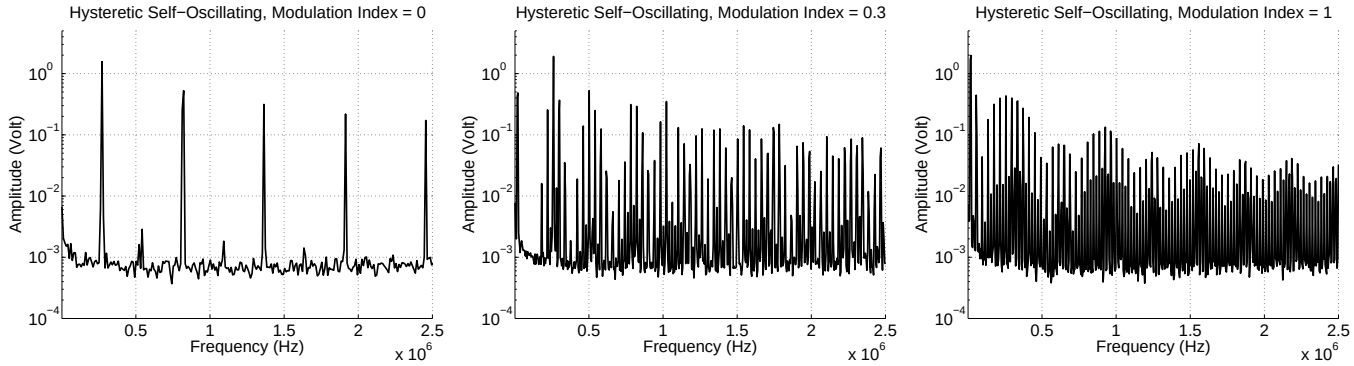
The same measurements have been carried out on the $\Delta\Sigma$ modulator prototype. Results are shown in figure 8(b). For $M = 0$ the spectral minima are masked by the noise level of the spectrum analyzer. This is a result of an trade-off between measurement time and accuracy. For longer measurement times and smaller measurement bandwidth the noise level of the analyzer can be significantly decreased. For higher modulation the noise level of the modulator is raised as predicted by simulation and the dips of the modulator dominate the noise level of the measurement system. The non-repetitive nature of a $\Delta\Sigma$ bit stream in time domain clearly results in a continuous spectrum. A full level modulation shows a dramatic increase in overall high frequency energy. The local minima in the spectrum stay consistent and have the width of twice the reference signals frequency f_{ref}. The increased noise reaches the audio band. An additional noise shaping is required to preserve the in-band performance. The $\Delta\Sigma$ modulator is likely



(a) NADD PWM



(b) $\Delta\Sigma$ modulator



(c) Hysteretic Self Oscillating

Fig. 8. Measured spectra

to run into stability problems at high modulation indices as researched in [15] and more recently in [16]. Practically the modulation indices in these systems therefore are limited.

The hysteretic self-oscillating modulator was tested in the same measurement setup as the above shown and results are shown in figure 8(c). Without any input signal the hysteretic self-oscillating modulator produces very perfect rectangular waveform with $50\ \%$ duty cycle, independent of any external signal sources. Therefore the even harmonics of the switching frequency at zero modulation $f_{ref}|_{M=0}$ are close to zero. Remaining imperfections only belong to the nonlinearity of the modulator components. With increasing modulation the switching frequency drops (in figure 8(c) from 273 kHz to 248 kHz). More discrete side bands occur than in the PWM case. For full modulation the decision points are forced by the input signal and the fundamental of the switching frequency $f_{sw}|_{M=1}$ drops to the input frequency $f_{ref} = 20$ kHz. Equation 2 does not take the forced commutation into account.

V. Comparison of Results

The shown simulated and measured spectra will be taken into perspective to receivers input sensitivity scenarios as explained in section I here. The main interesting parameters are the local maxima (peaks, table I), local minima (dips, table II) of the spectrum, the side bands around the carrier (table III) and the noise performance in the audio band (table IV). The height of the peaks is directly related to the probability of

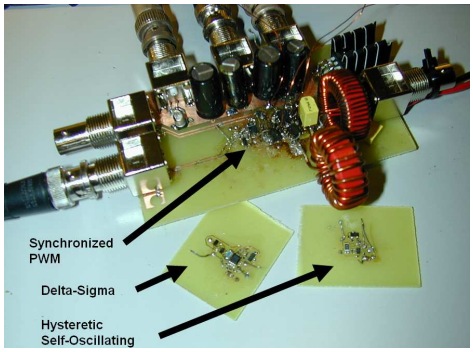


Fig. 7. Picture of Prototypes

a receiver locking accidentally into it and considering the peak as carrier of a broadcasting station. The dips allow receivers to detect very low signals because the minimum signal strength of the program material can be just slight above the dips. The side bands around the carrier act directly opposed to that and might overdrive program material of a station. The noise performance in the audio band does not disturb the receivers but is directly transferring audible noise through the power stage to the speaker. Again the program material, even if coming from a recorded source might be hidden below this noise level.
The rules for comparison and conclusions result in preferably

- low maxima (peaks),
- wide and low minima (dips),
- narrow, predictable and low side bands and
- low and frequency independent noise in the audio band.

PEAKS	PWM	$\Delta\Sigma$	HSO
$M = 0$	$n \cdot f_{clk}$	$\frac{2 \cdot n}{2} f_{clk}$	$n \cdot f_{sw}\|_{M=0}$
$M = 0.3$	$n \cdot f_{clk}$ & $n \cdot f_{clk} \pm m \cdot f_{ref}$	$\frac{2 \cdot n}{2} f_{clk}$ & $\frac{2 \cdot n}{2} f_{clk} \pm m \cdot f_{ref}$	$n \cdot f_{sw}\|_{M=0}$ & $n \cdot f_{sw}\|_{M=0} \pm m \cdot f_{ref}$
$M = 1$	$n \cdot f_{clk}$ & $n \cdot f_{clk} \pm m \cdot f_{ref}$	spread at $\frac{2 \cdot n}{2} f_{clk} \pm m \cdot f_{ref}$	$m \cdot f_{ref}$

TABLE I
COMPARISON OF LOCAL MAXIMA IN THE DIFFERENT MODULATORS

Common to all three modulators is that the peaks are decreasing with increasing modulation index.

DIPS	PWM	$\Delta\Sigma$	HSO
$M = 0$	practically limited to the noise floor by the dynamical range of the sytem	$n \cdot f_{clk}$	practically limited to the noise floor by the dynamical range of the system
$M = 0.3$		$n \cdot f_{clk}$	
$M = 1$		$n \cdot f_{clk} \pm f_{ref}$	

TABLE II
COMPARISON OF LOCAL MINIMA IN THE DIFFERENT MODULATORS

While the noise floor in PWM and hysteretic self-oscillating are system limitations, is the spectrum of a $\Delta\Sigma$ an intrinsically shaped form.

SIDE BANDS	PWM	$\Delta\Sigma$	HSO
$M = 0$	equivalent to the frequency stability of the oscillator	continuous	frequency stability equivalent to an RC-oscillator
$M = 0.3$	discrete, frequency stability dependent on input and on stability of the oscillator		discrete, frequency stability equivalent to an RC-oscillator and dependent on input signal
$M = 1$	discrete, many frequencies due to intermodulation		

TABLE III
COMPARISON OF SIDE BANDS AROUND THE CARRIER AND ITS HARMONICS

ADUIO NOISE	PWM	$\Delta\Sigma$	HSO
$M = 0$	constant	noise shappped	constant
$M = 0.3$			
$M = 1$	side bands may occur in audio band		

TABLE IV
COMPARISON OF AUDIO BAND NOISE

The best behavior for each modulation level is shaded gray in the tables based on the explained comparison rules.
Some related modulator technologies can extend this list, i.e. NBDD modulated PWM, which is removing differential peaks compared to what is shown in the NADD example, a

$\Delta\Sigma$ modulator of second order including intrinsically noise shaping or noise shaped $\Delta\Sigma$ modulators as well as phase shifted self oscillating systems. Two interesting approaches to influence the spectral behavior based on PWM are shown in [17] called predistorted PWM (Pd-PWM) and frequency modulated PWM (FM-PWM).

VI. Conclusion

The relevance of the EMI behavior of modulators has been explained with respect to potential EMI sinks, especially TV and radio receivers. Therefore four relevant parameters (maxima, minima, side bands and base band noise) to weight the performance have been defined. Three different types of modulators (PWM, $\Delta\Sigma$ and hysteretic self-oscillating) have been explained, simulated and verified by measurements on prototypes. The measurements match the simulations. The results have been summarized with respect to the criteria relevant for receivers. The characteristics of an optimal modulator as combination of all advantages has been found.

The PWM and the hysteretic self-oscillating modulator show very similar spectral behavior. In applications where the peak detection of a nearby receiver is the most critical situation, the hysteretic self-oscillating modulator shows slight advantages. If detection of very low signal strength of the broadcasting system is the design priority, PWM is the best modulation topology. $\Delta\Sigma$ offers spectral dips which can be used to detect low signals when a tuner is already locked into the carrier of a broadcasting station. This advantage of a $\Delta\Sigma$ shows best up at high modulation indices where the modulator tends to be instable.

Additionally an outlook to other topologies was given. Depending on the strived design, a modulator can be chosen based on the given parameterization for many applications such as switch-mode power amplifiers and supplies or motor drives.

Acknowledgment

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B.4 Active Electromagnetic Interference Cancellation for Automotive Switch-Mode Audio Power Amplifiers

36th AES Conf., 2009, Detroit, USA, linked to chapter 5

Active Electromagnetic Interference Cancelation for Automotive Switch-Mode Audio Power Amplifiers

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ABSTRACT

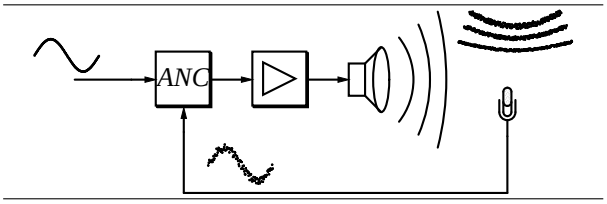
Recent trends in the automotive audio industry have shown the importance of active noise cancelation (ANC) for major improvements in mobile entertainment environments. These approaches target the acoustical noise in the cabin and superimpose an inverse noise signal to cancel disturbances. Electromagnetic interference between switch-mode audio power amplifiers and receivers show the same physical obstacle as the described ANC endeavors are targeting. The principle of active electromagnetic interference cancelation (AEC) is derived in this paper on a theoretical basis with verifications in simulation and experiment. The resulting switch-mode audio power amplifier of this experiment keeps its high efficiency and is able to deliver the signal with less than 0.1 % distortion, while improving the source of electromagnetic interference by 15 dB.

1. INTRODUCTION

The cabin of automobiles is exposed to several audible noise sources from its acoustical tough surroundings like road noise, engine noise, wind noise and other traffic. The topic of active noise cancelation (ANC) [1] [2] is dealing with those disturbances to generate a perfect rolling sound reproduction environment. The principle of ANC is to subtract a feedback or add a feedforward signal from or to the actual desired music – the contents material – to obtain an error signal. This signal is getting processed (as shown in [3]) and increased in an amplifier to drive the speakers mounted in the car. Within the passenger compartment the content material gets superimposed with the external perturbation signals which is acoustical noise. These two overlaid sources are measured by several microphones, who's output is used as feedback or feedforward signal to close the loop. The plant and its regulation for an exemplary feedback ANC as described is visualized in figure 1.

A similar disturbance path is given by the interface of a switch-mode audio power amplifier to the receiver input of a head unit. Instead of the longitudinal acoustical waves, the superposition of signal and noise happens by means of transversal electromagnetic waves. These phenomena are prevented by requirements, written by governments, technical committees and car manufacturers. Any manufacturer of equipment or supplier has to fulfill those requirements for any given product. The most interesting products with respect to these demands are switch-mode audio power amplifiers and switch-mode power supplies. Especially the former ones are in the major scope of this paper because their physical proximity to the media receivers is leading to a worst case situation as described following.

Fig. 1 A feedback active noise cancelation (ANC) system

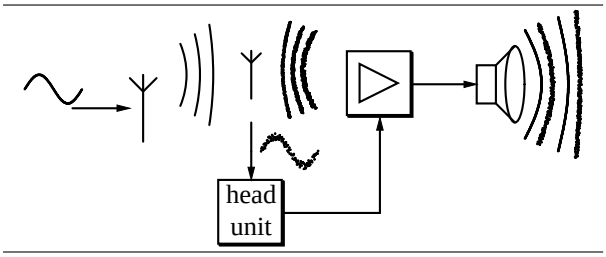


Transmission stations like radio and television stations are sending the modulated material contents in a high frequency band via air. Antennas of mobile receivers – as their counterparts – are taking any signal in the same band which is supposedly the desired transmitted content material, sending it to a head unit where the electronic part of the receiver, which is responsible for preamplifi-

cation and demodulation, is located and through a communication bus, e.g. MOST2, the music contents is driving the loudspeakers through an amplifier. In case this amplifier is a switch-mode audio power amplifier, it can conduct or radiate undesired signals in analogy to the acoustical perturbations in case of ANC. These electromagnetic perturbations cannot be distinguished from the actual desired transmission signal at the receiver side in the head unit, therefore they get demodulated together with the music and also reproduced through the transducers into the audible longitudinal domain of acoustical signals. Figure 2 is a visualized description of this problem.

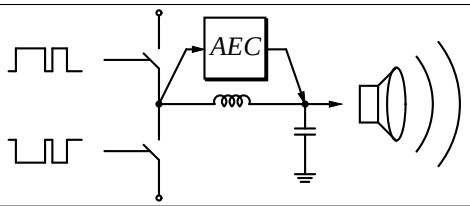
This paper will show an active electromagnetic interference (EMI) cancelation (AEC) system, which is suppressing the undesired transversal waves and the undesired conducted signals at its source. Within the switch-mode audio power amplifier, the highest transients, which are causing the high frequency disturbances, occur in the power stage. Before conducting this amplified signal to the loudspeakers, the signal in state-of-the-art consumer amplifiers pass at least a second order passive filter which in many cases is extended to a fourth order passive filter in automotive entertainment applications. Instead of these two extra filter orders, AEC forms an active parallel path to the existing second order filter to get a maximum of suppression of high frequent noise, before the connection interface of the amplifier to the speaker terminals.

Fig. 2 Block diagram of an applied electromagnetic interference (EMI) problem



Active EMI filters follow a similar approach. They have been designed in various combinations to switch mode power supplies [4] and proven to cancel theoretical sinusoidal waveforms for converters in military and space applications. A successful application to a real converter is shown in [5], which also mentions the difficulty to deal with dynamic behavior of the converters. When active filters of the described types are applied to DC-DC converters, they are mainly intended to cancel the contribution of the switching frequency and its harmonics (ripple) in the steady state of the power supply. In [5] the fact of dynamic behavior of power supplies in case of line and load variations is taken into account and the active filter is on purpose driven into saturation to prevent the active filter from reacting to the converters effort to stabilize by dynamic responses. Once the converter has settled to its steady state, the active filter is in operation again and provides a high level of ripple cancelation.

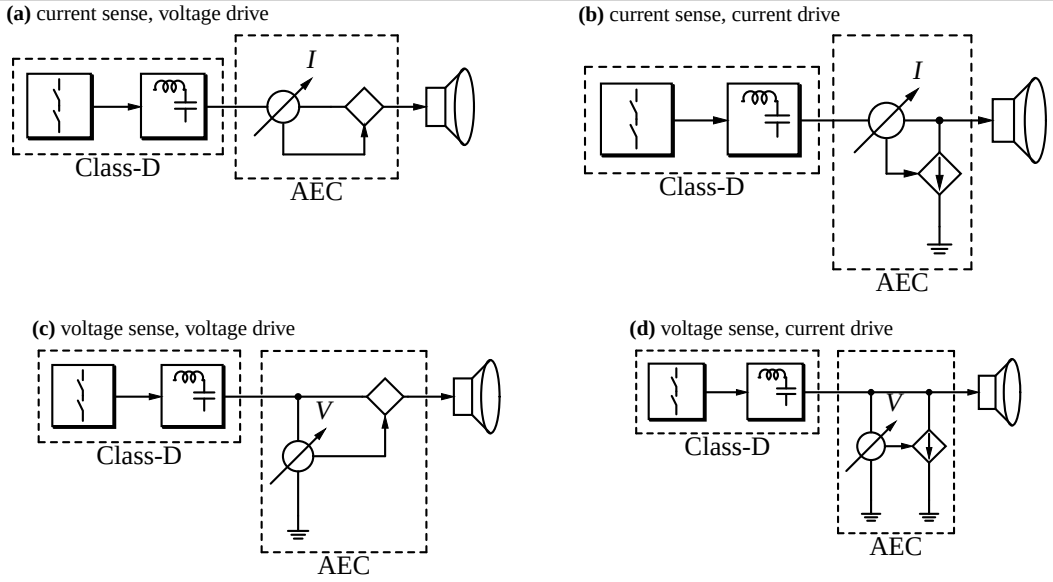
Fig. 3 Block diagram of an active electromagnetic interference cancelation (AEC) system



An application never reaching constant input and output voltages and currents is a power factor correction (PFC) stage. It always follows the frequency of the AC mains (60 Hz or 50 Hz) and active EMI filters need to be carefully designed not to cancel these low frequencies. An example is shown in [6], which therefore involves AC coupling between the ripple sensing and the active filter input as well as between the active filter output and the cancelation point. A wide variety of those possible filter structures is given in [7]. It is explaining possible combinations of current and voltage sensing in combination with current drive and voltage drive for power converters. Applying these principles to switch-mode audio power amplifiers the combinations as shown in figure 4 arise. In any case it is essential to take the highly dynamic contents material of the amplifier into account and prohibit cancelation or amplification of the audio signal through the active filter. A cancelation of the audio signal would decrease the output level, where an amplification would process the audio through the linear filter stage creating high losses there instead of utilizing the high efficiency of the switch-mode audio power amplifier.

These concerns are taken care of in this paper. First a practically suitable topology is chosen and the requirements for the active filter are derived in section 2. The resulting circuit is synthesized in section 3 by means of simulation and verification by experiment in section 4 before resulting in the concluding section 5.

Fig. 4 The four possible combinations of sensing voltages / currents and driving voltages / currents.



2. DERIVATION OF THE ACTIVE FILTER

With the filter structures as shown in figure 4, AC coupling with either of the sense or drive elements is provided by the use of passive components. A serial sense or drive component can be realized by transformers and parallel structures for either use are separated from the high voltage path by capacitors. The used transformers therefore need to stand the stresses of the audio signal current on the primary side, while they only operate in a lower power domain on the active filter side. Respectively the capacitors need to be chosen for the audio voltage.

2.1. Choice of topological Structure for AEC

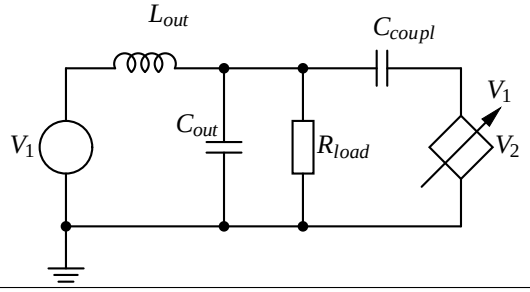
Experience has shown that inductors in the power signal path come with practical disadvantages:

- Inductors have a bigger tolerance in comparison to capacitors. The reason is mainly the tolerance of the core material which can be as high as 10 to 20 %, therefore making it quite unsuitable to sense and drive extremely low and precise signals such as the electromagnetic interference problems represent.
- Inductive components naturally come in round packages. It is possible to buy them with rectangular footprints but the selection of alternative components gets smaller which is resulting into an economical disadvantage. Round footprints are quite unpractical in designs for the automotive audio industry, because amplifiers include nowadays around 20 channels and the board layout gets majorly complicated with round component packages and overall product size limitations. There is intrinsically always somewhere valuable space left out by round components and therefore does not guarantee the highest level of power density.
- Nicely shaped inductors for the described business usually come with one winding only. A coupled inductor with adjustable turn ratios is not available on the market, whereas the scalability of capacitors is quite easy. Self developed inductors are not competitive in price to off-the-shelf inductors.
- In general a foil or ceramic capacitor is somewhat cheaper than an adequate inductor and many times also easier to place on the board with standard manufacturing machines, whereas inductors come with highly varying shapes and weights, which turns them either into hand-placing components, what increases the labor cost on the product or demands special mounting machines, which increase factory cost.

Based on these reasons it is desirable to design an active

EMI cancelation filter without inductive components and stick to resistors and capacitors as circuitry around the active filtering stage only. The prototype of such a circuit structure is shown in figure 5. Voltage source V_1 represents the power stage ("switch node"), L_{out} and C_{out} are the passive filter elements of the only remaining filter stage, R_{load} represents the nominal load for the amplifier, C_{coupl} is an AC-coupling capacitor separating the drive stage form the amplifier output and V_2 is a voltage source controlled from the voltage V_1 on the switch node.

Fig. 5 Filter structure for the active EMI cancelation circuit with V_2 as a voltage source controlled from the voltage on "switch node" V_1.



2.2. Analytical Derivation of AEC

The load voltage for this topology therefore becomes dependent on the voltage on the switch node as well as on the voltage of the controlled voltage source V_2. The resulting transfer function is a linear superposition of the single transfer functions as in 2.1.

Equation 2.1 Transfer function with superposition of the two sources from figure 5 to the voltage across the load.

$$\underline{V}_{out} = \frac{\underline{V}_1 + \underline{s}^2 L_{out} C_{coupl} \underline{V}_2}{1 + \underline{s}\frac{L_{out}}{R_{load}} + \underline{s}^2 L_{out}\left(C_{out} + C_{coupl}\right)}$$

The denominator is similar to a conventional second order low pass filter with the exception that the coupling capacitor adds to the output filter capacitor. The numerator has one degree of freedom, i.e. the controlled voltage source V_2. This can be used as a design criteria for the transfer function from V_1 to V_2 which defines the control of V_2.

It is desired that the voltage across the load V_{out} is zero for all frequencies beyond the filter resonance, i.e. the frequencies specified by equation 2.2.

Equation 2.2 Precondition to cancel EMC relevant signals

$$\underline{V}_{out} = 0 \;\forall\; \underline{s} > \sqrt{L_{out}\left(C_{out} + C_{coupl}\right)}$$

To cancel the voltage on the output node V_{out}, the numerator of equation 2.1 needs to be zero, which gives the specification for setting the voltage on V_2 as shown in equation 2.3.

Equation 2.3 Controlled voltage source V_2 specification.

$$\underline{V}_2 = -\frac{1}{\underline{s}^2 L_{out} C_{coupl}} \underline{V}_1$$

That is a second order inverting integrator from the switch node to the active filters output node.

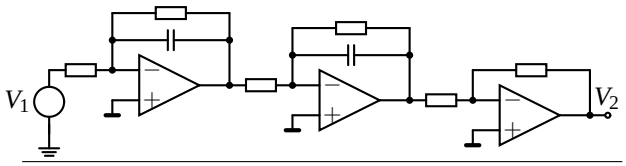
3. SYNTHESIS OF DERIVED FILTER STRUCTURE

3.1. Choice of adequate Filter

The realization of pure integrators to practice is quite difficult, because any infinitesimal small DC offset would be multiplied with the infinite gain of the integrators at 0 Hz and drive the circuit during its operation into saturation. An optimal reference for EMI canceling is therefore limited by a low frequency roll-off. This behavior is emulated for later reference by a circuit as shown in figure 6.

Even this circuit could be designed for a quite good approximation to perfect cancelation, it would still come

Fig. 6 An optimal AEC circuit with respect to EMI cancelation.



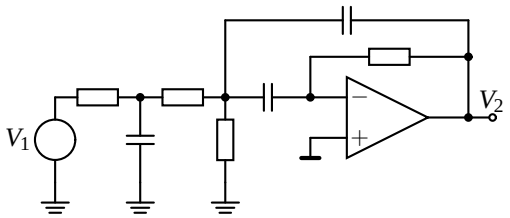
with the major drawback as described above. It could not stand the highly dynamic behavior of the amplifier. It is therefore the major difficulty to keep the contents material away from the active EMI canceling circuit and therefore guarantee operation despite the audio contents. This is leading to the design constraint for the active cancelation filter within the audio band: it is supposed to provide a decent amount of suppression up to 20 kHz. The final resulting specification for an AEC circuit is therefore given by

- adequate suppression in the audio band,
- second order integration above the resonance frequency of the passive second order output filter and
- inversion at frequencies above the resonance for a second order passive output filter.

Practically effectiveness is guaranteed, if the two conditions above the resonance of the output filter are fulfilled at the switching frequency of the switch-mode audio power amplifier and above. Possible realizations as in figure 7 for the desired behavior are extending an active second order bandpass by an additional pole and a second order lowpass by an additional highpass respectively. However none of those two exemplary filters can realize a complex pole pair, which would be required to converge the transfer function of the active filter for high frequencies as close as possible to the ideal second order integrator. It is desirable to develop a filter that comes with a high quality between the resonance frequency of the output filter and the switching frequency. This allows both, the highpass and the second order integrator to provide maximum suppression of the audio signal as well as tight following of the ideal integrator. Such a filter is a Sallen-Key filter equipped with an additional highpass as shown in figure 8 according to [8]. An additional inversion is required in conjunction with this filter because it is a non-inverting circuit.

Fig. 7 Possible AEC realizations with real pole pairs.

(a) active bandpass extended by additional pole



(b) active second order lowpass extended by additional highpass

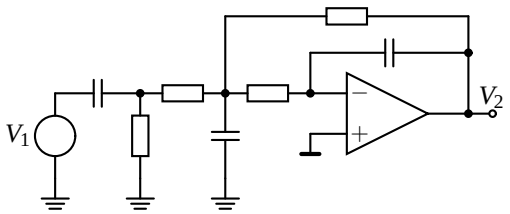
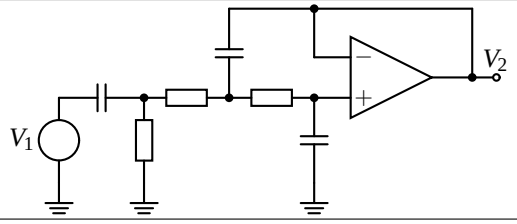


Fig. 8 A Sallen-Key lowpass with an additional passive high pass.



3.2. Revision of Analysis by Simulation

There are three different types of active filters from section 2 to choose for realization:

- the ideal analytical solution: second order integrator
- bandpass with real poles
- bandpass with complex poles

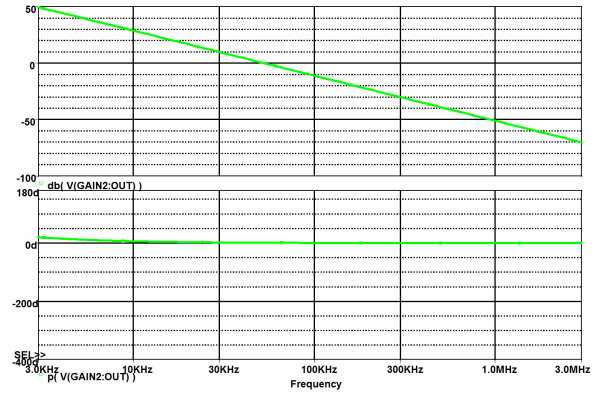
Even the ideal solution was excluded above, because it fails to provide suppression of the contents material, it will be included in simulation for reference. The other two solutions will be compared to match this ideal solution in the following paragraphs.

3.2.1. Ideal Filter: Second order Integrator

For reference two cascaded leaky integrators and an inverter as shown in figure 6 proof the described concept. The transfer function of the simulated filter is shown in figure 9. It is remarkable that the phase is not constant because the leakage of the integrators moves both poles above 0 Hz.

The same circuit got applied to a square wave signal which represents the switch node V_1 in a transient simulation. The output of the filter is replacing the controlled

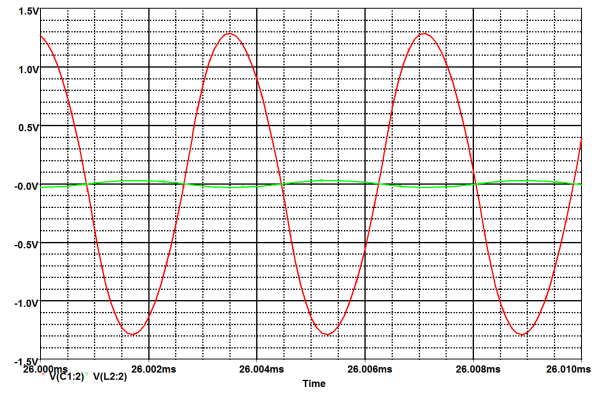
Fig. 9 Transfer function (magnitude and phase) of leaky integrators and inverter.



source V_2 as shown in figure 5. The results are compared with the same filter without active cancelation. For fair comparison, the coupling capacitor between the active filter and the output node of the amplifier was used as addition to the output capacitor of the passive filter.

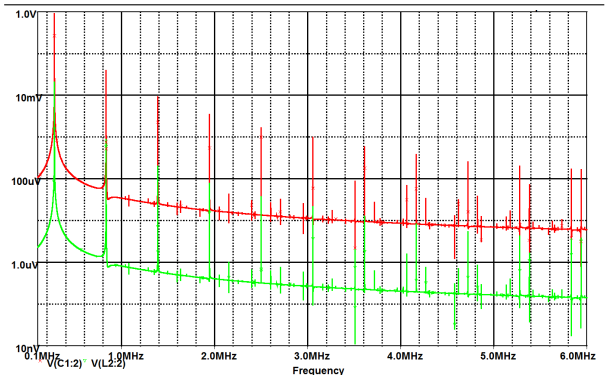
For qualitative relation of the improvement figure 11

Fig. 10 The red waveform (high amplitude) represents the parabolic ripple waveform of a second order filter and the green (lower amplitude) the same node, but with an additional perfect second order integrating active filter.



shows the spectrum of those waveforms. An advancement of over 30 dB can be constituted. Confronting this number with practical EMI problems, this is enough to get the emissions below the threshold levels of regulations and to keep the "switch noise" below the detection level of communication receivers.

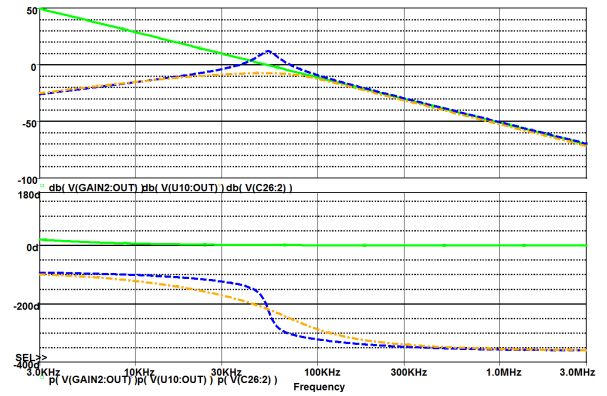
Fig. 11 Spectrum of the waveforms shown in figure 10: red (above) without active filter and green (below) with EMI cancelation filter consisting of two leaky integrators and an inverter.



3.2.2. Real Filters: Suppressing of the Audio

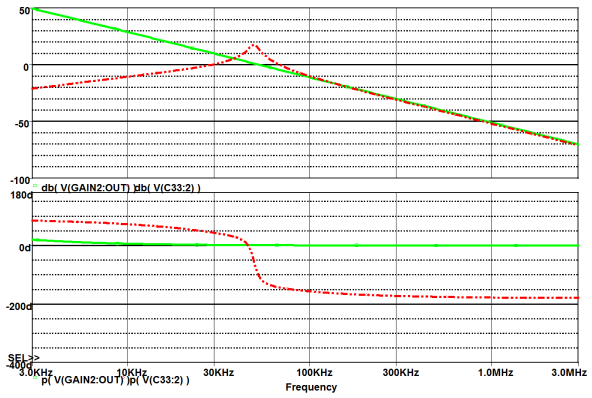
Taking the low frequencies of the transfer function as shown in figure 9 into deeper consideration, a resulting dilemma is, that the active EMI cancelation would not only remove the ripple but the audio signal as well. This is not only against the fundamental ambition of the amplifier but would also result in a huge amplification of the signal through the linear cancelation circuit. A suppression of the audio signal in the EMI cancelation path is therefore inevitable. The transfer functions of the two possibilities shown in figure 7 counteract this problem by damping in the audio band as shown in figure 12. Both

Fig. 12 Transfer functions of the extended bandpass filter (blue, dashed) and the extended second order lowpass filter (brown, dash-dotted) referred to the second order integrator (green, solid) from figure 10.



filters show an extra phase shift of 360 ° which is as good as a phase staying at 0 °. The bandpass filter requires a higher quality factor than the lowpass version to ensure suppression of the contents material as well as close following of the ideal solution.
Finally the transfer function of the Sallen-Key option is shown in figure 13. Even it requires an additional inverter, this solution is providing the best match in the frequency range of interest to the second order integrator. Therefore it is chosen for realization.

Fig. 13 Transfer functions of the Sallen-Key filter from figure 8 plotted in dotted red with reference to the solution from figure 10.

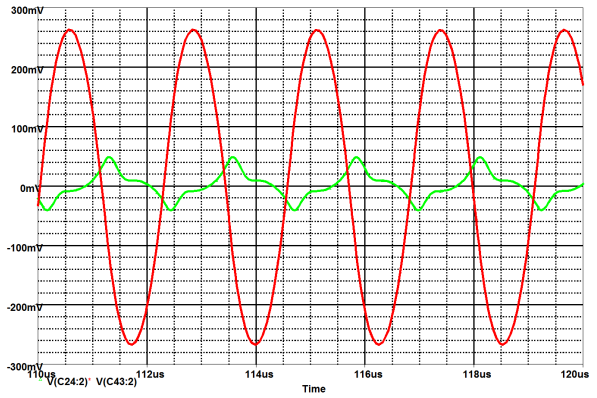


3.3. Implementation into Switch-mode Audio Power Amplifier

The synthesized filter needs to be designed in a matter to be capable to drive the output filter through the coupling capacitor C_{coupl}. Therefore a small linear stage as in [9] is used, which is the bandwidth limiting factor. Simulation of the complete circuit gives results as in figure 14.

The improvement in peak to peak ripple voltage with the Sallen-Key filter and the driver stage is 15.5 dB as opposed to the same output filter without AEC.
As stated in section 2.1, the output filter components and the coupling capacitor come with a substantial amount of tolerance which changes the transfer function of the second order integrator. The purpose of the AEC filter is to approximate this transfer function given by 2.3 and shown in figure 9 as close as possible. For a given and untrimmed AEC filter the expected improvement varies with the variation of the filter components.
Table 1 predicts the performance of AEC in dependence on the variation around their nominal values (L_{out} and C_{out}). Thereby the capacitor was modeled by a 10 % variance and the inductor by a 20 % and a 10 % scenario.

Fig. 14 Improvement of ripple size with designed AEC: red (high amplitude signal) is ripple without AEC and green (low amplitude signal) with AEC in place.



Concluding the tolerance consideration it might be desirable to choose both, inductor and capacitors, with 10 % tolerance.

Table 1 Influence of component tolerance

Inductor Value	Capacitor Value	Ripple Improvement
L_{out}	C_{out}	15.5 dB
$1.2 \cdot L_{out}$	$0.9 \cdot C_{out}$	16.1 dB
$0.8 \cdot L_{out}$	$1.1 \cdot C_{out}$	8.9 dB
$1.1 \cdot L_{out}$	$0.9 \cdot C_{out}$	20.9 dB
$0.9 \cdot L_{out}$	$1.1 \cdot C_{out}$	12.7 dB

4. VERIFICATION OF THE DEVELOPED ACTIVE EMI CANCELING SOLUTION

A switch-mode audio power amplifier as described in [10] was built and utilized to verify the described AEC filter. As for any amplifier its performance in terms of total harmonic distortion and noise is crucial. The proof of the amplifiers basic functionality is given by figure 15 and 16.

The Sallen-Key filter and the linear driver stage was integrated into a switch-mode audio power amplifier in parallel to the second order passive output filter. Figure 17 shows the output ripple voltage ripple without AEC in direct comparison to the same signal, when the active

Fig. 15 A-weighted total harmonic distortion and noise (THD+N) as a function of output power: top (red) at 1 kHz, bottom (blue) at 6.665 kHz.

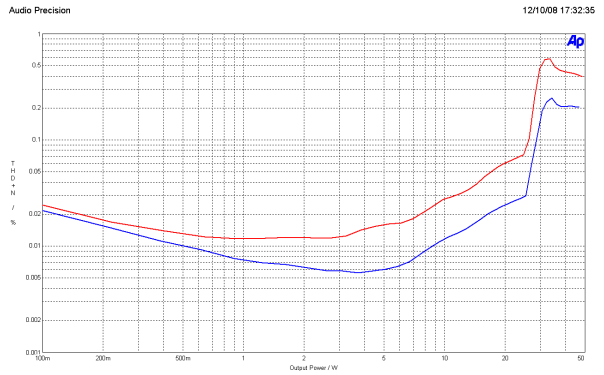


Fig. 16 A-weighted THD+N as a function of signal frequency.

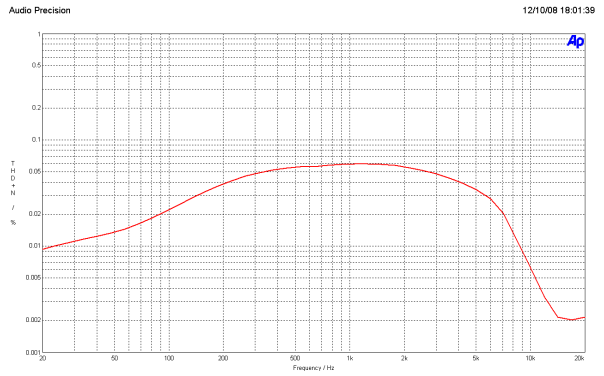


Fig. 17 Output voltage ripple without AEC.

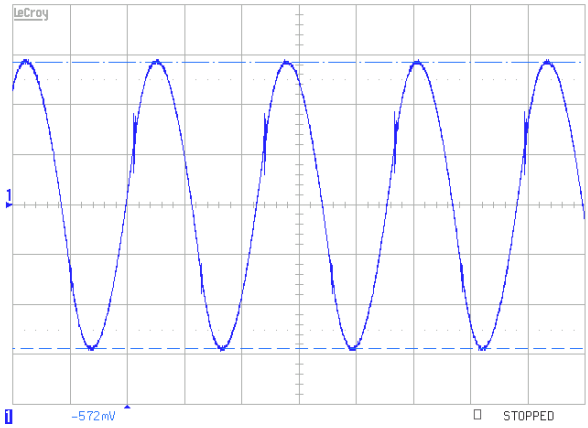
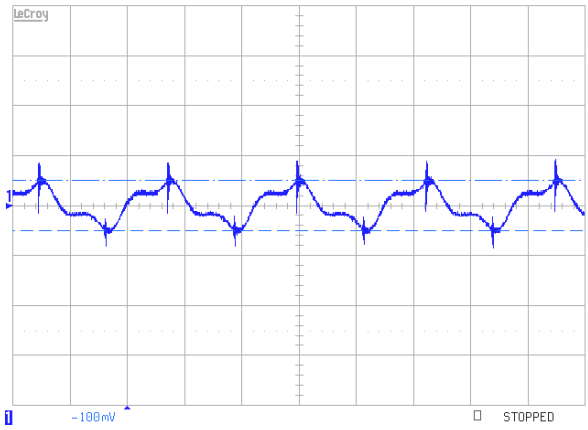


Fig. 18 Output voltage ripple with enabled AEC.



EMI cancelation is enabled in figure 18.

Of special notice is the change of the waveform: while the ripple without cancelation looks quite sinusoidal, AEC is limited by the linear amplifier and works best at the fundamental. Therefore the harmonics of the ripple get damped less and the waveform appears less sinusoidal.

The peak to peak ripple voltage got decreased from 572 mV to 100 mV, which is an improvement of 15.1 dB following quite close the predictions from simulation in section 3.3. Thereby the current consumption increased by 0.2 A from each rail.

5. CONCLUSION

The basic idea of active noise cancelation (ANC) got applied to the problem of electromagnetic interference (EMI) of switch-mode audio power amplifiers resulting in an active EMI cancelation (AEC) technology. The analytical requirements for this system got derived and topologies where chosen for best practical implementation. Reducing the topology to practice an EMI improvement of 15.5 dB in terms of peak to peak ripple reduction was predicted by simulation and the variances over production tolerances taken into account. Implementation into a sub 0.1 % distortion amplifier was able to reproduce a 15.1 dB by experiment.

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B.5 On the Myth of Pulse Width Modulated Spectrum in Theory and Practice

126th AES Conv., 2009, Munich, Germany, linked to all chapters

Audio Engineering Society

Convention Paper

Presented at the 126th Convention
2009 May 7–10 Munich, Germany

On the Myth of Pulse Width Modulated Spectrum in Theory and Practice

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ABSTRACT

Switch-mode audio power amplifiers are commonly used in sound reproduction. Their well known drawback is the radiation of high frequent energy, which can disturb radio and TV receivers. The designer of switch-mode audio equipment therefore needs to make arrangements to prevent this coupling which would otherwise result in bad audio performance. A deep understanding of the pulse width modulated (PWM) signal is therefore essential, which resulted in different mythic models as pulse, trapezoidal or Double Fourier Series (DFS) representations in the past. This paper will clarify these theoretical approaches by comparing them with reality from both the time and the frequency domain perspective. For validation a switch-mode audio power amplifier was built, delivering the contents material with less than 0.06 % distortion across the audio band at 50 W. The switch-mode signals have been evaluated very precisely in time and spectral domain to enlighten the assumptions about the PWM spectra and decrypt this myth.

1. INTRODUCTION

Pulse Width Modulation (PWM) is a wide spread approach for efficient conversion of energy from a source to the load of a given application. The field of power electronics covers numerous applications driving a switching element like a transistor into its saturation region or completely close it. A very special application is the reproduction of content material of audio sources. The final load in this application - the human ear - is a high quality demanding sensor. It can cover a wide range of levels (around 120 dB), detect even small perturbations like 0.01 % distortion and cover a broad range of different signal speeds (20 Hz to 20 kHz). Above that frequency band, another engineering discipline comes into play: electromagnetic compatibility. The

purpose of this qualifying variety is to allow the reproduction of content material for technical listeners, like radio receivers, TV receivers, radio communication and wireless steering and controlling applications.
In terms of switch-mode audio power amplifiers the frequency ranges above the human ears sensibility range becomes of interest, because it can disturb the above mentioned applications and – when having a closer look at radio receivers – the high frequent content can even disturb the reception of its own input signal. Drilling deeper into the spectrum of switch-mode audio power amplifiers, the myth about the PWM signal is quite widespread: some assume the PWM signal to be a rectangular signal, others treat it as a trapezoid while further take modulation into account.
An analytical way to describe the spectrum of the PWM signal was derived by [1] based on the methods of [2] and got reused many times later as for example in [3] for deriving the spectra of various related modulation techniques and phase shifting of different PWM signals and in [4] and [5] to cover multi-level converters in high power electronics and their total harmonic distortion.
This paper will first recall assumptions which are widely made in practical engineering about the PWM spectra in theory. This will cover modeling the PWM signal as a square wave, a trapezoid and as rectangular modulated pulses. To show the relevance for the practical problems of electromagnetic interferences (EMI), a prototype of a switch-mode audio power amplifier is demonstrated with a focus on staying close to industry available products instead of including the latest and greatest findings coming out of academia. The functionality of this prototype is proven in terms of qualifying audio parameters. Spectral measurements on this prototype validate the theory and show its limitations.

2. ANALYTICAL APPROACH TO UNDERSTANDING PWM SPECTRA

This section will build various commonly used modeling approaches for PWM signals, starting with the simple idea of a square wave then including the finite rise time of edges covered by a trapezoidal signal model to end up in the most precise but least practical approach of a Double Fourier Series (DFS).

2.1. Square wave modeling

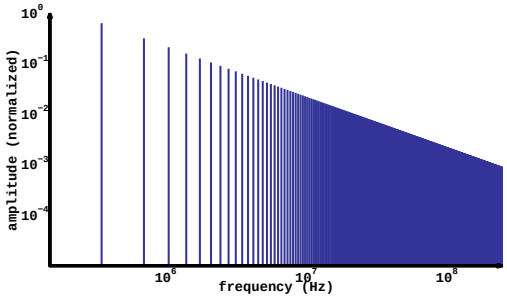
A common rule of thumb approach is to think about a PWM signal as a square wave. This straight forward approach is built on the fact that an ideal PWM signal without modulation needs to have 50 % duty cycle for avoiding a constant offset voltage across the speaker terminals. Any variations of the duty cycle would represent noise, which is undesired. The analytical representation of such a square wave p_{square} is covered by any introduction literature in technical education, e.g. [6], and is expressed by a Fourier Series as in equation 2.1.

Equation 2.1 Fourier Series expression for a square wave signal.

$$p_{square}(t) = \sum_{m=1}^{\infty} \frac{2H}{m\pi} \sin(m\omega_{sw}t)$$

Here m is representing the harmonic number, H is the height of the pulses and the radian switching frequency is ω_{sw}. The resulting spectrum for a switching frequency of $f_{sw} = \omega_{sw}/2\pi = 350$ kHz is shown in figure 1. Especially product development engineers – which are faced with EMI measurements – are familiar with square wave appearing signals from applications like microcontrollers, processors and high-speed communication busses. This engineering discipline tends to model those waveforms as trapezoids and therefore appreciate the finite rise and fall times of the signals [7] and [8]. With equal rise and fall time τ the analytical expression via Fourier Series is equation 2.2

Fig. 1 The spectrum of a rectangular waveform.

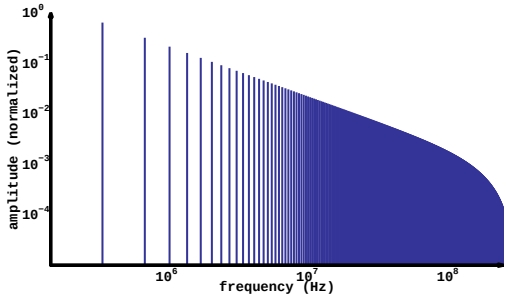


Equation 2.2 Fourier Series expression for a trapezoidal signal.

$$p_{trapeze}(t) = \sum_{m=1}^{\infty} \frac{2H}{\pi^2 \tau f_{sw}} \frac{\sin(\pi \tau f_{sw})}{m^2} \sin(m\omega_{sw} t)$$

With the rise and fall time of the edges set to a realistic value (by experience a thousandth of the period $1/f_{sw}$) of 3.5 ns, figure 2 gives a numerical representation of equation 2.2. Additions to this model-

Fig. 2 The spectrum of a rectangular waveform.



ing principle include also ringing on the waveform [7]. However none of those rule-of-thumb modeling methods are capable of including the impact of the audio signal on the resulting spectrum. Therefore they are only valid for small-signal investigations around the ideal idle point of a switch-mode audio power amplifier.
To develop the fourier series result of a PWM signal, it would not take more than an integration over the pulses along one period of the audio signal, wherever the signal is high and no contribution to the result whenever the signal is low. It therefore only needs to be known, whenever the signal crosses the midpoint. Knowing these points it would be trivial to include the finite edges as described above. These so called decision points are in most of the switch-mode audio power amplifiers an effect of a triangular signal crossing a sinusoidal signal. The triangular signal can be modeled as a piecewise linear function. The analytical derivation of the crossing points is according to this principle the solution for x of equation 2.3 with a, b and c being coefficients to represent the correct bias point, the slope of the triangular carrier and the frequency of the content material.

Equation 2.3 Expression to derive decission points from a carrier and reference.

$$a + b \cdot x = \sin(c \cdot x)$$

Unfortunately there is no analytical solution known for this problem. However displaying both, the carrier and the reference signal over a separate time axis each, the projection of the third dimension can be used to represent a PWM signal according to the DFS [1]. The result from this method includes different parts:

- a time invariant component (DC),
- the contents material (music signal),
- a modulation independent representation of the switching frequency and its harmonics,
- the same frequencies, but modulation dependent,
- left side band components to each of the switching frequency harmonics and
- right side bands thereto.

Each of those components has its discrete amplitude and phase representation. Different modulation principles show different symptoms. A double edge modulated signal, for example, has no contribution from the third component in the above list. The different parts as listed above are given by equation 2.4.

Equation 2.4 Double Fourier Series result for a double edge modulated PWM signal (positive frequencies only).

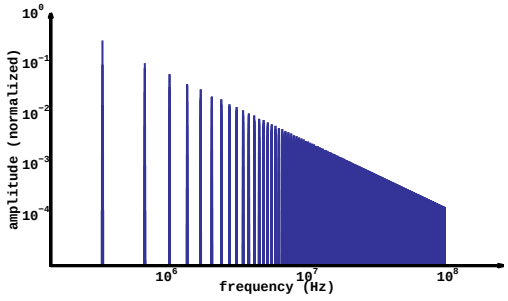
$$
\begin{aligned}
p_{DFS}(t) \quad = \quad & HM\cos(\omega_{audio}t) \\
& \sum_{m=1}^{\infty} \frac{HJ_0(mM\pi)}{m\pi}\sin(m\omega_{sw}t - m\pi) \\
& \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{HJ_n(mM\pi)}{m\pi} \\
& \sin((m\omega_{sw} + n\omega_{audio})t - (m + \frac{n}{2})\pi)
\end{aligned}
$$

The additional coefficients M and ω_{audio} and n describe the modulation index, the frequency of the content material and the number of the side band peak with reference to the harmonic it is attached to. The function J is the magnitude of the Bessel function of the first kind. To derive this equation some of the equations of [9], [10] and [11] are required.

These enable a fast and very accurate prediction of the spectrum of a PWM signal which is shown in figure 3.

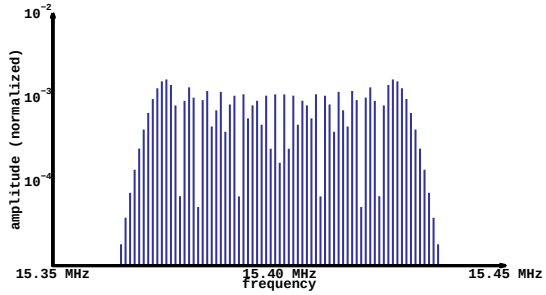
As the left side bands may fall into the audio band,

Fig. 3 The spectrum of a double side PWM signal at $M = 20$ % modulation depth



provisions have been taken to eliminate those in [12]. Compared to the above descriptions with rectangular and trapezoidal signals as modeled for the PWM signal, the DFS enables a more detailed spectral evaluation. Figure 4 shows the 44tth harmonic of the switching frequency and its relevant side bands.

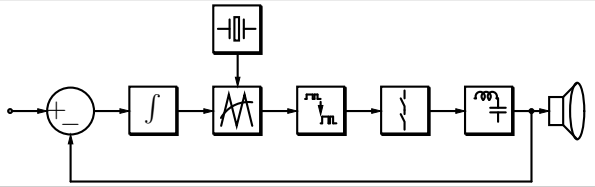
Fig. 4 An arbitrarily chosen harmonic of the switching frequency and its side bands.



3. EXPERIMENTAL BASIS

To verify the described theoretical explanation of the spectrum, a prototype of a double edge modulated switch-mode audio power amplifier was built. The block diagram in figure 5 shows the input, a summing point for the feedback, followed by a double edge modulator which is supplied by a triangular waveform from an crystal oscillator. The modulator output is getting level shifted before the half bridge is driving the speaker through a second order LC low pass filter. Figure 6 is a photograph of the realized

Fig. 5 Block diagram of the switch-mode audio power amplifier



prototype. The achieved audio performance of the prototype is shown in figures 7 and 8. The amplifiers distortion peaks at 0.06 % delivering a 50 W, 6.665 kHz signal to the load. A signal to noise ratio of 120 dB is provided by this amplifier.

4. SPECTRAL ACHIEVEMENTS FROM EXPERIMENT

The described amplifier was used to evaluate the spectrum of the PWM signal in practice. Opposed to the assumptions of rectangular signals, as made in the theoretical approaches described in section 2, the PWM signal contains an overshoot after each

Fig. 6 Picture of prototype.

Fig. 7 A-weighted Total Harmonic Destortion and Noise (THD+N) of the prototype amplifier as a function of output power. The top curve shows the preformance at 6.665 kHz audio signal, the lower curve for 1 kHz.

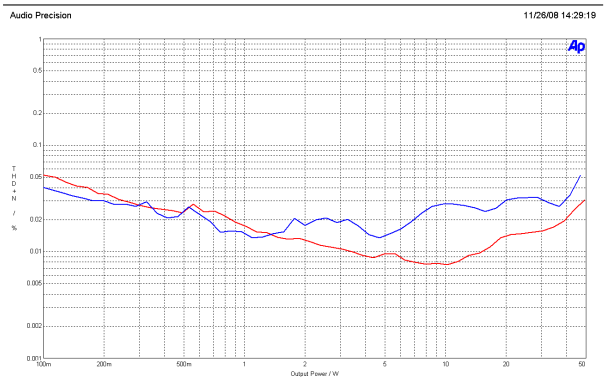


Fig. 8 A-weighted THD+N across the audio band at 50 W output power level.

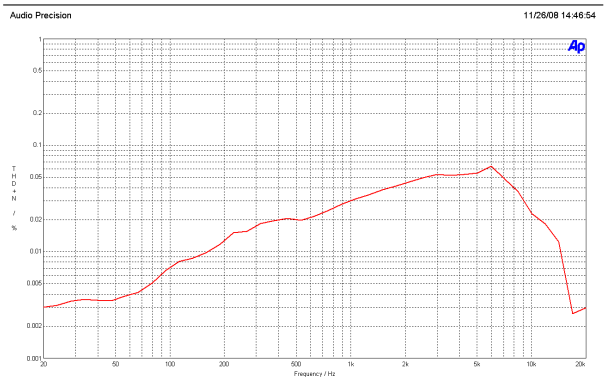
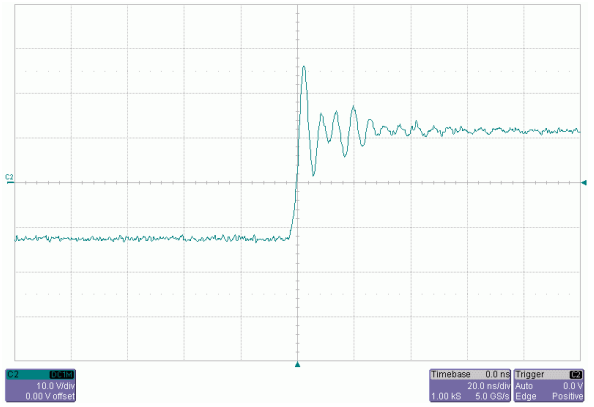


Fig. 9 Overshoot after a rising transition point captured by a 1 GHz oscilloscope LeCroy 6100A.



decision point from low to high and an undershoot respectively for negative going transitions. This supply voltage exceeding event is followed by a short swinging. For a positive and a negative transition the described phenomena are shown in figures 9 and 10 respectively. Another assumption for analytical evaluation is infinite rise and fall times. In the experimental amplifier they have been 3 ns and 4 ns respectively. The spectral occurrence of the switch node (PWM signal of the power stage) in the amplifier was measured with an EMI Test Receiver Rhode & Schwarz ESI7. A first quick screening of the band of interest was done according to the settings as legislative requirements demand. Therefore the resolution bandwidth RBW was set to 9 kHz and the impact of modulation to the switch nodes spectrum was measured. Figure 13 illustrates the measurement results for three different modulation indices. There is actually no notable difference dependent on the modulation depth. The effect of the rise and fall time on the spectrum can be recognized around 200 MHz. The spectrum begins to drop off there rapidly but rising again later.

This setting is only detecting the envelop of the spectrum. To capture the modulation dependent sidebands of a 1 kHz sine wave at a modulation index of $M = 0.2$, the RBW was set to 200 Hz. Each

Fig. 10 Overshoot after a falling transition point.

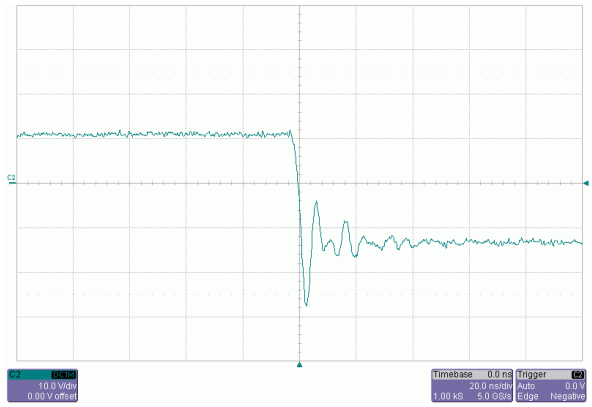
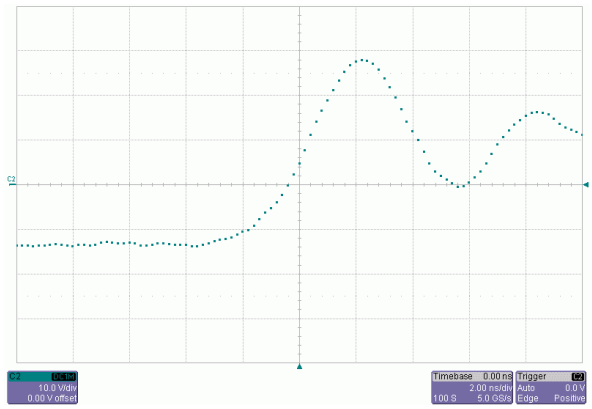


Fig. 11 Limited rise time of the PWM signal: $t_r \approx 3$ ns



80 Hz the receiver captured a data point over a time period of $t_{step} = 2$ ms. This setting allows to detect any signal resulting from modulation and from the audio. The setting is therefore also quite close to reality of radio receivers, which stay at a specific frequency also for multiple periods of the contents material. These devices also divide between small spectral distances away from their center frequency, because this is actually the contents material.
Measuring with such a precision, it is not possible to display the results on the analyzers screen, because it has less resolution as the number of data points. Therefore the measured data was extracted from the instrument and displayed via Matlab. Another restriction of the measurement equipment is

Fig. 12 Limited fall time $t_f \approx 4$ ns differs from the rise time.

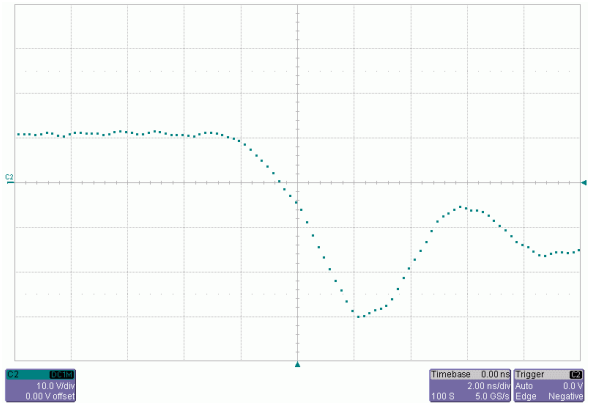
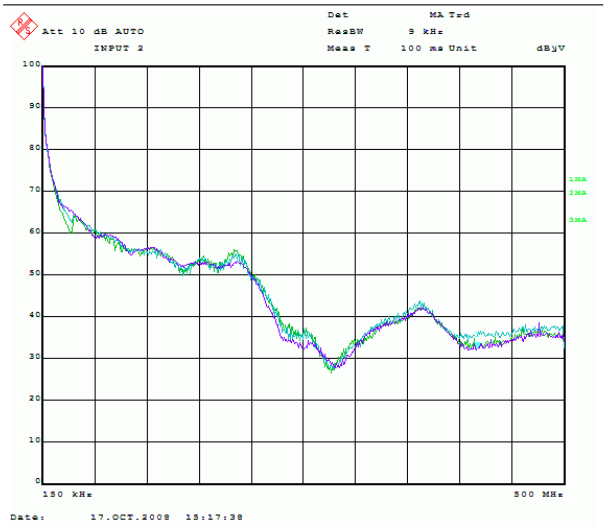


Fig. 13 Spectrum of the switch node measured with $RBW = 9$ kHz and a measurement time at each point of $t_{step} = 100$ ms from 150 kHz to 500 MHz.

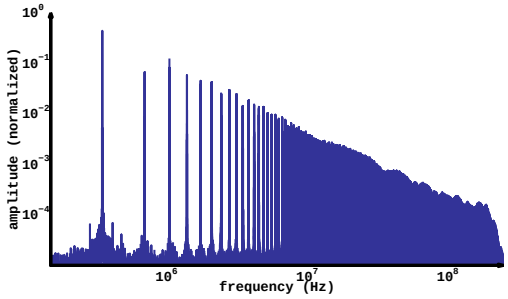


the amount of measurement memory. To overcome those limitations, the EMI test receiver has been automated via GPIB and performed the measurements under remote control. Notice that the pure measurement time - excluding the instruments time to settle between shifting its input window and settling times of settings - are close to two hours. In total the capturing took more than 24 hours. All captured data points are displayed in figure 14 as allowed by the limitations of the computer display and the inter-

pretation of Matlab how to display nearly 4 million data points on a 1900 dot wide display.

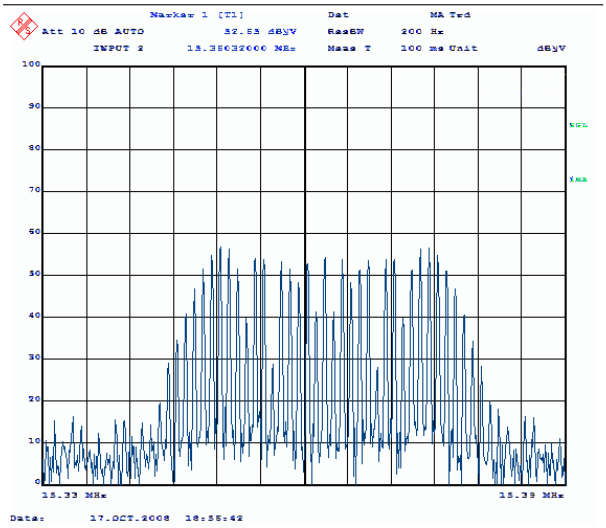
To get a more precise picture of the PWM signal

Fig. 14 Precisely measured spectrum of the PWM signal with display limitations in a frequency range from 150 kHz to 300 MHz.



the arbitrary chosen 44th harmonic of the switching frequency and its side bands is shown in figure 15.

Fig. 15 Zoom into measured spectrum at the 44th harmonic of the switching frequency.



5. COMPARISON OF THEORY AND PRACTICE

As in many engineering disciplines it is quite useful for developers to have practical models of system behavior in mind, however the area of validity must be remembered all the time. Simple models to understand the PWM signal have been shown in this paper. Their complexity was increasing from a simple rectangular signal through a trapezoidal signal ending up with a rectangular representation of the PWM behavior via DFS. The trapezoidal signal exceeds the validity beyond a pulse model by taking the finite rise and fall times of the edges into account resulting in a high frequency roll-off of the magnitude spectrum. The DFS on the other hand allows a deeper understanding of the modulation process in the spectral domain. This modeling approach is adding even order harmonics of the switching frequency as well as side bands to each of the harmonics.

The built and measured prototype's purpose was meant to test the validity of these mythic models. After validating the functionality of the amplifier by relevant audio measurements a closer look at the signals in time domain was undertaken. The transition times (switching events) where found to vary greatly from the assumptions of the models. The signal shows over- and underswing following the switching events and the rise and fall times were different. Setting the EMI test receiver to parameters as demanded by legal requirements shows a good correlation to the models up to the inverse of rise and fall times. Beyond that frequency, the spectrum starts to rise again completely uncorrelated to expectations. More precise measurement methods, which are following the actual behavior of radio and TV receivers, reveal a good correlation between the trapezoidal model for the envelope of the spectrum, but a closer consistence to the DFS model when considering the single spectral measurement points.

The final enlightening of the myth of PWM spectra is, that dependent on how and which frequency range of the PWM signal is measured one or another model is more adequate. For looking at a very broad spectral range, but only the envelop of the magnitude spectrum, the trapezoidal model is best accommodating for the expected spectrum. This is the recommended method for a broad normative EMI test. In case a precise understanding within a very narrow frequency range is demanded, the DFS approach fits best. This would be the case if a theoretical prediction of spectrum around specific transmission bands (e.g. the frequency modulated radio (FM radio)) is in question. Assuming the PWM signal to be a rectangular signal shows enough precision for the lower

frequency bands and no modulation applied to the amplifier. This would be the case when trying to get an estimation of the worst case spectrum in the amplitude modulated radio (AM radio) bands.

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B.6 Multi Carrier Modulation Audio Power Amplifier with Programmable Logic

37th AES Conf., 2009, Hillerød, Denmark, linked to chapter 4

Multi Carrier Modulation Audio Power Amplifier with Programmable Logic

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ABSTRACT

While switch-mode audio power amplifiers allow compact implementations and high output power levels due to their high power efficiency, they are very well known for creating electromagnetic interference (EMI) with other electronic equipment. To lower the EMI of switch-mode (class D) audio power amplifiers while keeping the performance measures to excellent levels is therefore of high interest. In this paper a class D audio amplifier utilising Multi Carrier Modulation (MCM) will be analysed, and a prototype Master-Slave Multi Carrier Modulated (MS MCM) amplifier has been constructed and measured for performance and out of band spectral amplitudes. The basic principle in MCM is to use programmable logic to combine two or more Pulse Width Modulated (PWM) audio signals at different switching frequencies. In this way the out of band spectrum will be lowered compared with conventional class D amplifiers. Analytically expressions, simulations and measurements result in reduced switching frequency amplitudes using MCM techniques. It is also shown that the Total Harmonic Distortion (THD) tends to be compromised compared to conventional class D amplifiers due to intermodulation products of the switching frequencies entering the audio band. Still, the MS MCM topology with two carrier signals shows a 6 dB reduction of the switching frequency amplitudes as well as THD across the audio band below 1% at 55 W output power open loop.

1. INTRODUCTION

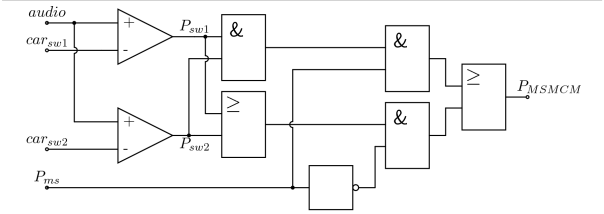
While switch-mode audio power amplifiers allow compact implementations and high output power levels due to their high power efficiency, they are very well known for creating electromagnetic interference (EMI) with other electronic equipment. To lower the EMI of switch-mode audio power amplifiers while keeping the performance measures to excellent levels is therefore of high interest.

Multi Carrier Modulation (MCM) is introduced in [1],[2] as a new audio modulation technique to effectively reduce the out of band spectral components present in switch-mode (Class D) audio power amplifiers. In MCM, multiple carrier signals at different frequencies are compared to the audio signal to produce multiple Pulse Width Modulated (PWM) signals. The multiple PWM signals are combined to a single altered PWM signal by digital logic operators. [1],[2] reports that simply combining two PWM signals with an AND-gate (ANDing) or OR-gate (ORing) indeed reduces the spectral amplitudes of the switching frequencies, but they introduce distortion. Also a DC offset is present due to the uneven distributions of 1's and 0's in the AND and OR truth tables. XOR and XAND have not been found suitable for combining PWM signals. Instead a so-called Master Slave MCM (MS MCM) has been proposed, which utilises a derivative of one of the triangle carrier signals as a master clock. It has been shown that the MS MCM architecture has increased Total Harmonic Distortion (THD) compared to a conventional class D amplifier. A THD of 0.1% is possible without load and with a PI compensator in the feedback loop.

In this paper an altered MS MCM architecture is used, see figure 1, where the master clock is independent of carrier frequencies and thus introduces a third switching frequency in the system.

The logic part in prior MCM prototypes have been designed using discrete components, [1],[2]. However, in the prototype in this paper, the logic is programmed into a Complex Programmable Logic Device (CPLD). The benefit of using a CPLD is that different MCM meth-

Fig. 1 Master Slave MCM block diagram.



ods can be used on the same prototype board simply by re-programming the CPLD. Frequency dividers and master clocks can be implemented internally. The use of a CPLD also makes it easy to experiment and test new and more complex MCM architectures for future research.

Section 2 analyses the logical operators AND, OR and MS MCM of two PWM signals from an analytical point of view. The expressions are verified with MATLAB SIMULINK simulations in section 3. The design implemented in the MCM prototype is described in section 4 and measurement results on spectral amplitudes and Total Harmonic Distortion (THD) [3] are shown in section 5. A new setup using Multiple Master Slave Multi Carrier Modulation (MMS MCM) blocks is presented in section 6.

2. MULTI CARRIER MODULATION CALCULATIONS

In this section analytically expressions for the AND logic operator of two PWM signals will be presented. These investigations are made in order to explain the behaviour of MCM.

A natural sampled, two level, double sided PWM audio signal, P_{PWM}, can be expressed using [4] as

$$\begin{aligned} P_{PWM} =& k && \text{(k)}\\ &+MH\cos(y) && \text{(A)}\\ &+2H\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx) && \text{(B)}\\ &+2H\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\cdot\\ &\quad\sin(m\pi/2+n\pi/2)\cos(mx+ny) && \text{(C)} \end{aligned}$$

where $y=\omega_a t$ and $x=\omega_{sw}t$ is the audio and switching frequency in radians, respectively, t is the time, $J_n(a)$ is the n'th order Bessel function of argument a, M is the modulating index, and H is the signal amplitude. The term (A) is the audio signal with a possible DC offset k. The term (B) is the switching frequency and its harmonics while the last term (C) represents the side lobes on both sides of the switching frequency and its harmonics. Similar expressions for single sided and three level PWM exists, see [4], [5], [6].

By choosing $k=0.5$ and $H=0.5$, the PWM signal ranges from 0 to 1, and the logic operators used in ANDing, ORing, and MS MCM can be expressed as shown in table 1.

Table 1 Logic operators used for MCM.

Logic operator	Symbol	Expression
ANDing	P_{AND}	$P_{sw1}P_{sw2}$
ORing	P_{OR}	$P_{sw1}+P_{sw2}-P_{sw1}P_{sw2}$
MS MCM	P_{MSMCM}	$P_{AND}P_{ms}+P_{OR}(1-P_{ms})$

where P_{sw1} and P_{sw2} are PWM signals with switching frequencies f_{sw1} and f_{sw2} respectively, and P_{ms} is the master clock signal with frequency f_{ms}.

The master clock signal is a square wave and can be expressed as

$$P_{ms}=\sum_{m=1}^{\infty}\frac{4H}{(2m-1)\pi}\sin\left((2m-1)\omega_{ms}t\right) \qquad (1)$$

The significant logic operator is the AND operator since it is used in both the OR and MS MCM operators. The expression for P_{AND} can be interpreted as the product: $(k+A_1+B_1+C_1)(k+A_2+B_2+C_2)$ and a full expression is given in appendix A.
Table 2 lists some interesting aspects of the P_{AND} expression. Note that all amplitudes are independent of the switching frequencies. The amplitude expressions for the switching and intermodulation frequencies utilises the trigonometric identity

$$\cos(a)\cos(b)=\frac{1}{2}\left[\cos(a+b)+\cos(a-b)\right] \qquad (2)$$

Similar expressions are derived for P_{OR}. P_{OR} has a normalised DC offset of 1.25, that is, +25% compared to convetional PWM. Apart from that, all frequency component amplitudes in P_{OR} are equal to P_{AND}, simply because $k=0.5$.

The DC offset and second harmonic component of the audio signal present in both ANDing and ORing MCM

Table 2 Amplitude expressions for specific frequency components in P_{AND}. Expressions are evaluated for $k = 0.5$, $H = 0.5$, and $M = 0.75$ and normalised with respect to H.

Component	Appendix reference	Amplitude expression	Normalised value	Comment
DC offset	(kk), (A1A2)	$k^2 + \frac{1}{2}(HM)^2$	0.75	Last term found using $\cos^2(x) = \frac{1}{2}(1+\cos(2x))$. DC offset is -25% of the audio amplitude.
Audio	(k(A1+A2))	$2kHM$	1	Audio amplitude is unaffected.
Audio second harmonic	(A1A2)	$\frac{1}{2}(HM)^2$	-17.0 dB	THD is roughly given by the amplitude of the second harmonic component.
Switching frequency	(k(B1+B2))	$2kH\frac{\mathrm{J}_0(\pi M/2)}{\pi/2}\sin(\pi/2)$	-7.2 dB	The amplitudes of the switching frequencies are reduced a factor 2 with respect to ordinary PWM.
First intermodulation	(B1B2), (C1C2)	$\left[H\frac{\mathrm{J}_0(\pi M/2)}{\pi/2}\sin(\pi/2)\right]^2 + 2\left[H\frac{\mathrm{J}_2(\pi M/2)}{\pi/2}\sin(3\pi/2)\right]^2$	-13.6 dB	First intermodulation component $\lvert f_{sw1} - f_{sw2}\rvert$ should not enter the audio band to prevent distortion.

makes direct use of both modulation types not optimal for audio applications.

The full analytical expression for MS MCM, which is not included in the paper, shows that MS MCM has no DC offset nor second harmonic component of the audio signal. These components are shifted in frequency due to the multiplication of the master clock signal P_{ms}. Instead MS MCM has more intermodulation products and extra care has to be taken to avoid intermodulation products in the audio band and at the resonance top of the output filter.

Frequency spectra for all described MCM methods are shown in figure 2 and are evaluated for $k = 0.5$, $H = 0.5$, $M = 0.75$, $\omega_{sw1} = 2\pi \cdot 250$ kHz, $\omega_{sw2} = 2\pi \cdot 625$ kHz, and $\omega_{ms} = 2\pi \cdot 431$ kHz. The scaling is chosen to match measurement results later in the paper. The spectra in figure 2 have been numerically evaluated using the expressions in table 1, where P_{sw1} and P_{sw2} have been evaluated with sum indexes in equations (B) and (C) up to 100. Table 3 concludes this section by showing the reduction in switching frequency amplitude of all described MCM methods with respect to the switching frequency amplitude of P_{PWM}. The switching frequencies have been chosen arbitrarily while still assuring that the first intermodulation products are out of the audio band. For MS MCM, two master clock frequencies have been used in the calculations.

Table 3 Calculated reduction in MCM switching frequency amplitudes with respect to the switching frequency amplitude of P_{PWM}.

f_{sw} [kHz]	250	625	431	192
ANDing [dB]	-5.7	-5.6	–	–
ORing [dB]	-6.2	-5.8	–	–
MS MCM [dB]	-6.0	-5.3	-5.7	–
MS MCM [dB]	-6.0	-5.7	–	-5.2

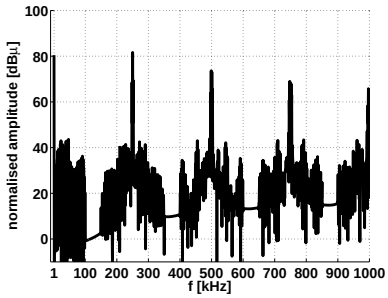
3. MCM SIMULATIONS

To verify the previous calculations and expressions a MATLAB SIMULINK model has been setup. The model is constructed from the schematic shown in figure 1. Using the same switching and clock frequencies, the simulated spectra for all MCM methods are shown in figure 2.

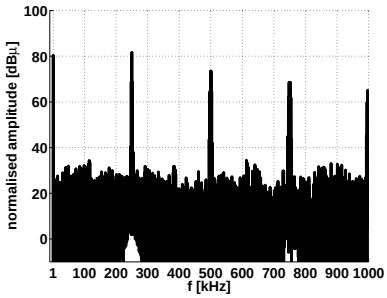
There is good agreement between calculated and simulated results. The simulated reduction in frequency amplitude, see table 4, are also in good agreement with the

Fig. 2 Calculated and simulated output spectra for P_{PWM}, P_{AND}, P_{OR}, and P_{MSMCM}.

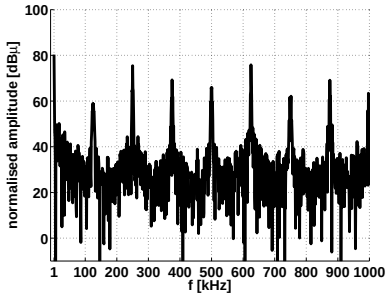
(a) Calculated P_{PWM} spectrum.



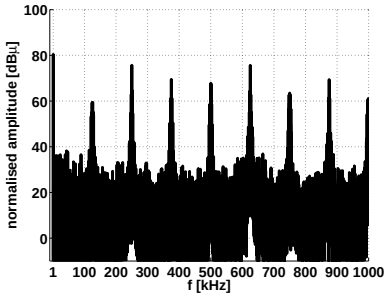
(b) Simulated P_{PWM} spectrum.



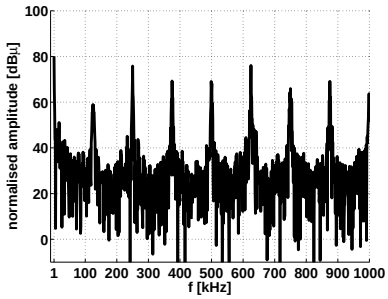
(c) Calculated P_{AND} spectrum.



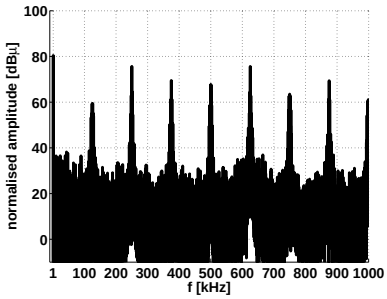
(d) Simulated P_{AND} spectrum.



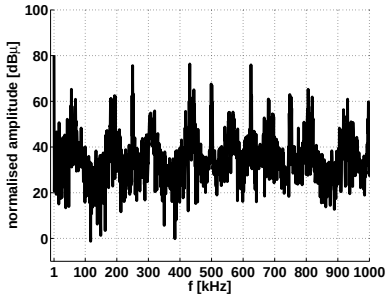
(e) Calculated P_{OR} spectrum.



(f) Simulated P_{OR} spectrum.



(g) Calculated P_{MSMCM} spectrum.



(h) Simulated P_{MSMCM} spectrum.

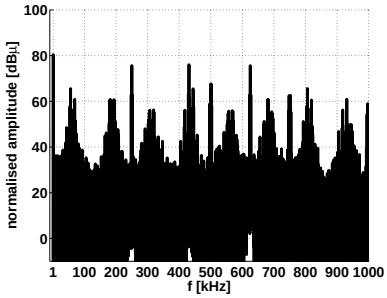


Table 4 Simulated reduction in MCM switching frequency amplitudes with respect to the switching frequency amplitude of P_{PWM}.

f_{sw} [kHz]	250	625	431	192
ANDing [dB]	−6.0	−5.9	–	–
ORing [dB]	−6.0	−6.1	–	–
MS MCM [dB]	−6.1	−5.7	−6.1	–
MS MCM [dB]	−6.0	−6.0	–	−5.7

previous calculations. The model verifies the analytical expressions from the previous section.

4. MCM AMPLIFIER DESIGN

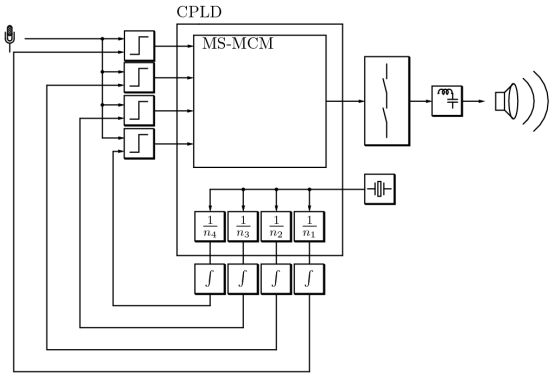
An MCM prototype amplifier, see figure 3, has been constructed. The prototype has been designed from the principle block diagram shown in figure 4. It utilises four PWM signals, where each can be set to a specific switching frequency. Each PWM signal is generated as follows: The CPLD is clocked by an external 25 MHz crystal. Internal counters in the CPLD divides the 25 MHz to lower frequencies useful in switch-mode audio applications; the frequencies available are given by $\frac{25}{n}$ MHz, where n is an integer. Four integrators then converts the clock signals to triangle carriers, which, when compared to audio, produces PWM audio signals at different frequencies. The PWM audio signals are sent back to the CPLD where the MCM logic operations are performed. With this configuration it is possible to experiment and test different signals by programming the CPLD with a new source code written in Very high speed integrated circuits Hardware Description Language (VHDL). The CPLD used in this prototype is a Lattice ispMACH 4000V with 64 macrocells.

5. MEASUREMENT RESULTS

The prototype board is used to measure THD performance and switching frequency amplitudes. The spectrum measurements are performed open loop in order to compare the measured results with the expected values from the calculations and simulations. The measurements are performed directly on the output of the CPLD. This means that effects like limited edges, overshoot, and undershoot from the power stage and output filter are avoided. The measurements are made with a Rohde&Schwarz EMI test receiver ESI7. In figures 5 and 6, the spectrum of ordinary PWM, ANDing, ORing, and MS MCM can be seen with $\omega_{sw1} = 2\pi \cdot 250$ kHz,

Fig. 3 Prototype circuit board with CPLD.

Fig. 4 Overview schematic showing how the CPLD is utilised on the prototype board.

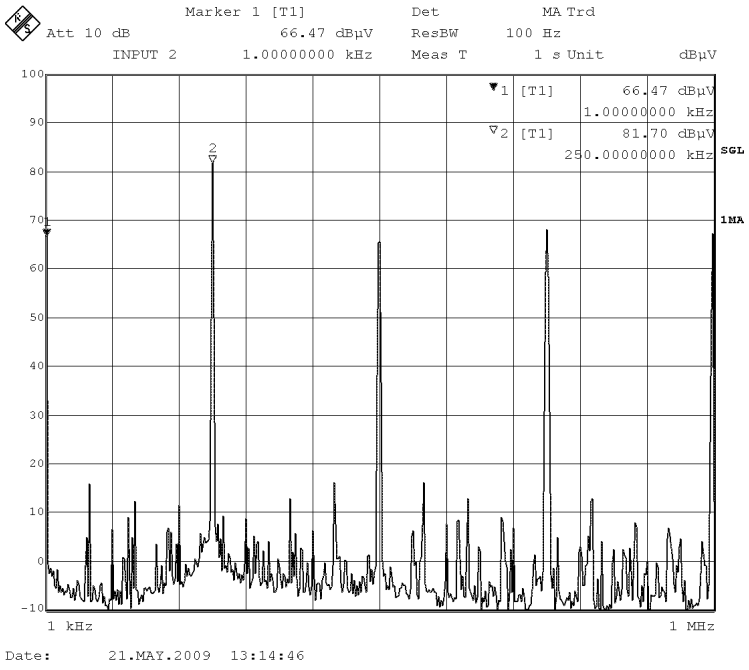


$\omega_{sw2} = 2\pi \cdot 625$ kHz, and $\omega_{ms} = 2\pi \cdot 431$ kHz. It should be noted that the audio amplitude is lower than expected compared to the switching frequency amplitude. This is due to a high pass filter in the measuring equipment; frequencies over 100 kHz are reasonable accurate and comparable. However, the reduced audio amplitude is consistent, so it is possible to compare the results.

The measured switching frequencies amplitudes are normalised with respect to the PWM signal, as seen in table 5. These normalised frequencies can be compared with the results from the simulations, see table 4,

Fig. 5 Measured output spectra for P_{PWM} **(a)**, P_{AND} **(b)**

(a) Measured P_{PWM} spectrum.



(b) Measured P_{AND} spectrum.

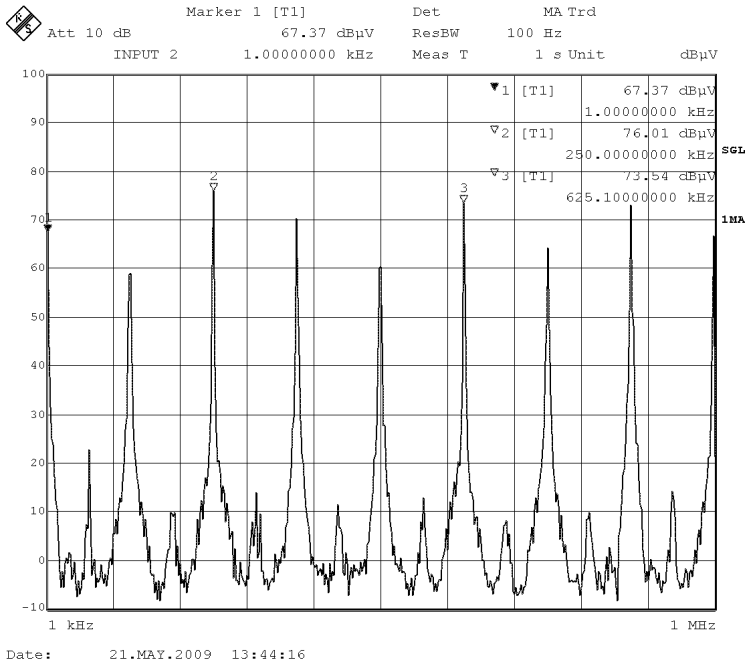
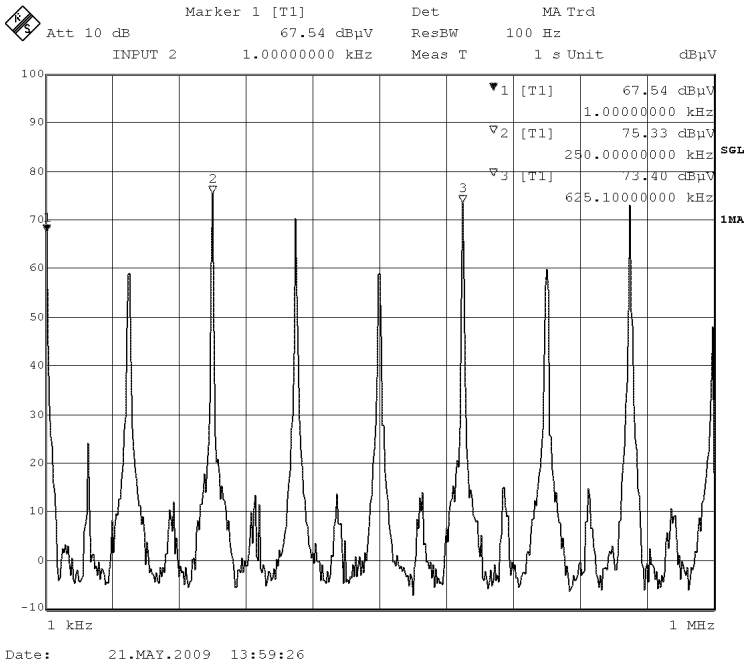


Fig. 6 Measured output spectra for P_{OR} **(a)**, and P_{MSMCM} **(b)**.

(a) Measured P_{OR} spectrum.



(b) Measured P_{MSMCM} spectrum.

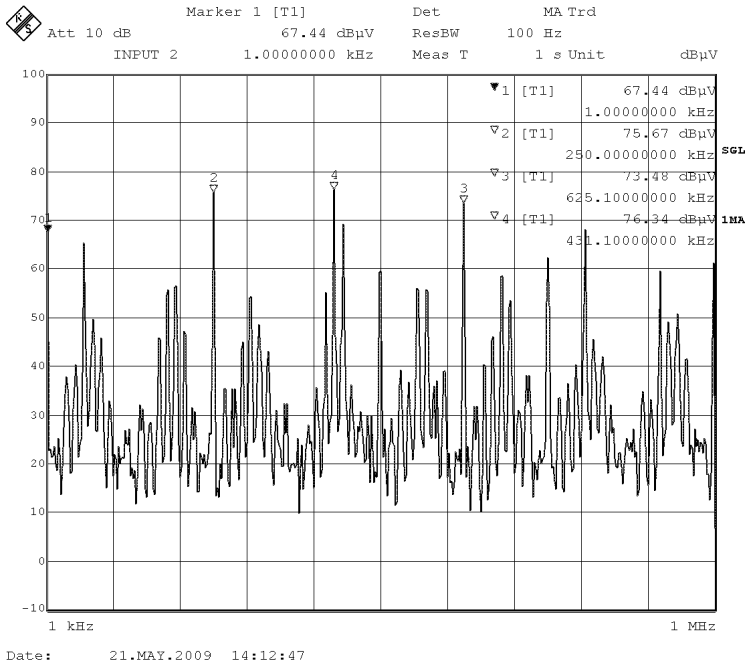
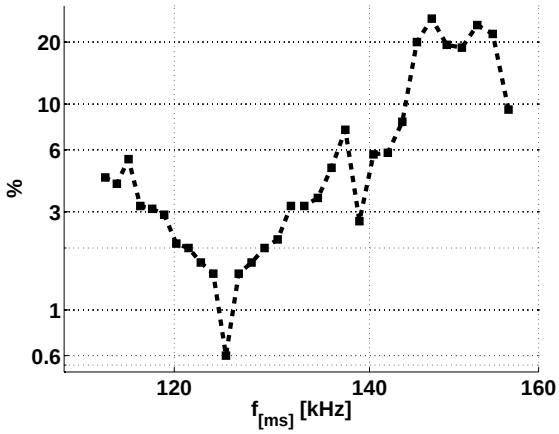
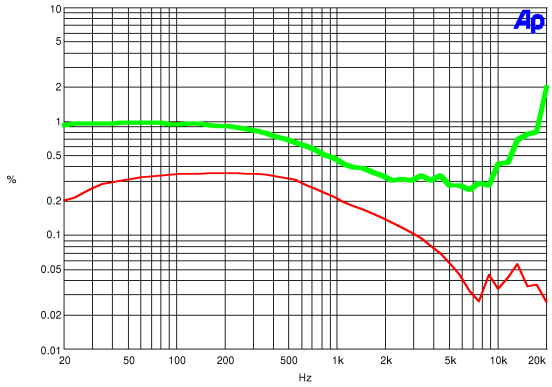


Fig. 7 Measured open loop THD from prototype MCM amplifier. The lower graph (red) is with a normal PWM signal output while the upper graph (green) is with a MCM signal output.

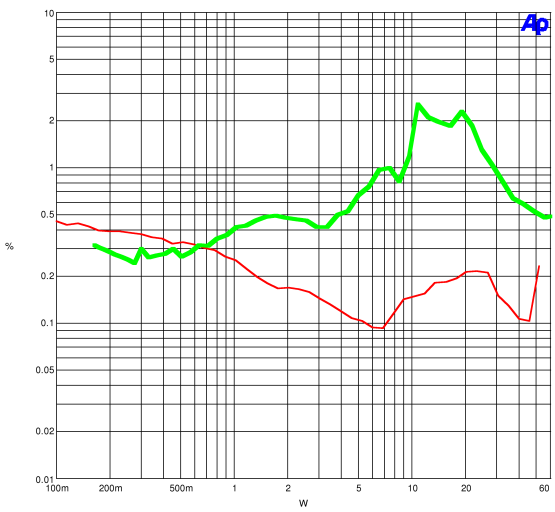
(a) Measured THD at different master clock frequencies.



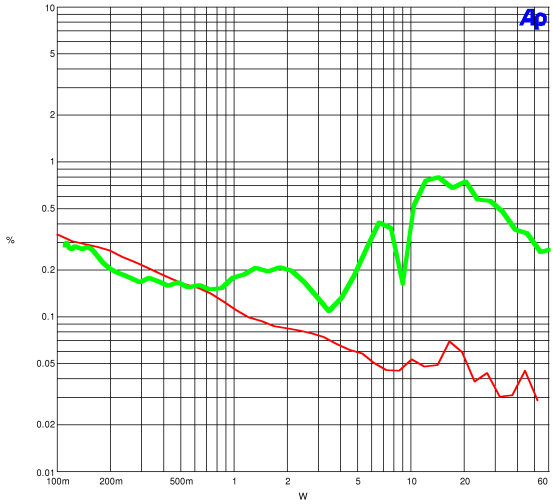
(b) Measured THD versus frequency at 55 W output power.



(c) Measured THD versus power at 1 kHz audio input.



(d) Measured THD versus power at 6.67 kHz audio input.



and actually the measured reduction of the switching frequency amplitudes is better as predicted.

5.1. THD in MCM prototype

As stated in the introduction, the MS MCM amplifier introduces extra THD. This is mostly because of intermodulation components between the different switching frequencies entering the audio band. Therefore THD measurements as a function of master clock frequency are performed. The THD is measured at 1 kHz audio input with 0.2 modulation index. The measurements are

Table 5 Measured reduction in MCM switching frequency amplitudes with respect to the switching frequency amplitude of P_{PWM}.

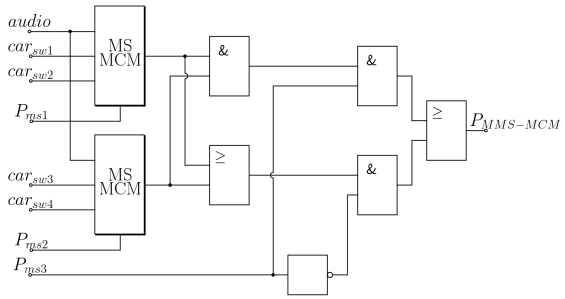
f_{sw} [kHz]	250	625	431	192
ANDing [dB]	−6.6	−9.1	–	–
ORing [dB]	−7.4	−9.4	–	–
MS MCM [dB]	−7.0	−9.2	−6.3	–
MS MCM [dB]	−6.9	−9.2	–	−6.9

made including the power stage and output filter, but still open loop. As a reference, THD of a normal PWM signal was measured to 0.15% THD. The THD versus master clock frequency, see figure 7a, is highly affected by the choice of master clock frequency. The wide variation in THD is due to intermodulation products entering the audio band.
Figures 7b, 7c, and 7d show the measured THD versus frequency and power, respectively, with MCM frequencies $\omega_{sw1} = 2\pi \cdot 250$ kHz, $\omega_{sw2} = 2\pi \cdot 500$ kHz, and $\omega_{ms} = 2\pi \cdot 125$ kHz. The THD measurements are performed open loop to ensure that the feedback does not compensate differently on PWM and MCM, thereby making direct comparisons doubtful.

6. FUTURE WORK - MULTIPLE MS MCM

As future work it could be interesting to investigate an extended Multiple Master Slave Multi Carrier Modulated (MMS MCM). It utilises multiple MS MCM blocks in a tree-like structure see figure 8. MMS MCM can be setup on the prototype by utilising all four available carrier signals at four different switching frequencies. Two MS MCM blocks with two different master clocks are used to generate two output signals. A third MS MCM (without the two comparators) has the two outputs as inputs and another master clock is inserted, thus producing a single output MCM PWM signal consisting of up to 7 different switching frequencies. In principle, the procedure can be repeated with even more MS MCM blocks. However, to effectively control and monitor the intermodulation products of that many frequencies becomes a difficult task, and the ability to avoid intermodulation in the audio band is uncertain.
MMS MCM is subject for further research in the future.

Fig. 8 Multiple Master Slave Multi Carrier Modulation block diagram.



7. CONCLUSION

When using Multi Carrier Modulation (MCM) in switch-mode audio power amplifiers, it is possible to lower the switching frequency amplitudes compared with conventional switch-mode audio power amplifiers. Analytical expressions for the logic operators used in MCM are derived and evaluations show a 6 dB reduction in switching frequency amplitudes. Measurements on a Master-Slave Multi Carrier Modulation (MS MCM) prototype board indeed show reduced switching frequency amplitudes, and THD across the audio band is below 1% at 55 W output power open loop. THD of the MS MCM amplifier is highly affected by the frequency of the master clock, so it is important to choose this frequency with great care. The MS MCM topology could be a good choice in applications where strict EMI demands apply.

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A. FULL P_{AND} EXPRESSION

$$
\begin{aligned}
P_{AND} =& P_{sw1}P_{sw2} \\
=& k^2 && \text{(kk)} \\
&+2kMH\cos(y) && \text{(k(A1+A2))} \\
&+(MH)^2\cos^2(y) && \text{(A1A2)} \\
&+2MH\cos(y)\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw2}) && \text{(A1B2)} \\
&+2MH\cos(y)\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw1}) && \text{(A2B1)} \\
&+2MH\cos(y)\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw2}+ny) && \text{(A1C2)} \\
&+2MH\cos(y)\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw1}+ny) && \text{(A2C1)} \\
&+2kH\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\left[\cos(mx_{sw1})+\cos(mx_{sw2})\right] && \text{(k(B1+B2))} \\
&+4H^2\left[\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw1})\right]\cdot\left[\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw2})\right] && \text{(B1B2)} \\
&+4H^2\left[\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw1})\right]\cdot \\
&\left[\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw2}+ny)\right] && \text{(B1C2)} \\
&+4H^2\left[\sum_{m=1}^{\infty}\frac{\mathrm{J}_0(m\pi M/2)}{m\pi/2}\sin(m\pi/2)\cos(mx_{sw2})\right]\cdot \\
&\left[\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw1}+ny)\right] && \text{(B2C1)} \\
&+2kH\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\left[\cos(mx_{sw1}+ny)+\cos(mx_{sw2}+ny)\right] && \text{(k(C1+C2))} \\
&+4H^2\left[\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw1}+ny)\right]\cdot \\
&\left[\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\mathrm{J}_n(m\pi M/2)}{m\pi/2}\sin(m\pi/2+n\pi/2)\cos(mx_{sw2}+ny)\right] && \text{(C1C2)}
\end{aligned}
$$

B.7 Investigation of switching frequency variations in self-oscillating class D amplifiers

127th AES Conv., 2009, New York, USA, linked to all chapters

Investigation of switching frequency variations in self-oscillating class D amplifiers

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ABSTRACT

Class D audio amplifiers have gained significant influence in sound reproduction due to their high efficiency. However the switching nature of these amplifiers causes high frequent disturbance also known as electromagnetic interference (EMI). Knowledge of such couplings between class D audio amplifiers and their surroundings are of great importance with respect to audio performance, government regulations among others. A commonly used control method known as self-oscillation possess new challenges, when considering the EMI of the class D audio amplifier. These properties arise because the carrier is no longer kept at a fixed frequency. The effects of a none fixed carrier cause a falling switching frequency as the modulation index is increased. Most research on this subject uses however small signal models, and do not investigate the switching frequency dependency on the reference frequency. This is very unfortunate as small signal models do not necessarily represents the dynamics of class D audio amplifiers very well. Furthermore is investigation of the switching frequency dependency on the reference frequency lacking. It is thus the wish of this paper to give a deeper understanding of the switching frequency dependency on modulation index and reference frequency. The mathematical difficulties of obtaining a large signal model of a class D audio amplifier are outlined, and simulations together with prototyping on a 50 W amplifier providing an Total Harmonic Distortion (THD) of 0.1 % are used to map variations in the switching frequency. Spectrums have been measured with high accuracy, and very good compliance with simulation results are observed.

1. INTRODUCTION

Pulse Width Modulation (PWM) is a very well known and wide spread method of converting energy from a source to a load.

The field of power electronics covers numerous applications driving a switching element like a transistor into its saturation region or completely close it. A very special application is the reproduction of content material of audio sources. The final load in this application - the human ear - is a high quality demanding sensor. It can cover a wide range of levels (around 120 dB), detect even small perturbations like 0.01 distortion and cover a broad range of different signal speeds (20 Hz to 20 kHz). Above that frequency band, another engineering discipline comes into play: electromagnetic compatibility. The purpose of this qualifying variety is to allow the reproduction of content material for technical listeners, like radio receivers, TV receivers, radio communication and wireless steering and controlling applications. In terms of switch-mode audio power amplifiers the frequency ranges above the human ears sensibility range becomes of interest, because it can disturb the above mentioned applications and – when having acloser look at radio receivers – the high frequent content can even disturb the reception of its own input signal.

2. PRIOR ART

It is believed that one publication exits, which describes the One of the most common equations used to describe the switching frequency dependency on modulation index is

$$f_{Sw}(M) = \frac{V_S}{4}\frac{1-M^2}{\tau_{Int}V_{Hyst}} \quad (1)$$

where V_S power supply, $M = \frac{V_{Ref}}{V_S}$, V_{Hyst} (modulation index), V_{Hyst} hight of hysteresis windows and τ integration time constant. The equation can among others be found in [1], [2] and [4]. It is evident from (1), that the switching frequency falls for increasing modulation index, cursing a degraded carrier and thus reduce the overall amplifier performance. This is the reason why the modulation index is normally limited to 0.8 in slide mode control class D amplifiers.

(1) can be extended to include the loop propagation delay, t_d. An example of this is found in [1] yielding

$$f_{Sw}(M) = \frac{V_S}{4} \frac{1-M^2}{\tau_{Int} V_{Hyst} + \frac{1}{2} t_d V_S (1+M^2)} \quad (2)$$

Mikkel Høyerby has also derived an expression including the loop propagation delay, but using the duty cycle D instead of the modulation index. This is found in [3], and also shows that the switching frequency travels towards as the duty cycle is increase e.g. as the modulation index is increased.

For comparison is (1) and (2) is plotted using an idle switching frequency of 300 kHz, $\tau_{Int} = 55.56s$, $V_{Hyst} = 450mV$, $t_d = 100ns$ and $K_{Fb} = \frac{1}{8}$. Note that these parameters matches with the ones of the developed prototype as presented later on in this paper[1].

From Figure 2 on page 2 is it seen that an loop propagation delay lowers the switching frequency at low modulation indexes. Further more is the general assumption stressed ones more, that the switching frequency falls for increasing modulation index.

The main drawback of (1) and (2) is that they relay on small signal models linearized around the modulation index. Such models are thus not true AC-models, and provided an poor basis for investigating audio amplifiers. In the following section will illuminate the problems of deriving a true AC-model of class D audio amplifiers.

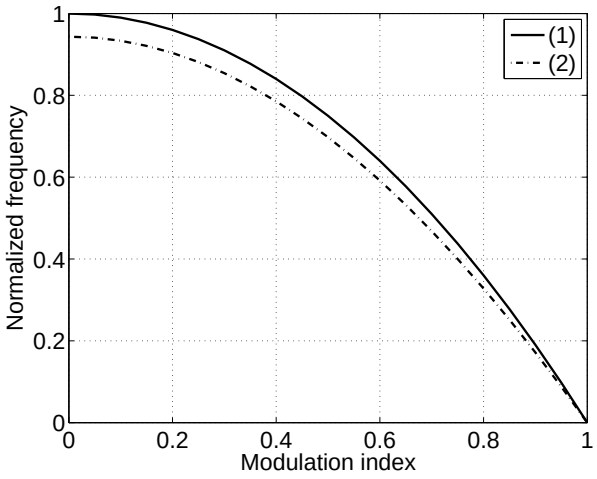


Fig. 1: Normalized switching frequency.

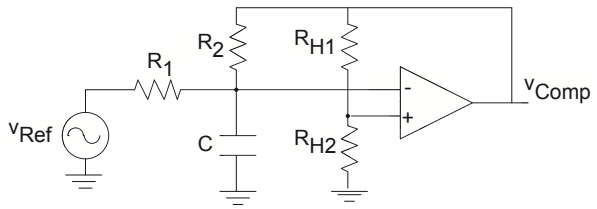


Fig. 2: Astable Integrating Modulator (AIM) audio amplifier without output filter.

3. AC-MODEL

[1] See for instance Table 1 on page 6.

One of the most basic class D audio amplifiers is the Astable Integrating Modulator (AIM) topology, which is patented in [6]. An realization of the AIM amplifier are presented in Figure 3 on page 2, where the output filter has been omitted. Notice that the comparator can be modeled to include the power stage if necessary. However in order to investigate the switching nature of the AIM amplifier can feedback from the comparator easily be assumed.

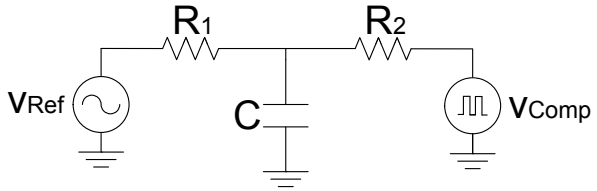


Fig. 3: Proposed AC-model.

An AC-model of the AIM amplifier is obtained by replacing the comparator with a voltage source generating pulses according to the PWM methodology. The model can be seen in Figure 3 on page 3. Notice that R_{H1} and R_{H2} can be omitted for now as these just determines the hight of the hysteresis window. The AIM amplifier will switch each time the voltage across the capacitor becomes equal to the hight of the hysteresis window [2]. This thus yields the equation

$$V_{Hyst}(s) = \frac{1}{R_1Cs+1}v_{In}(s) + \frac{1}{R_2Cs+1}v_{Comp}(s) \qquad (3)$$

[5]

Converting (3) to the time domain requires two well-known operations. These are the responses of a sine wave and a step function to a first order filter. The response of a step is an exponential function, while the response of a sine wave will be a sine wave. The later assumes that the frequency of the sine wave is well below the cut off frequency of the first order filter. Grouping constants one thus obtain an expression of the form

One thus obtain

$$k = sin(at) + e^{bt} \qquad (4)$$

[2]For this derivation will the loop propagation delay be omitted.

In (4) is k a constant with unit voltage, while a and b are real numbers.

(4) might look like a fairly simple equation. It is however the authors believe, that no general solution exists to this equation. This stresses the complex nature of obtaining an AC-model of a slide mode controlled class D audio amplifier. Because of this will the attention now be turn to results obtained through simulations.

4. SIMULINK SIMULATIONS

Simulations have been preformed using the Simulink model of Figure 4 on page 4. Further more has an FFT-function been written in Matlab allowing for instigation of switching frequency variations. Figure 4 on page 4 contains the comparator in which the propagation time delay is included, an output filter, a P regulator using feedback taking before the output filter and an integrator in the forward path securing slide mode control.

4.1. Spectrum simulations

The switching node output spectrum obtained by simulation are shown in Figure 5.1 on page 7. Starting out with an relatively small modulation index of 0.1 as shown in Figure 5(a) on page 4, can the switching frequency and its harmonics clear be identified. At modulation index 292 is the switching frequency identified to be 293 kHz, which is an reduction of 7 kHz comparing with the idle switching frequency of 300 kHz. Increasing the modulation index to 0.3 causes an drop in switching frequency of 18 kHz. One could argue, that these observed fall in switching frequency are relatively small (6 % drop at M = 0.3). However increasing the modulation index to 0.6 as seen on Figure 5(c) on page 4 clear one of the main problems by using sliding mode control.

4.2. Switching frequency

Using Figure 4 on page 4 has a surface plot been produced, which maps variations in switching frequency as function of modulation index and reference frequency. The plot can be seen in Figure 4.2 on page 5. Note that the plot only considers reference frequencies between 14 kHz and 20 kHz, while the modulation index is limited to the interval 0.1-0.5. In the script determining the switching frequency is the tracking done by identifying the highest peak in the spectrum above the reference

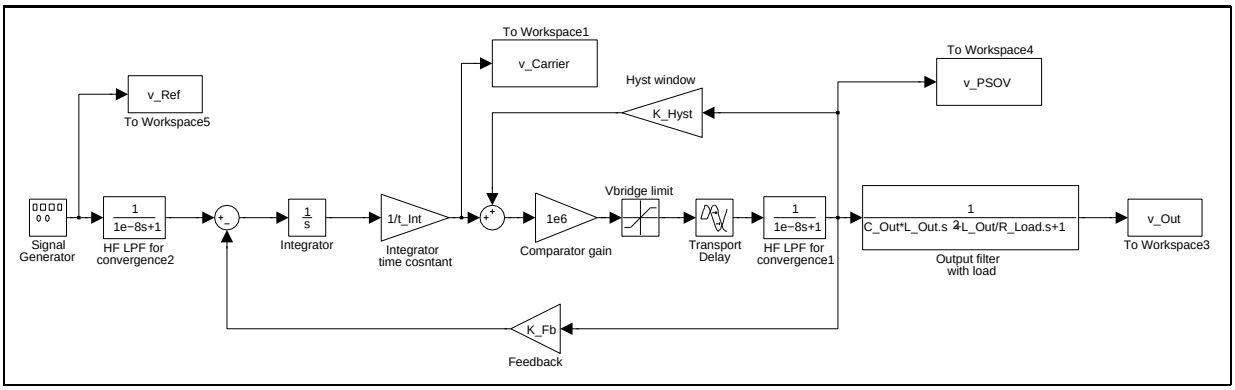
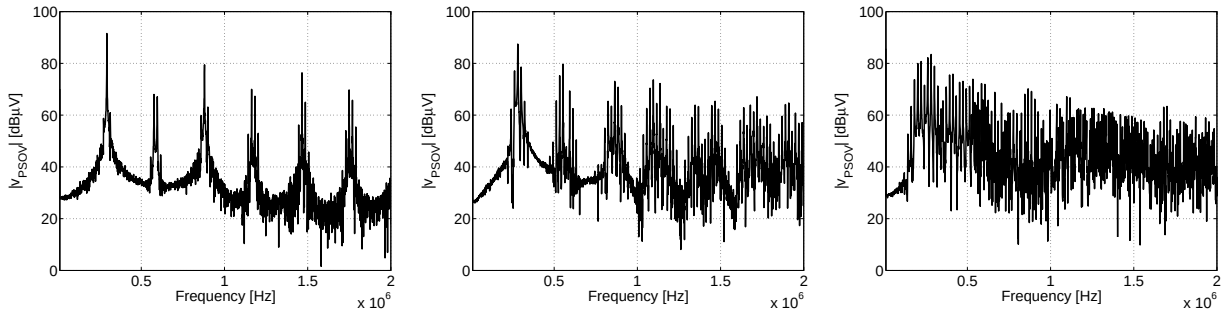


Fig. 4: Simulink simulation model.



(a) Modulation index = 0.1 (b) Modulation index = 0.3 (c) Modulation index = 0.6

Fig. 5: Simulated spectrums using different modulation indexes. All measurements are performed with an 10 kH reference signal.

frequency.

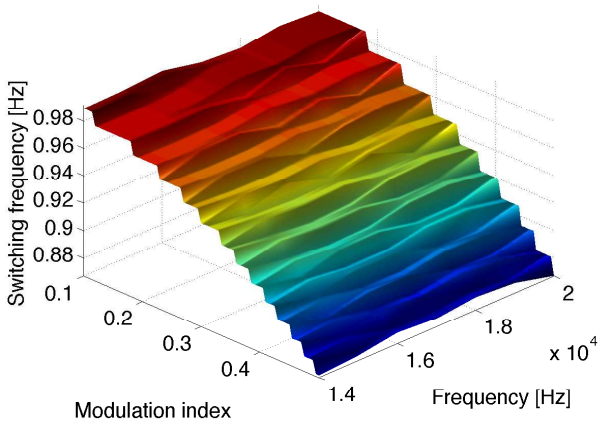


Fig. 6: Surface plot of normalized switching frequency.

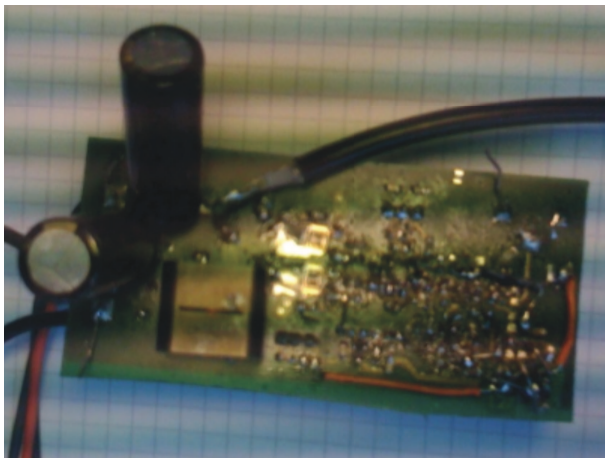


Fig. 7: Developed prototype.

An clear and important conclusion of Figure 4.2 on page 5 is that the switching frequency is independent of the reference frequency. This comply very well with the prior arts at presented in Section 2.

5. VERIFICATION BY PROTOTYPING

Experimental measurements are performed on a 50 W self-oscillating class D audio amplifier with an rated Total Harmonic Distortion of 0.1 %. The prototype can be seen in Figure 5 on page 5, while Table 1 on page 6 collects the key parameters of the prototype. Note that all measurements are performed with an load of 4 Ω. THD over power are presented in Figure 5 on page 5, and it is the authors believe that reasonable performance are obtained.

5.1. Spectrum measurements

Spectrum measurements have been divided into 2 two main parts. The first part considers the switching frequency dependency on modulation index, while the second part treats the influence of the reference frequency. All spectrum measurements are performed with a Rohde & Schwarz EMI Test Receiver.

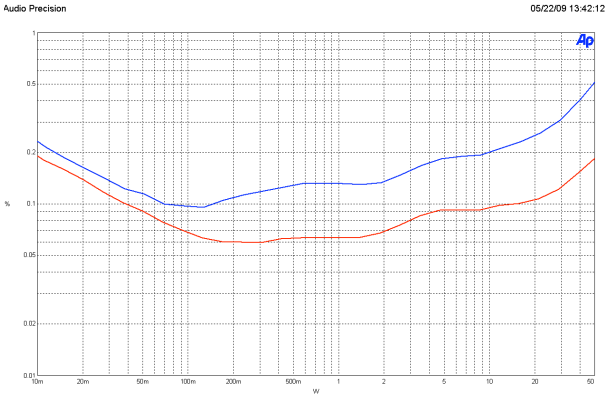


Fig. 8: THD vs power (blue 1 kHz and red 6.65kHz).

Switching frequency (idle)	Supply	THD	Gain
300 kHz	$\pm$30 V	0.1%	8

Table 1: Key parameters of prototype.

Figure 5.1 on page 7 shows the switching node output spectrum of modulation index 0.1, 0,3 and 0.6. Remembering that the idle switching frequency is 300 kHz one observe a drop in switching frequency of 2.6 kHz at modulation index 0.1. As expected does the reduction in switching frequency continue yielding a drop of 18.4 kHz at modulation index 0.3. Finally is the carrier such degraded at modulation index 0.6 that the switching frequency drowns in its sidebands.

5.2. Switching frequency measurements

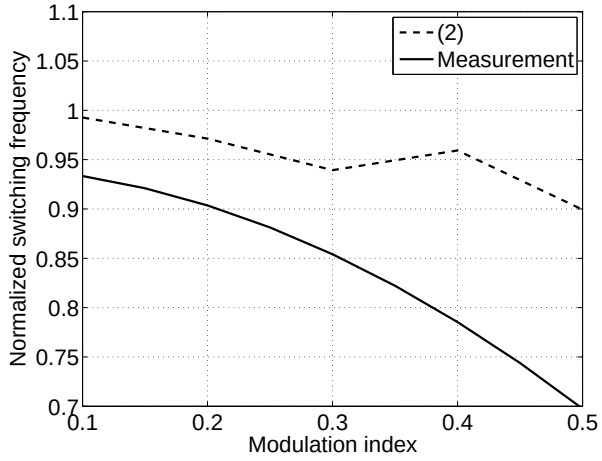


Fig. 11: Comparison of switching frequency obtained by (2) and measuring. The measurement are performed with 10 kHz reference signal.

6. CONCLUSION

It has been shown that the switching frequency of self oscillating class D audio amplifiers is independent of the reference frequency. Further more is it concluded, that the spectrum of self oscillating class D audio amplifier deviates significantly from the one of fixed frequency amplifier. This is seen by the sidebands, which is not of the same magnitudes. At high modulation indexes is the switching frequency no longer clearly defined and only spectral distribution of peaks are observed. In order to improve EMI design would it be desirable to have a model of self oscillating class D audio amplifiers spectrum. However as shown in this paper are such models not easily obtained.

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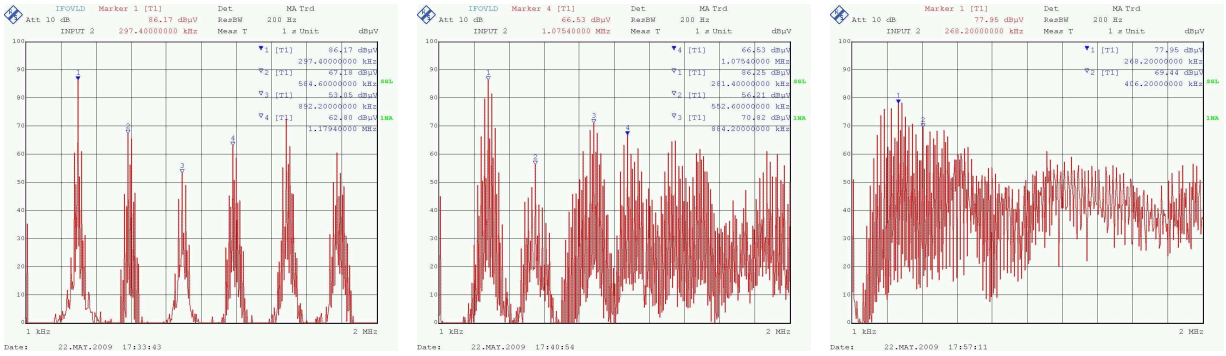
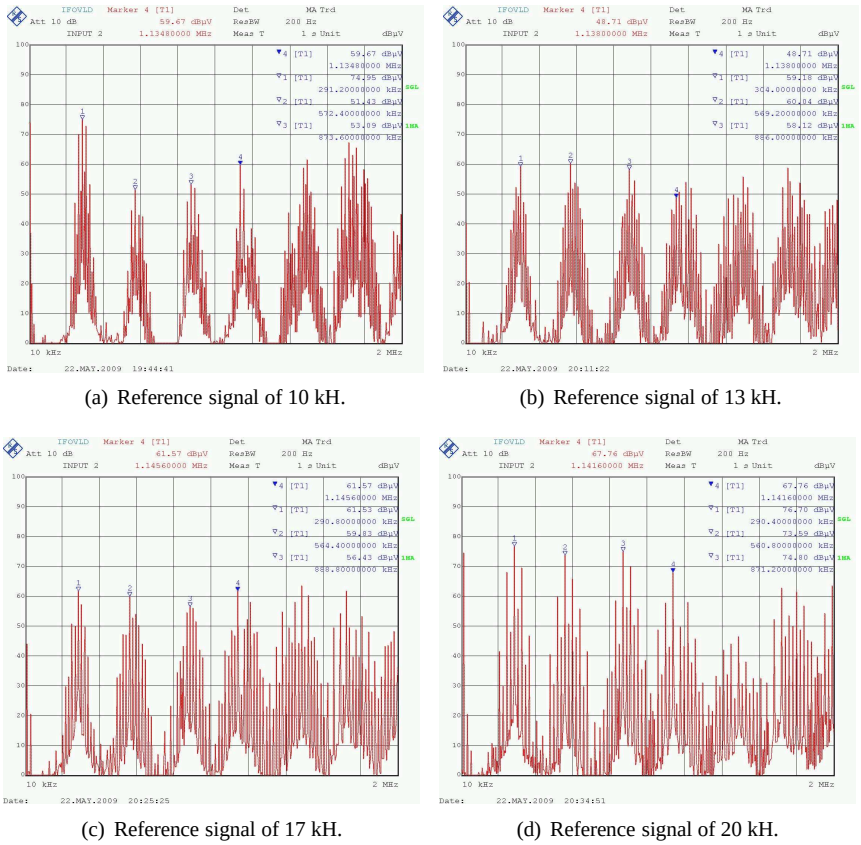


(a) Modulation index = 0.1 (b) Modulation index = 0.3 (c) Modulation index = 0.6

Fig. 9: Spectrum using different modulation indexes. All measurements are performed with an 10 kH reference signal.



(a) Reference signal of 10 kH. (b) Reference signal of 13 kH.

(c) Reference signal of 17 kH. (d) Reference signal of 20 kH.

Fig. 10: Spectrum using reference frequencies. All measurements are performed with M = 0.2.

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B.8 Modeling Distortion Effects in Class-D Amplifier Filter Inductors

128th AES Conv., 2010, London, England, linked to all

Audio Engineering Society

Convention Paper

Presented at the 128th Convention
2010 May 22–25 London, UK

Modeling Distortion Effects in Class-D Amplifier Filter Inductors

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ABSTRACT

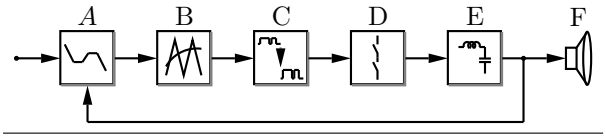
Distortion is generally accepted as a quantifier to judge the quality of audio power amplifiers. In switch-mode power amplifiers various mechanisms influence this performance measure. After giving an overview of those, this paper focuses on the particular effect of the nonlinearity of the output filter components on the audio performance. While the physical reasons for both, the capacitor and the inductor induced distortion are given, the practical in depth demonstration is done for the inductor only. This includes measuring the inductors performance, modeling through fitting and resulting into simulation models. The fitted models achieve distortion values between 0.03 % and 0.2 % as a basis to enable the design of a 200 W amplifier.

1. INTRODUCTION

Even other measures, like intermodulation distortion are more in depth measures, a distortion figure is the fundamental starting point to distinguish amplifiers. It reveals the noise level of the amplifier and provides the basics for more advanced tests as described in [1]. As the desired figures necessitate the precision of signal levels to be in the µV range, it makes sense to break the origin of the distortion mechanisms down into the various parts of an amplifier. For linear audio power amplifiers this was done in [2]. For the more efficient switch-mode audio power amplifiers a number of publications covered these mechanisms. The different stages of these amplifiers can be broken down according to the block diagram in figure 1.

The blocks and their distortion sources are:

Fig. 1 Block diagram of a switch-mode audio power amplifier



A. **Input and Control** The distortion is dominated in the input stage and regulator by either the used operational amplifier for time-continuous inputs and specified in their datasheets or, for time-discrete inputs, by the sampling process [3, 4, 5] or clock induced noise level [6].

B. **Modulator** The modulator induced distortion is mainly based on linearity of the carrier [7].

C. **Level Shifter** The impact of the level shifter on the audio performance has not been researched up to now and leaves room for further research.

D. **Power Stage** The power stages influence on the audio performance has been described in [8].

E. **Output Filter** This paper is dealing with the influence of the output filters properties on linearity of the amplifier.

F. **Loudspeaker** The transducers influence on audio performance has been described in [9] and broken down into single mechanisms in [10]

2. OUTPUT FILTER

The output filter is required to suppress the energy, which is used to operate the output stage in an efficient mode. The frequency of this energy is beyond the audible frequency range [11] and generally causing trouble in electromagnetic compatibility. The insertion of the filter is solving those, however generating audible effects and losses, which leads to the tradeoffs visualized in figure 2.

A simplified circuit diagram of the output filter is shown in figure 3 and its transfer function is given in 2.1 where V_{ps} denotes the output voltage of the power stage and V_{out} the output voltage of the amplifier, which is applied across the speaker terminals.

Fig. 2 Tradeoffs in output filter design.

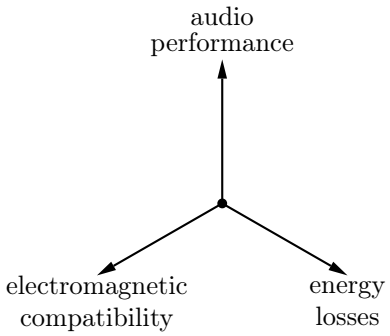
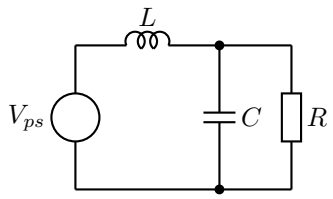


Fig. 3 Circuit of an output filter for an audio power amplifier.



Equation 2.1 Transfer function of filter in figure 3.

$$\underline{H}\left(\underline{s}\right) = \frac{\underline{V}_{out}}{\underline{V}_{ps}} = \frac{1}{1 + \underline{s}\frac{L}{R} + \underline{s}^2 LC}$$

This paper is specifically investigating the nature and impact of the output filter on the audio performance. Therefore both filter components, the capacitors and the inductors physical properties are investigated in this section.

2.1. Capacitor

Capacitance C is defined as stored charge q per voltage V 2.2.

Equation 2.2 Definition of capacitance.

$$C = \frac{q}{V}$$

Applying Gauss Law to the charge allows itemiza-

tion into electrical field $\vec{E}$ with vacuum permittivity ε_0 and displacement vector $\vec{P}$ via charge density ϱ and electric displacement $\vec{D}$ 2.3.

Equation 2.3 Gauss Law.

$$q = \iiint \varrho \, \delta Vol = \oint_A \vec{D} \, \delta\vec{s} = \oint_A \left(\varepsilon_0 \vec{E} + \vec{P}\right) \, \delta\vec{s}$$

The denominator of 2.2 can be expressed by Farradys law 2.4.

Equation 2.4 Farradays Law.

$$V = \oint_s \vec{E} \, \delta\vec{s}$$

Through both of those physical principles, the definition of capacitance can be rewritten as in 2.5

Equation 2.5 Definition of capacitance taking Gauss and Farradays Law into account.

$$C = \underbrace{\frac{\oint_A \varepsilon_0 \vec{E} \, \delta\vec{s}}{\oint_s \vec{E} \, \delta\vec{s}}}_{\text{linear part}} + \underbrace{\frac{\oint_A \vec{P} \, \delta\vec{s}}{\oint_s \vec{E} \, \delta\vec{s}}}_{\text{polarization dependent}}$$

The nonlinearity of the capacitor is therefore originated in the polarization defined through the electric susceptibility χ 2.6 for anisotropic dielectric materials [12].

Equation 2.6 Linear and nonlinear parts of displacement vector.

$$\frac{\vec{P}}{\epsilon_0} = \underbrace{\sum_j \chi^{(1)}_{ij} \vec{E}_j}_{\text{linear susceptibility}} + \underbrace{\sum_{jk} \chi^{(2)}_{ijk} \vec{E}_j \vec{E}_k}_{\text{Pockels Effect}} + \underbrace{\sum_{jkl} \chi^{(3)}_{ijkl} \vec{E}_j \vec{E}_k \vec{E}_l}_{\text{Kerr Effect}}$$

This reveals the Pockels effect to be responsible for second order nonlinearities and the Kerr Effect to be the reason for third order effects.
For ferroelectric materials, the description of nonlinearity is getting somewhat more complicated, as the displacement vector has a hysteretic dependency on the electrical field. Theses hysteretic curves have been shown quantitativelty in [13].

2.2. Inductor

The equivalent physical derivation of the reasons for the nonlinearity of the inductor start with the definition of inductance 2.7 in dependency on magnetic flux Φ and electrical current I.

Equation 2.7 Definition of inductance.

$$L = \frac{\phi}{I}$$

Through Gauss Law of Magnetism Φ is expressed in 2.8 as a function of magnetic field $\vec{H}$ and the magnetization $\vec{M}$ with the aid of the permeability in vacuum via the magnetic flux density $\vec{B}$.

Equation 2.8 Gauss Law of Magnetism.

$$\Phi = \oint_S \vec{B} \, \delta\vec{A} = \oint_S \mu_0 \left(\vec{H} + \vec{M}\right) \, \delta\vec{A}$$

Through Amperes Circuit Law the current is expressed as a function of the magnetic field $\vec{H}$ as in 2.9.

Equation 2.9 Amperes Circuit Law.

$$I = \oint_C \vec{H} \, \delta\vec{l}$$

Taking both of those two laws into account, the definition of the inductance is rewritten in 2.10.

Equation 2.10 Definition of inductance taking Gauss and Amperes Law into account.

$$L = \underbrace{\frac{\oint_S \mu_0 \vec{H}\,\delta\vec{A}}{\oint_C \vec{H}\,\delta\vec{l}}}_{\text{linear part}} + \underbrace{\frac{\oint_S \mu_0 \vec{M}\,\delta\vec{A}}{\oint_C \vec{H}\,\delta\vec{l}}}_{\text{polarization dependent}}$$

The polarization dependent part $\vec{M}$ is not following the BH-curve, which has been numerically fitted in [14], but rather the Rayleigh Loop [15] which has been extended to symmetry of the loop as only limitation, by [16] as described in [17]. While the current I is linear dependent on the magnetic field $\vec{H}$, its relation to the magnetic polarization $\vec{M}$ contains higher order terms. This nonlinear dependency of magnetization on the magnetic field is covered by the high order terms in 2.11 by the named references.

Equation 2.11 Peterson relation.

$$\vec{M} = \chi\vec{H} + \mu_0 a_{11}\vec{H}^2 + \mu_0\left(a_{12} + a_{30}\right)\vec{H}$$

The coefficients a_{11}, a_{12} and a_{30} are the first Peterson Coefficients, describing both, the nonlinearity of the magnetization curve and ensure the fulfillment of the energy conservation law. As shown in [17] the lost energy in the magnetic field corresponds with the hysteresis losses in the material. Also in [17] the Peterson Coefficients got used to quantitatively describe the nonlinearity of the magnetic flux density for single sinusoidal tones as well as double sinusoidal tones and their intermodulation products.
For the choice of output filter inductors for switchmode power amplifiers those coefficients are of quantitative interest. However the Peterson Coefficients where derived for small field excitations only, whereas the linearity of an amplifier is affected by the large signal behaviour of the magnetization loop. Therefore the next logical step is to measure the large signal behaviour of inductors and use the quantized data for estimation of the impact on the audio performance. This is done in the next section.

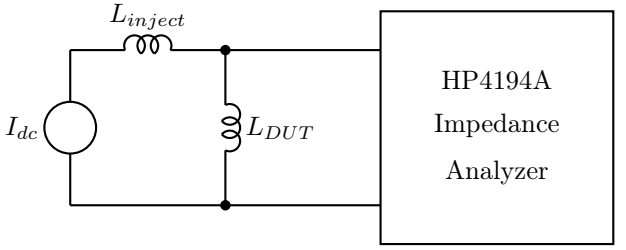
3. MODELING

Section 2 showed the duality between capacitor and inductor in theory. Consequently the rest of the paper is dealing with one of them only, without loosing generality for the other one. It is the inductor, which is generally dominating size constraints, electromagnetic compatibility challenges and showing the most interesting saturation effects. Therefore the inductors linearity is pursued furtheron in this paper.
Through the desired power rating of an amplifier and neglect of the ripple current, the current rating of the filter inductor is given. For the following analysis of inductors, a power rating of 200 W into a 4 Ω transducer is arbitrarily chosen. This leads to a peak current of 10 A through the filter inductor. Only few technical documentations of suitable components give the dependency of inductance on the current flowing through the windings like in [18]. Therefore a measurement setup is described following, allowing to derive this curve.

3.1. Measurement Setup

To measure the linearity of the inductor, it needs to be biased with the desirable current and simultaneously measured with an impedance analyzer. If an analyzer with current bias option is not available the bias can be done externally as shown in figure 4.
Through the inductor L_{inject} the device under test

Fig. 4 Measurement Setup.



L_{DUT} is biased to the desired current level. To prevent damage on the gain phase analyzer, which is both superimposing the test signal as well as taking the measurement data, the voltage limitation of the current source shall be set below the maximum input rating of the analyzer. Otherwise a voltage leading to destruction in the input of the analyzer might occur in case the DUT fails. The purpose of the injection inductance is, to provide a high ohmic path for the measurement signal. Therefore the in-

jection inductance needs to be significantly bigger than the inductance of the DUT. Also the injection inductance needs to be more linear than the device under test. This results into a high volume consuming inductor compared to the DUT. The parameters of the injection inductor are given in table 1.

Three possible output filter inductors have been chosen based on their rating. Their main parameters are compared in table 2. The inductance curves have been captured with the above described measurement method and the results are visualized in figure 5. The inductance droop varies from less than 1 %, around 3 % up to nearly 10 % with respect to the unbiased inductance measurement.

Table 1 Design of injection inductor.

core	air gap	turns	L_{inject}
ETD59-N97	1.6 mm	32	306 µH

Table 2 Parameters of the three devices under test.

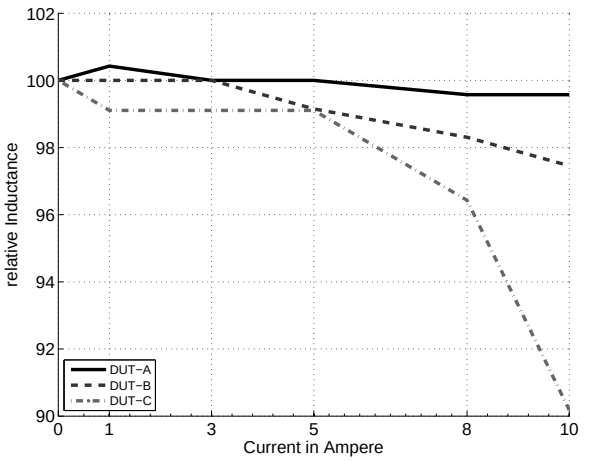
	DUT-A	DUT-B	DUT-C
nominal inductance	22 µH	10 µH	10 µH
current rating	11 A	10 A	10 A
DC resistance	11 mΩ	8.8 mΩ	17.2 mΩ
resonant frequency	9.3 MHz	41 MHz	20 MHz
boxed volume	9.2 cm^3	1.6 cm^3	2.3 cm^3
footprint area	2.3 cm^2	1.9 cm^2	3.3 cm^2
datasheet	[19]	[20]	[21]

These relative variations shall not be confused with the distortion of an amplifier. The fitting of the inductance droop to a distortion number is done in the following section.

3.2. Fitting

Through the above shown nonlinear behaviour of the inductor, equation 2.1 is getting another dependency on the inductor current as shown in 3.1.

Fig. 5 Inductance curves.



Equation 3.1 Transfer function taking nonlinearity of inductor into account.

$$\underline{H}\left(\underline{s}, \underline{I}_L\right) = \frac{\underline{V}_{out}}{\underline{V}_{ps}} = \frac{1}{1 + \underline{s}\frac{L\left(\underline{I}_L\right)}{R} + \underline{s}^2 L\left(\underline{I}_L\right) C}$$

Applying ohms law to the load impedance, removes one degree of freedom and gives 3.2

Equation 3.2 Transfer function only dependent on voltages.

$$\underline{H}\left(\underline{s}, \underline{V}_{out}\right) = \frac{\underline{V}_{out}}{\underline{V}_{ps}} = \frac{1}{1 + \underline{s}\frac{L\left(\underline{V}_{out}\right)}{R} + \underline{s}^2 L\left(\underline{V}_{out}\right) C}$$

with

Equation 3.3 Inductors dependence on signal level.

$$L = \frac{\oint\limits_S \mu_0 \vec{H}\left(\underline{V}_{out}\right)\, \delta\vec{A}}{\oint\limits_C \vec{H}\left(\underline{V}_{out}\right)\, \delta\vec{l}} + \frac{\oint\limits_S \mu_0 \vec{M}\left(\underline{V}_{out}\right)\, \delta\vec{A}}{\oint\limits_C \vec{H}\left(\underline{V}_{out}\right)\, \delta\vec{l}}$$

Taking into account, that Petersons Coefficients, which are describing the nonlinearity of the inductor,

are a series of polynoms, also the transfer function can be modeled by a series of polynoms, which is done in 3.4 up to second order for one signal frequency with the fitting coefficients α, β and γ.

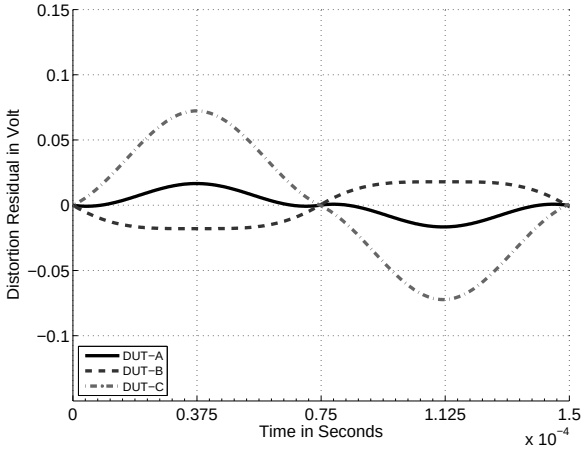
Equation 3.4 Second order fitting of transfer function.

$$\underline{H}\left(\underline{V_l}oad\right) = \alpha\underline{H}^2 + \beta\underline{H} + \gamma$$

A quantitative representation of the distortion for a 6.665 kHz sinusoidal test signal is the difference between an undistorted and a distorted signal. The undistorted signal as reference is taken from the output voltage of the signal after passing a linear filter as reference. The difference of those two voltages are known as distortion residual and for the modeled inductors shown in figures 6 and 7 for first and second order fitting respectively.

From those signals the root means square (RMS)

Fig. 6 Distortion residual for first order fitting.



values can be numerically calculated and set in relation to the RMS of the desired signal according to the definition of total harmonic distortion (THD). This leads to the distortion figures, which are the ratio between the distortion residual and the signal before the filter, as shown in table 3.

4. SIMULATION

As has been described above, the inductors influence on distortion is only one of several influences.

Fig. 7 Distortion residual for second order fitting.

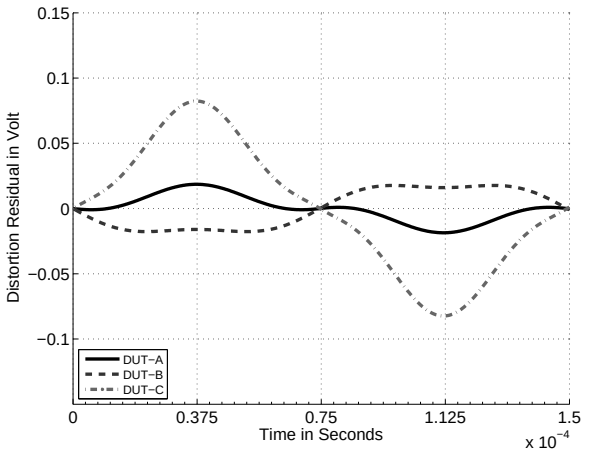


Table 3 Estimated total harmonic distortion (THD) for the modeled inductors.

	DUT-A	DUT-B	DUT-C
1st order fitting	0.034 %	0.053 %	0.165 %
2nd order fitting	0.036 %	0.053 %	0.171 %

Therefore the above model needs to enabled to connect with the other distortion mechanisms to reveal their interaction. This can be done with circuit analyzers like "GeckoCircuits". Therefore the nonlinear model of the above DUTs was simulated against their linear representations as shown in figure 8.
"GeckoCircuits" was chosen as simulation tool, because of its ability to directly deal with nonlinear passive components and its ability to process large simulation data very fast. The later property is relevant, because the distortion signal of an audio amplifier is generally very low compared to the signal. Therefore, both very precise simulation and large dynamical range of the simulator are required. In many software tools, this either leads to excess simulation time or large memory usage. "GeckoCircuits" requires neither one of them.
The simulation parameters and the duration of the simulation are given in table 4. The solver of this simulator takes all six modeled datapoints and interpolates the circuit behaviour linearly between those. The distortion residuals are shown in figures 9, 10 and 11. The simulated distortion numbers are given

Fig. 8 Simulated circuit with the three nonlinear models and their equivalent linear models.

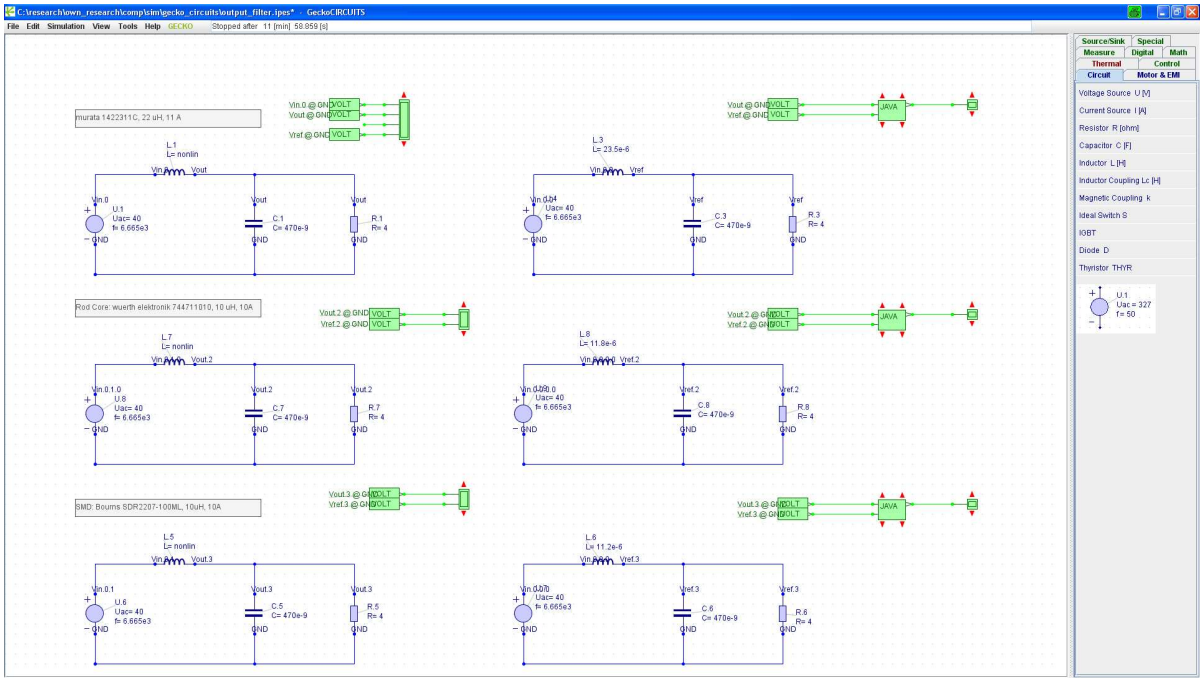


Table 4 Simulation parameters and duration.

start time	150 µs
time step	10 ps
stop time	300 µs
simulation time	≈ 12 min

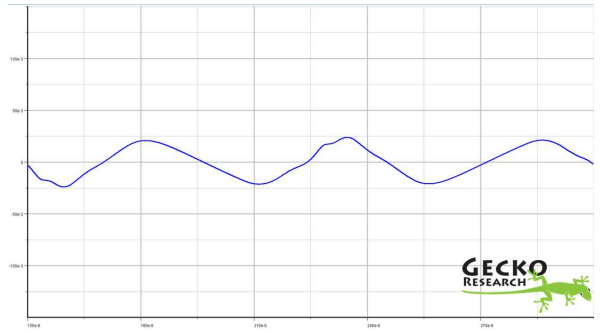
in table 5.

The distortion is slightly higher here, however showing the same tendency as in the model above.

Table 5 Estimated total harmonic distortion (THD) for the modeled inductors.

DUT-A	DUT-B	DUT-C
0.060 %	0.094 %	0.215 %

Fig. 9 Simulated distortion residual based on the above model for DUT A. (x-axis: 150 µs . . . 300 µs; y-axis: −0.150 V . . . 0.15 V)



5. CONCLUSION

With distortion being a quantitative qualifier for an amplifier as starting point, the influences on this figure where revisited here. The focus within this study is on the output filters distortion and in particular the audio degradation induced by the inductor. After reviewing the physical reasons for the nonlinearity of both, the capacitor and the inductor, a procedure for modeling the nonlinearity of the inductor was shown. By fitting the transfer function of the output filter to this nonlinearity, an estimation on

Fig. 10 Simulated distortion residual based on the above model for DUT B. (x-axis: 150 µs . . . 300 µs; y-axis: −0.150 V . . . 0.15 V)

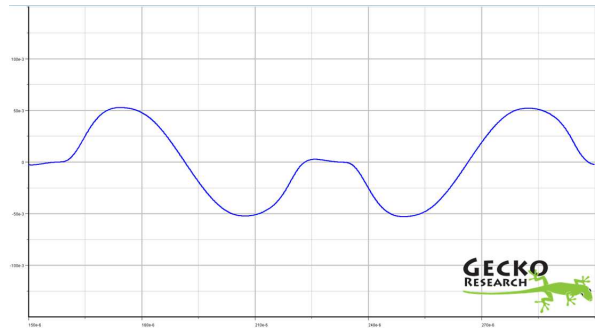
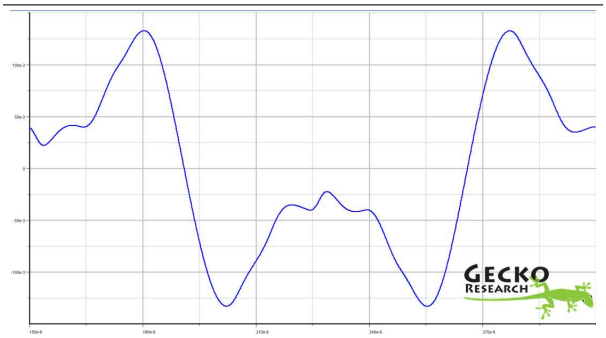


Fig. 11 Simulated distortion residual based on the above model for DUT C. (x-axis: 150 µs . . . 300 µs; y-axis: −0.150 V . . . 0.15 V)



the amount of influence on the THD from the inductors linearity was derived. Finally the modeled component nonlinearity got applied to the filter in a circuit simulator to further enable the inclusion of the modeled details on system level.
As a rule of thumb the following mapping table 6 shall enable the design engineer of Class-D amplifiers to allow an estimation of THD, when the inductance drop at the rated current is the only known parameter — which is in some cases given in inductor datasheets.

Table 6 Mapping inductance droop to the caused THD as an approximated rule of thumb.

$\frac{\Delta L}{L_0}$	1 %	3 %	10 %
approximately expected THD	0.05 %	0.10 %	0.20 %

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B.9 Electrical Load Detection Apparatus

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(19) **United States**

(12) **Patent Application Publication**

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Woelfl et al.

(54) **ELECTRICAL LOAD DETECTION APPARATUS**

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(21) Appl. No.: **12/431,368**

(22) Filed: **Apr. 28, 2009**

(30) **Foreign Application Priority Data**

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Publication Classification

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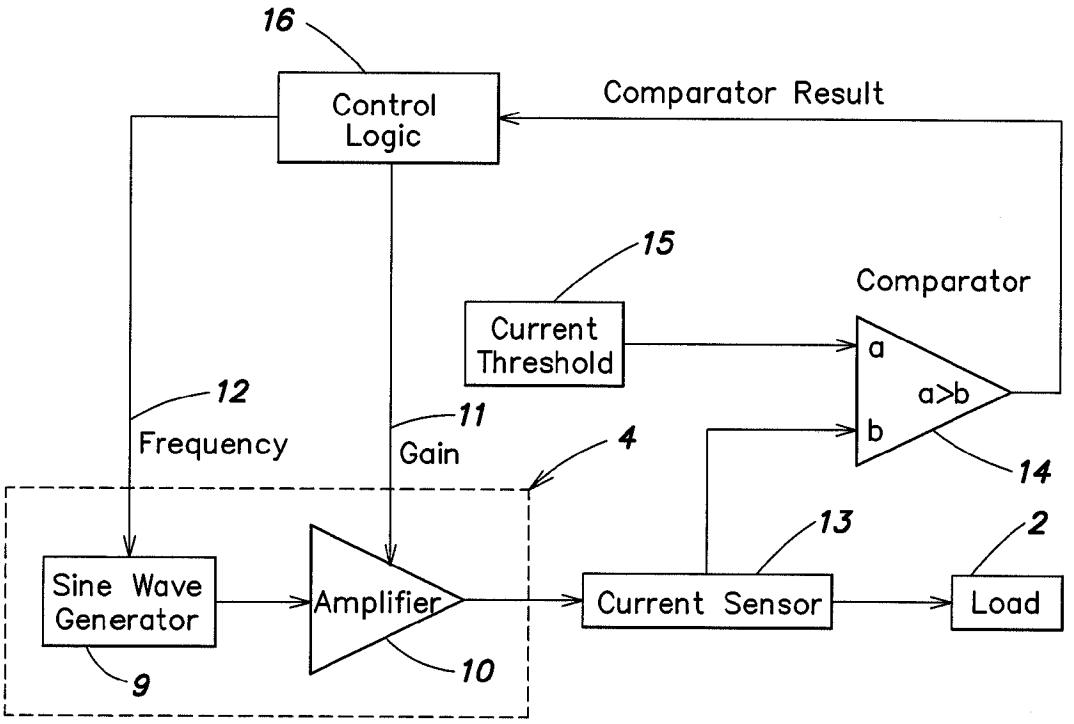
G01R 27/08 (2006.01)

(52) **U.S. Cl.** **324/691**

(57) **ABSTRACT**

A load detection technique for a load comprising multiple frequency-dependant sub-loads comprises measuring a representation of the impedance characteristic of the load; providing stored representations of a multiplicity of impedance characteristics of the load; each one of the stored representations represents the impedance of the load when at least a particular one of the sub-loads is in a fault condition; and comparing the measured representation of the current impedance characteristic of the load with each one of the stored representations and in case that the measured representation matches a stored representation, identifying the sub-load or sub-loads being in a fault condition by the corresponding stored representation.



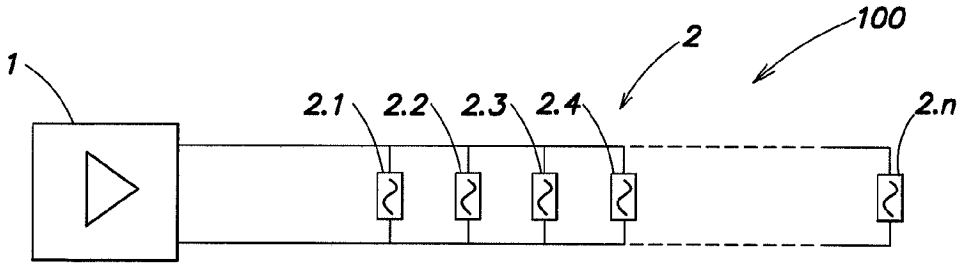


FIG. 1

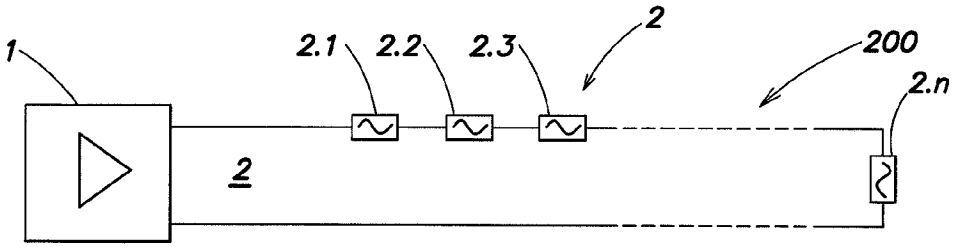


FIG. 2

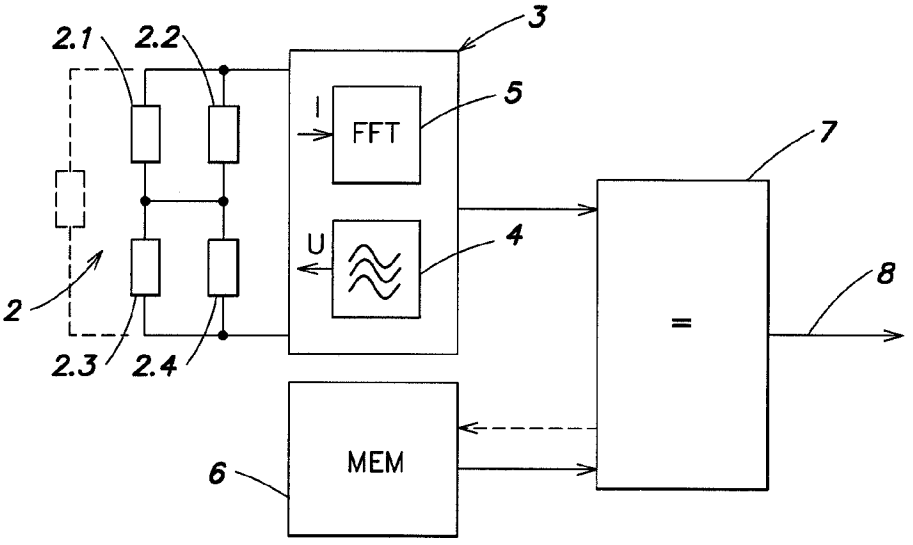


FIG. 3

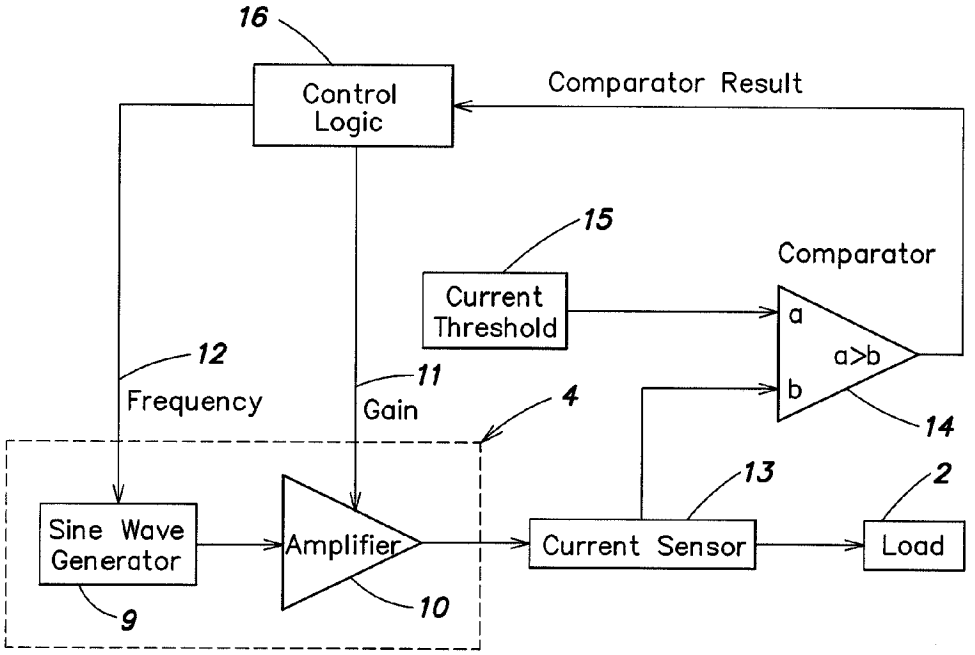

16
Control Logic
Comparator Result
15
Comparator
Current Threshold
a
a>b
b
12
Frequency
11
Gain
4
14
13
2
Sine Wave Generator
Amplifier
Current Sensor
Load
9
10

FIG. 4

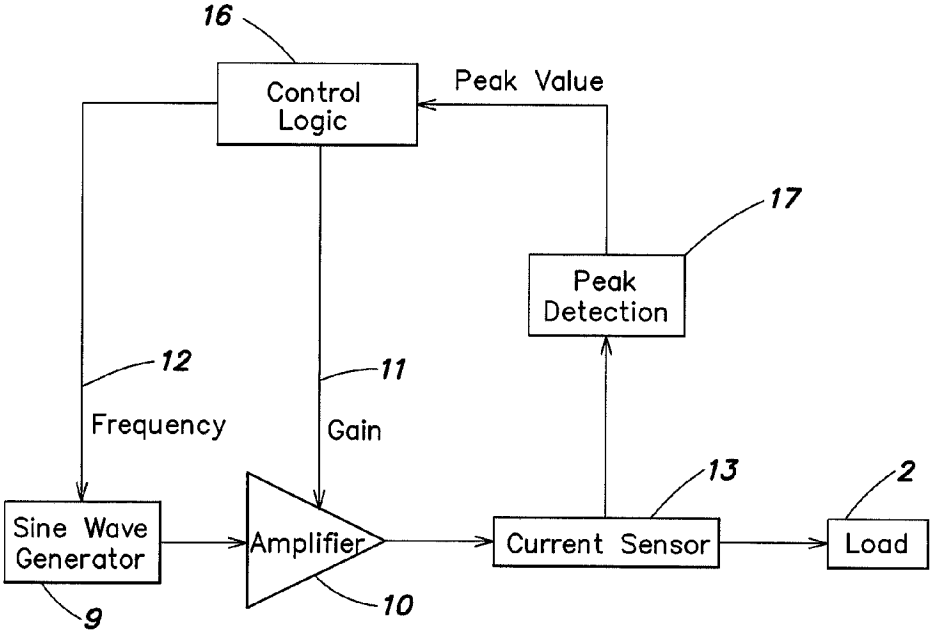

16
Control Logic
Peak Value
17
Peak Detection
12
Frequency
11
Gain
13
2
Sine Wave Generator
Amplifier
Current Sensor
Load
9
10

FIG. 5

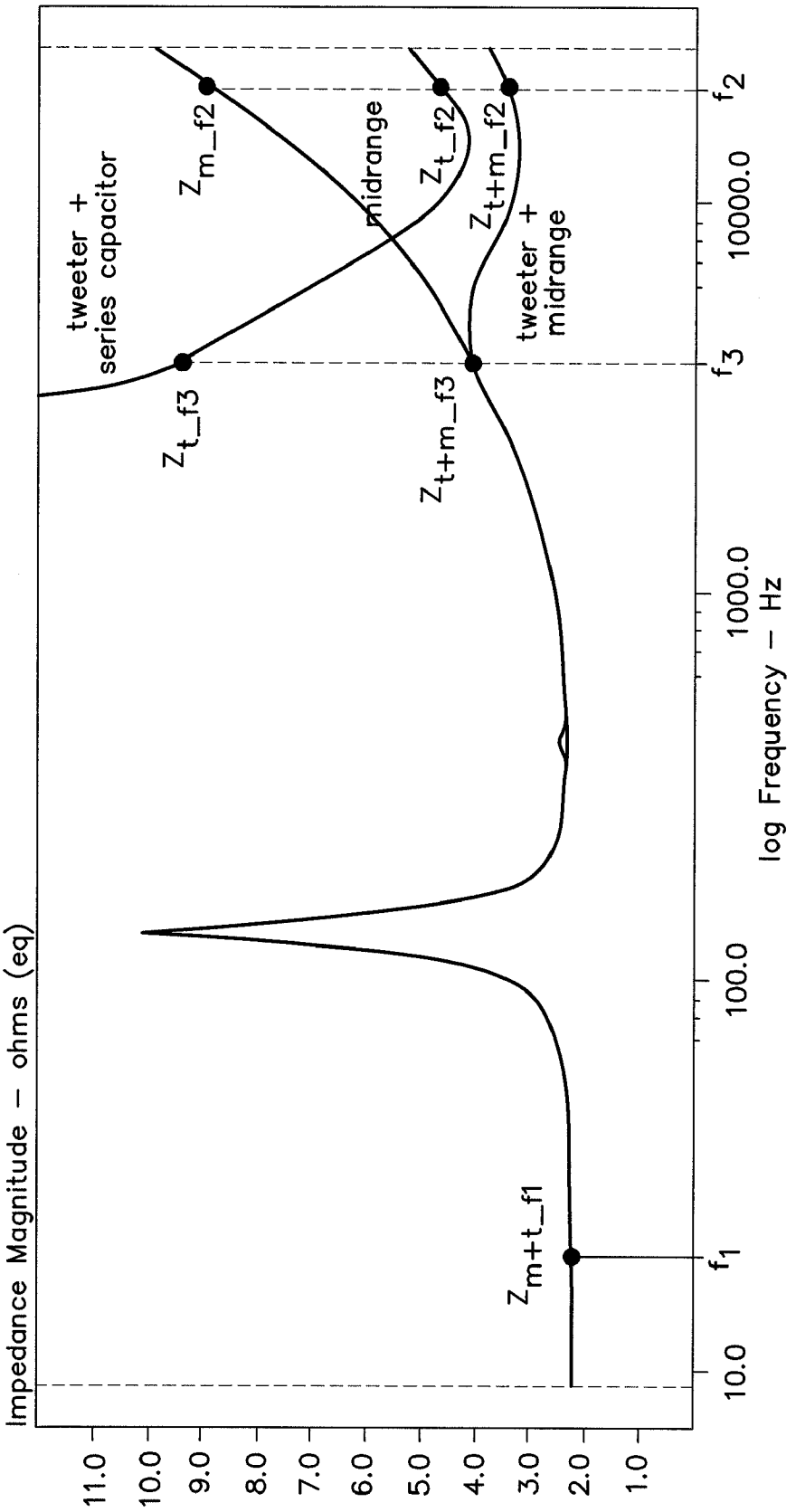

Impedance Magnitude – ohms (eq)
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
10.0
100.0
1000.0
10000.0
log Frequency – Hz
f1
f2
f3
Zm+t_f1
Zt_f3
Zm_f2
Zt+m_f3
Zt_f2
Zt+m_f2
tweeter + series capacitor
midrange
tweeter + midrange

FIG. 6

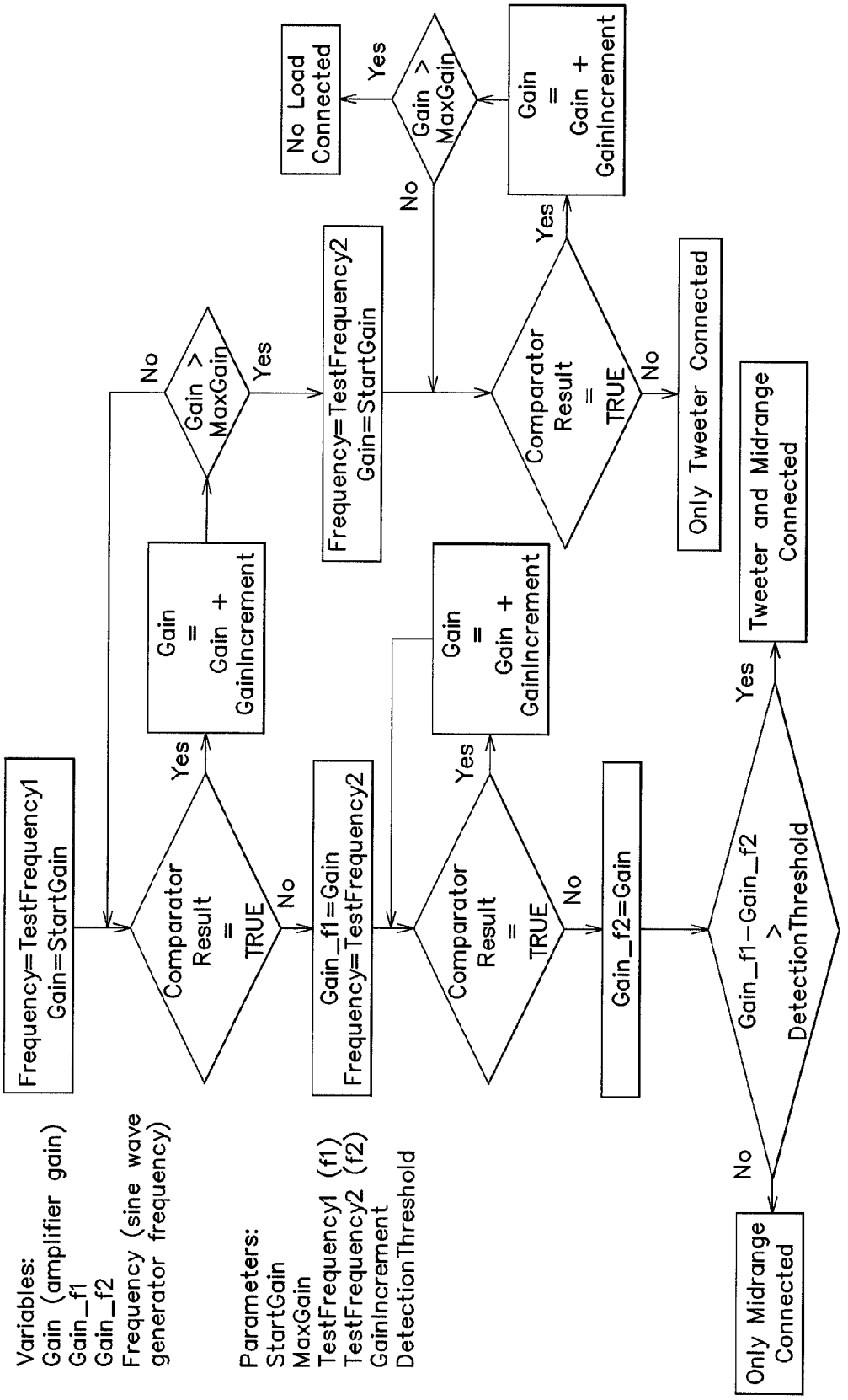

Variables:
Gain (amplifier gain)
Gain_f1
Gain_f2
Frequency (sine wave generator frequency)
Parameters:
StartGain
MaxGain
TestFrequency1 (f1)
TestFrequency2 (f2)
GainIncrement
DetectionThreshold
Frequency=TestFrequency1 Gain=StartGain
Comparator Result = TRUE
Yes
No
Gain = Gain + GainIncrement
Gain > MaxGain
Yes
No
Gain_f1=Gain Frequency=TestFrequency2
Comparator Result = TRUE
Yes
No
Gain = Gain + GainIncrement
Gain > MaxGain
Yes
No
Frequency=TestFrequency2 Gain=StartGain
Comparator Result = TRUE
Yes
No
Gain = Gain + GainIncrement
Gain > MaxGain
Yes
No
Gain_f2=Gain
Gain_f1−Gain_f2 > DetectionThreshold
Yes
No
No Load Connected
Only Tweeter Connected
Tweeter and Midrange Connected
Only Midrange Connected

FIG. 7

Gain_f1 < MaxGain	Gain_f2 < MaxGain	Gain_f1 − Gain_f2 > Detection Threshold	Tweeter Connected	Midrange Connected
NO	NO	X	NO	NO
NO	YES	X	YES	NO
YES	YES	NO	NO	YES
YES	YES	YES	YES	YES

FIG. 8

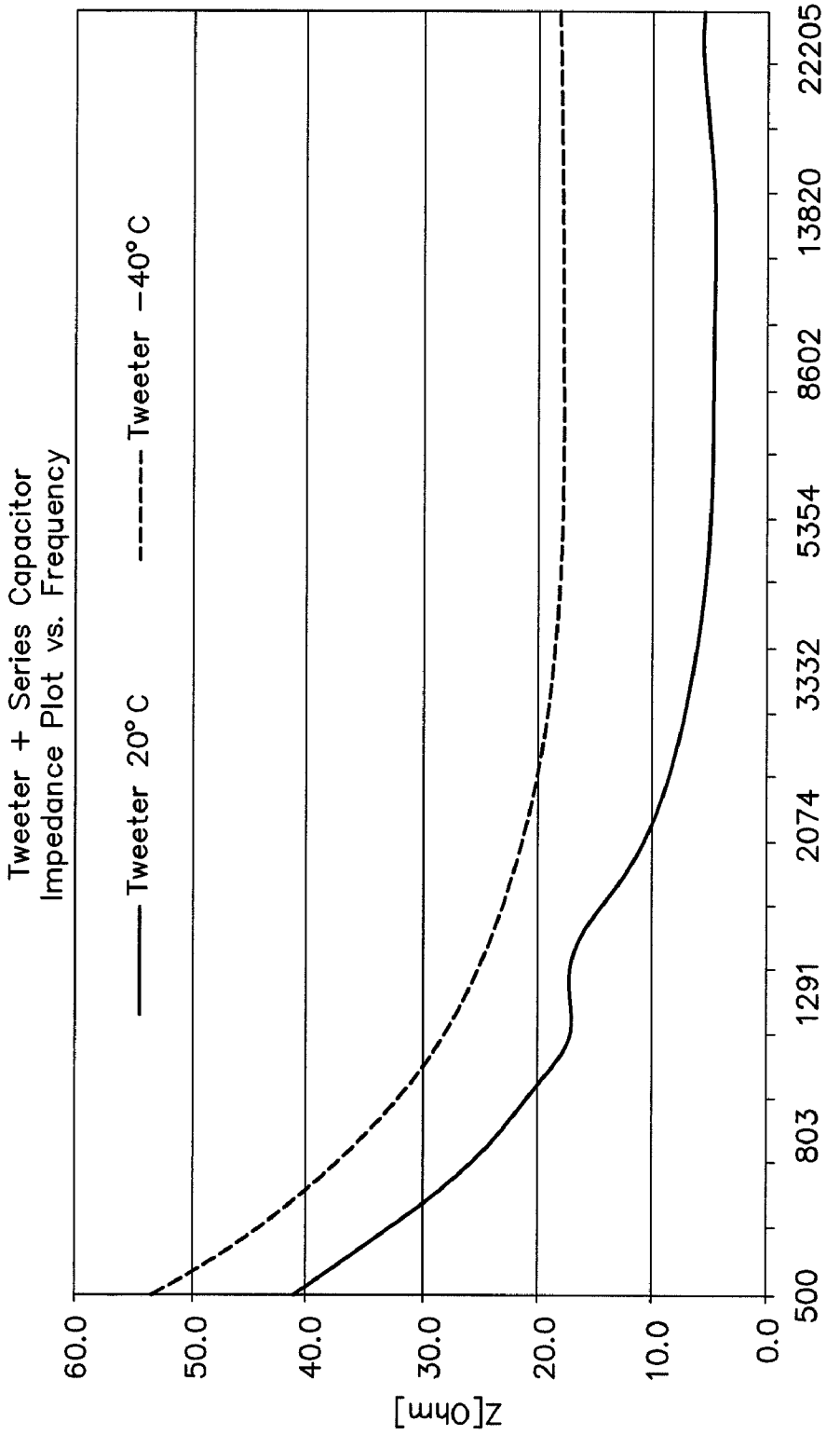

Tweeter + Series Capacitor
Impedance Plot vs. Frequency
Tweeter 20° C
Tweeter −40° C
Z[Ohm]
60.0
50.0
40.0
30.0
20.0
10.0
0.0
500
803
1291
2074
3332
5354
8602
13820
22205
Frequency [Hz]

FIG. 9

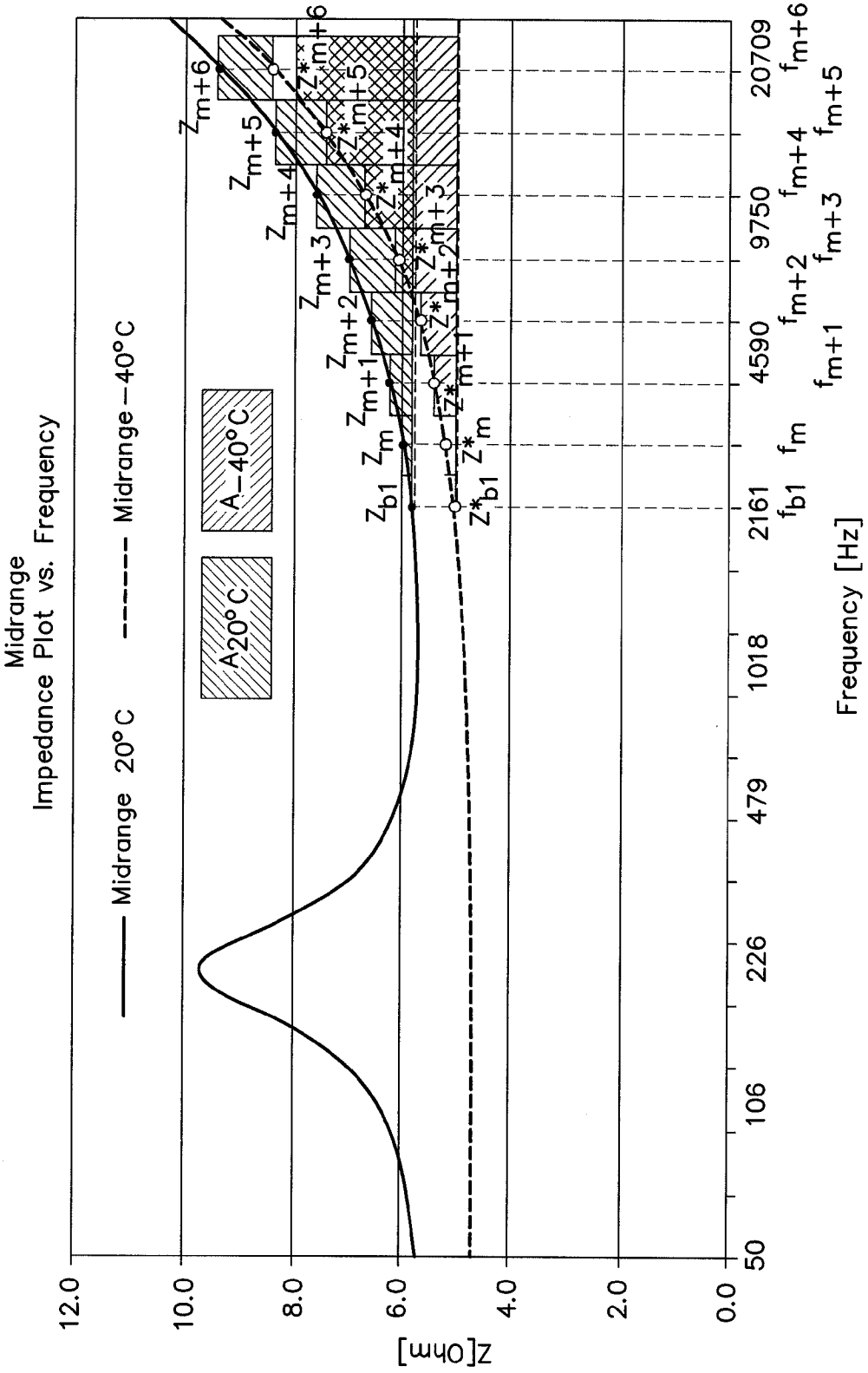

Midrange
Impedance Plot vs. Frequency
Midrange 20°C
Midrange −40°C
A20°C
A−40°C
Z[ohm]
12.0
10.0
8.0
6.0
4.0
2.0
0.0
50
106
226
479
1018
2161
4590
9750
20709
Frequency [Hz]
f_{b1} f_m f_{m+1} f_{m+2} f_{m+3} f_{m+4} f_{m+5} f_{m+6}
Z_{b1} Z_m Z_{m+1} Z_{m+2} Z_{m+3} Z_{m+4} Z_{m+5} Z_{m+6}
Z^*_{b1} Z^*_m Z^*_{m+1} Z^*_{m+2} Z^*_{m+3} Z^*_{m+4} Z^*_{m+5} Z^*_{m+6}

FIG. 10

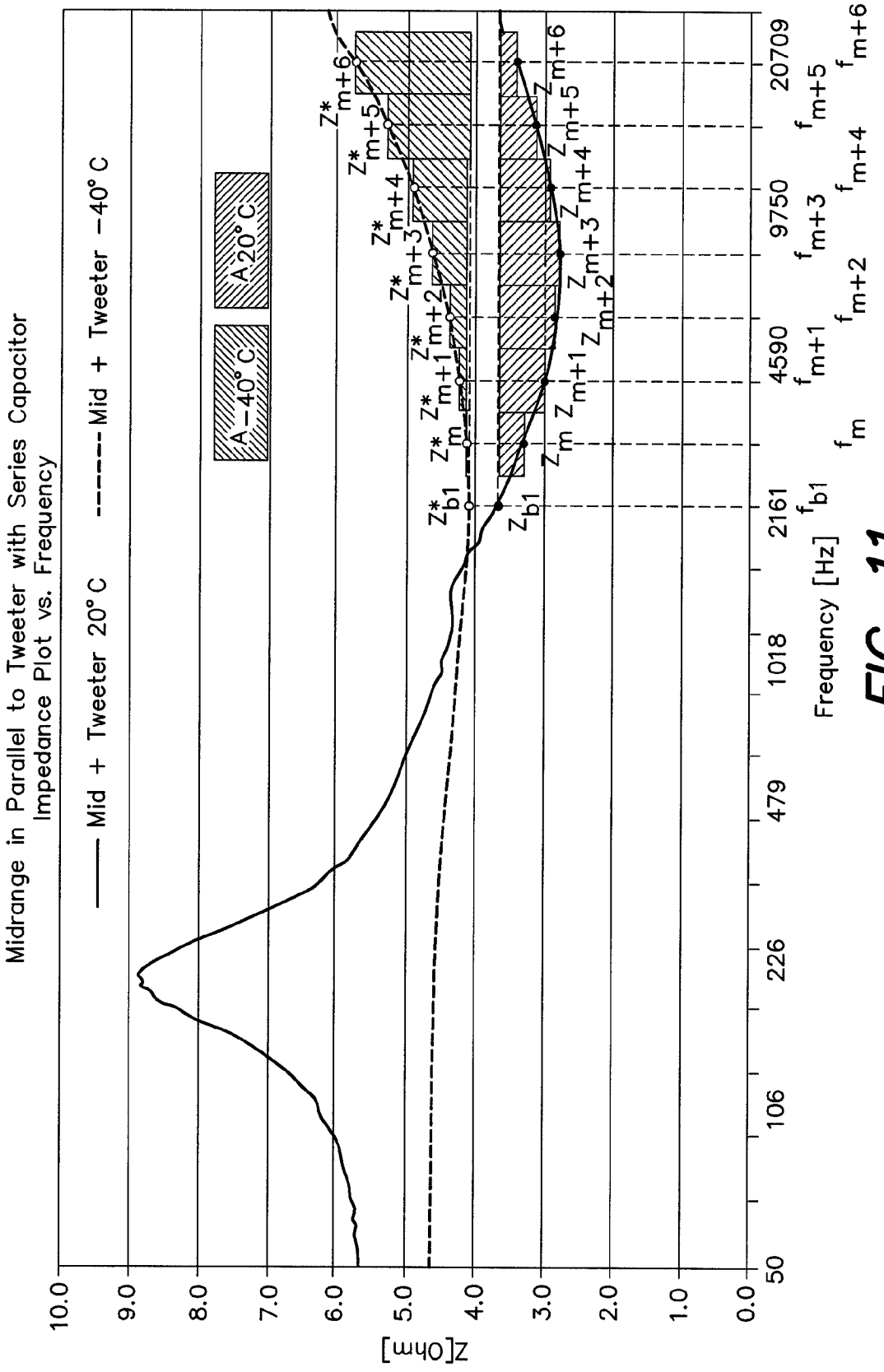

Midrange in Parallel to Tweeter with Series Capacitor
Impedance Plot vs. Frequency
Mid + Tweeter 20° C
Mid + Tweeter −40° C
A −40° C
A 20° C
Z[Ohm]
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
50
106
226
479
1018
2161
4590
9750
20709
Frequency [Hz]
f_{b1}
f_m
f_{m+1}
f_{m+2}
f_{m+3}
f_{m+4}
f_{m+5}
f_{m+6}
Z^*_{b1}
Z^*_m
Z^*_{m+1}
Z^*_{m+2}
Z^*_{m+3}
Z^*_{m+4}
Z^*_{m+5}
Z^*_{m+6}
Z_{b1}
Z_m
Z_{m+1}
Z_{m+2}
Z_{m+3}
Z_{m+4}
Z_{m+5}
Z_{m+6}

FIG. 11

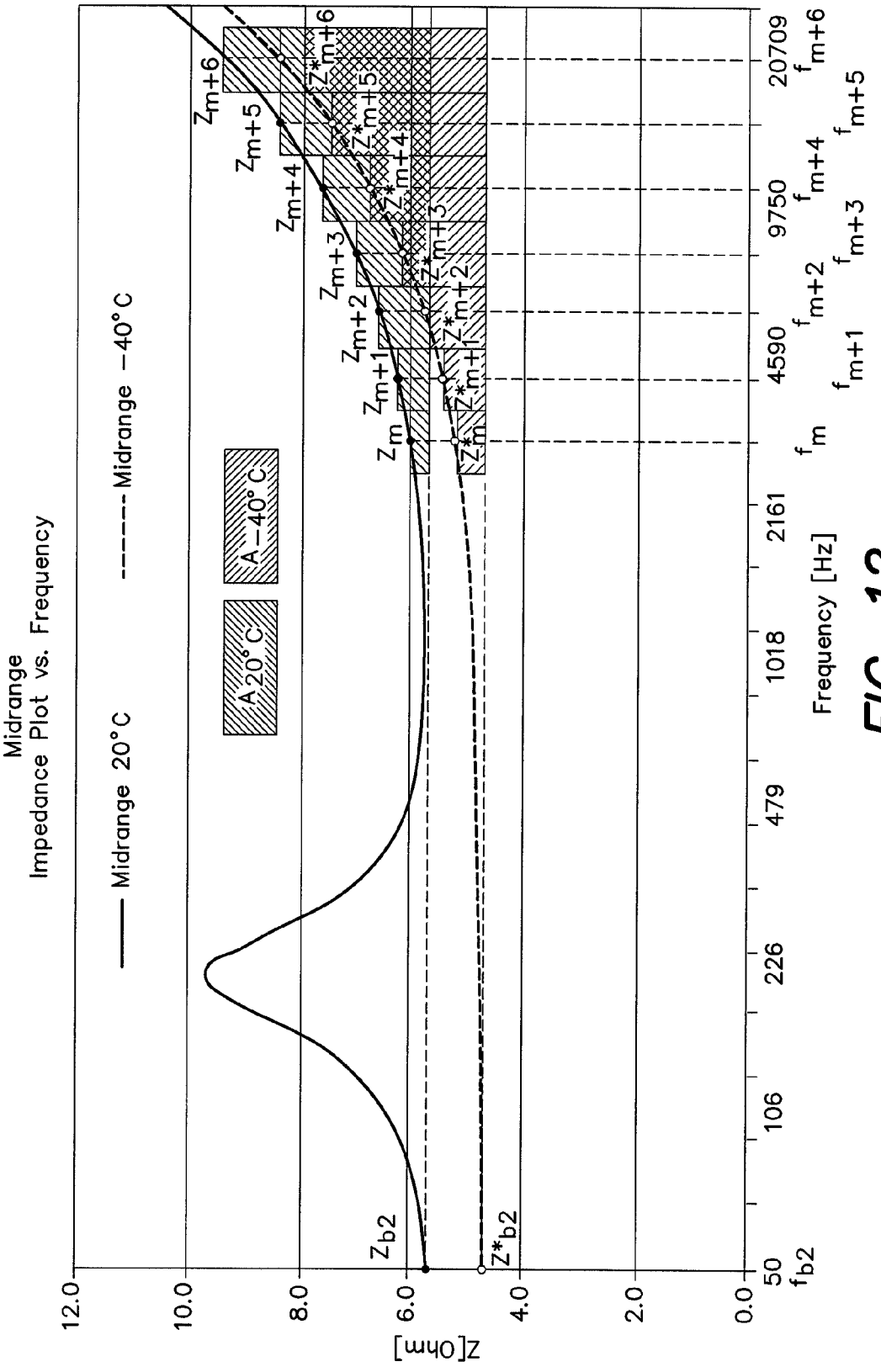

Midrange
Impedance Plot vs. Frequency
Midrange 20°C
Midrange −40°C
A 20°C
A −40°C
Z[Ohm]
12.0
10.0
8.0
6.0
4.0
2.0
0.0
Frequency [Hz]
50
106
226
479
1018
2161
4590
9750
20709
f_{b2}
f_m
f_{m+1}
f_{m+2}
f_{m+3}
f_{m+4}
f_{m+5}
f_{m+6}
Z_{b2}
Z^*_{b2}
Z_m
Z_{m+1}
Z_{m+2}
Z_{m+3}
Z_{m+4}
Z_{m+5}
Z_{m+6}
Z^*_m
Z^*_{m+1}
Z^*_{m+2}
Z^*_{m+3}
Z^*_{m+4}
Z^*_{m+5}
Z^*_{m+6}

FIG. 12

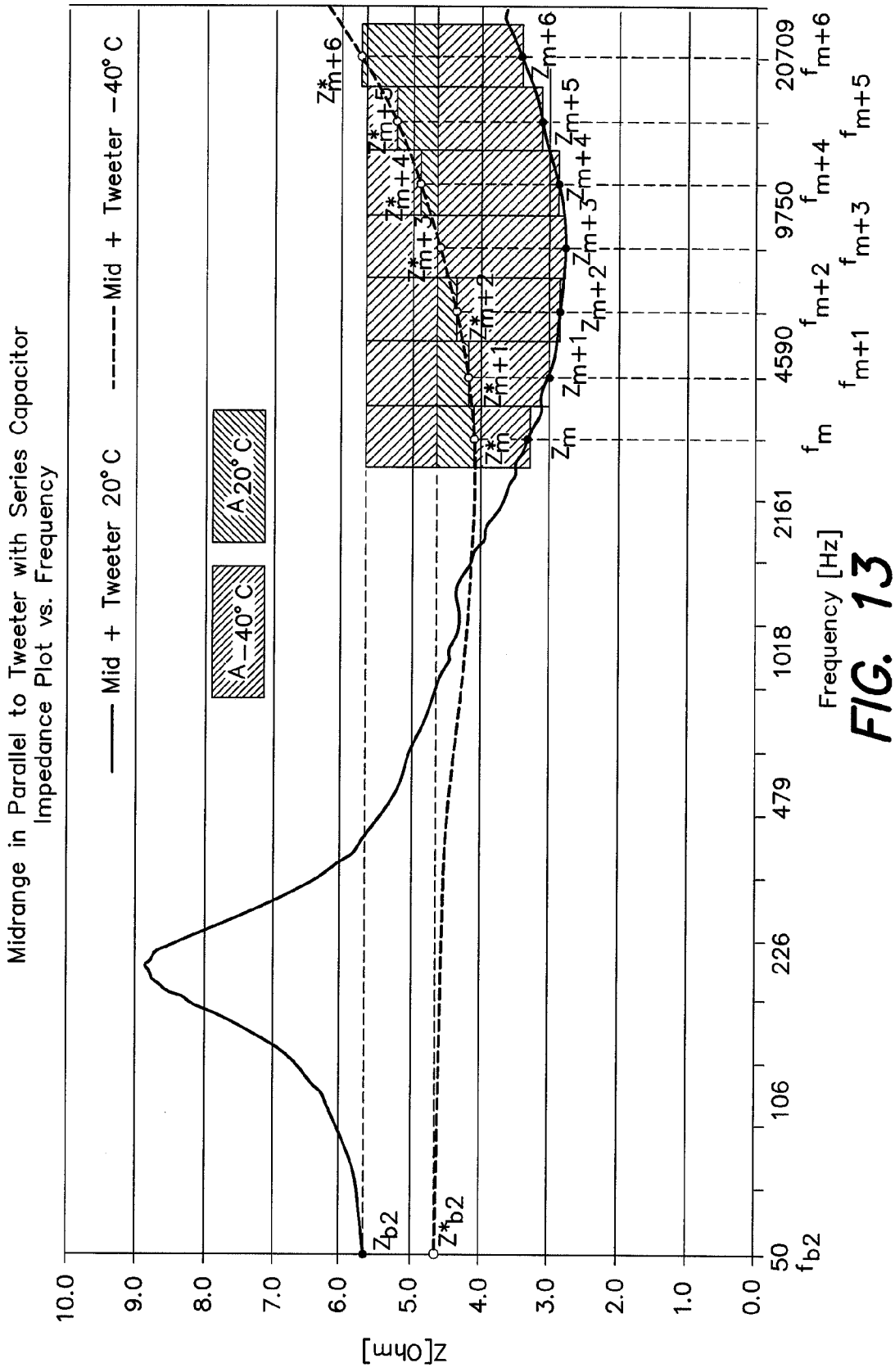

Midrange in Parallel to Tweeter with Series Capacitor
Impedance Plot vs. Frequency
Mid + Tweeter 20° C
Mid + Tweeter −40° C
A −40° C
A 20° C
Z[ohm]
Frequency [Hz]
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
50
106
226
479
1018
2161
4590
9750
20709
f_{b2}
f_m
f_{m+1}
f_{m+2}
f_{m+3}
f_{m+4}
f_{m+5}
f_{m+6}
Z_{b2}
Z^*_{b2}
Z_m
Z_{m+1}
Z_{m+2}
Z_{m+3}
Z_{m+4}
Z_{m+5}
Z_{m+6}
Z^*_m
Z^*_{m+1}
Z^*_{m+2}
Z^*_{m+3}
Z^*_{m+4}
Z^*_{m+5}
Z^*_{m+6}

FIG. 13

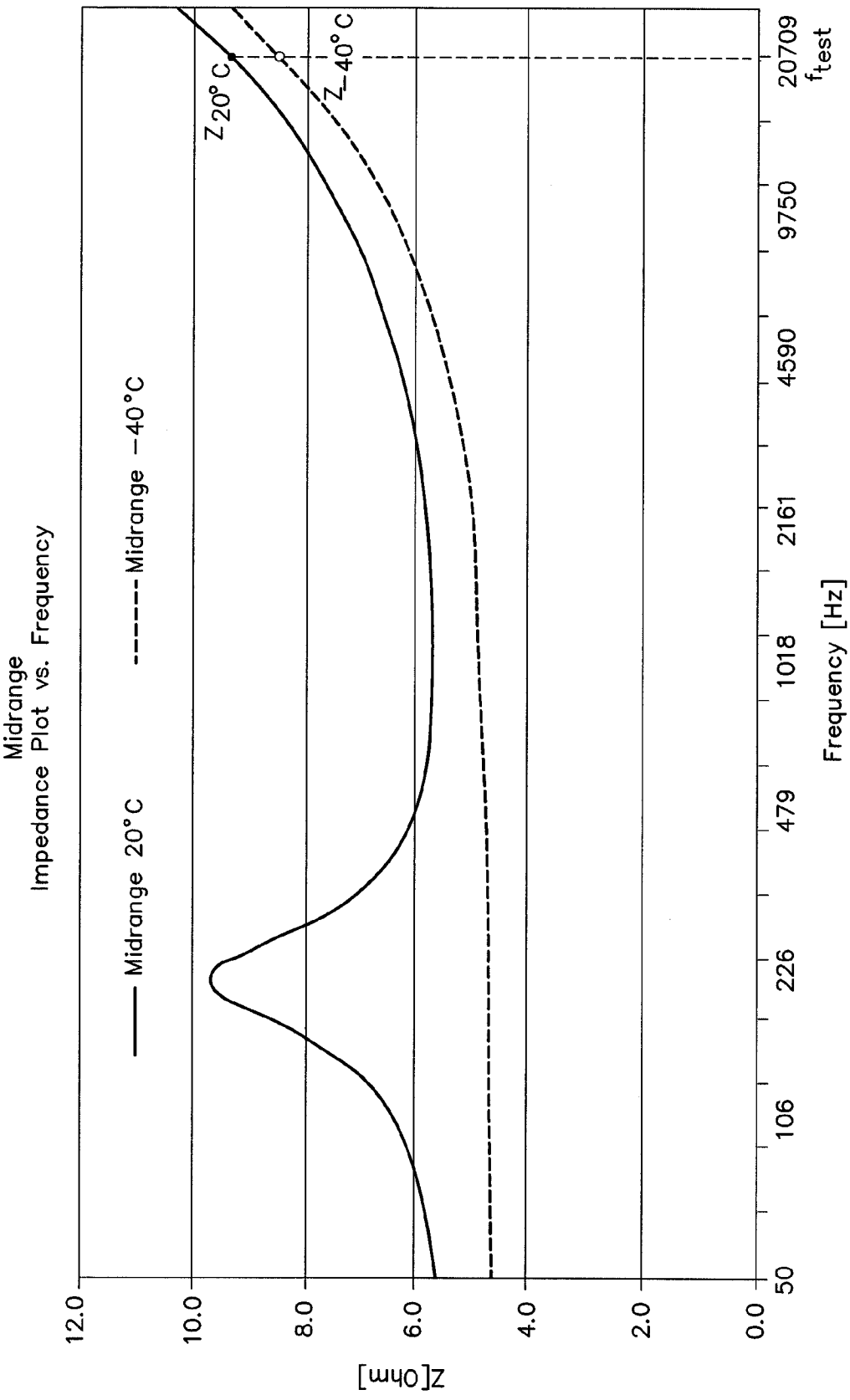

Midrange
Impedance Plot vs. Frequency
Midrange 20°C
Midrange −40°C
Z 20° C
Z −40° C
Z[Ohm]
12.0
10.0
8.0
6.0
4.0
2.0
0.0
50
106
226
479
1018
2161
4590
9750
20709
ftest
Frequency [Hz]

FIG. 14

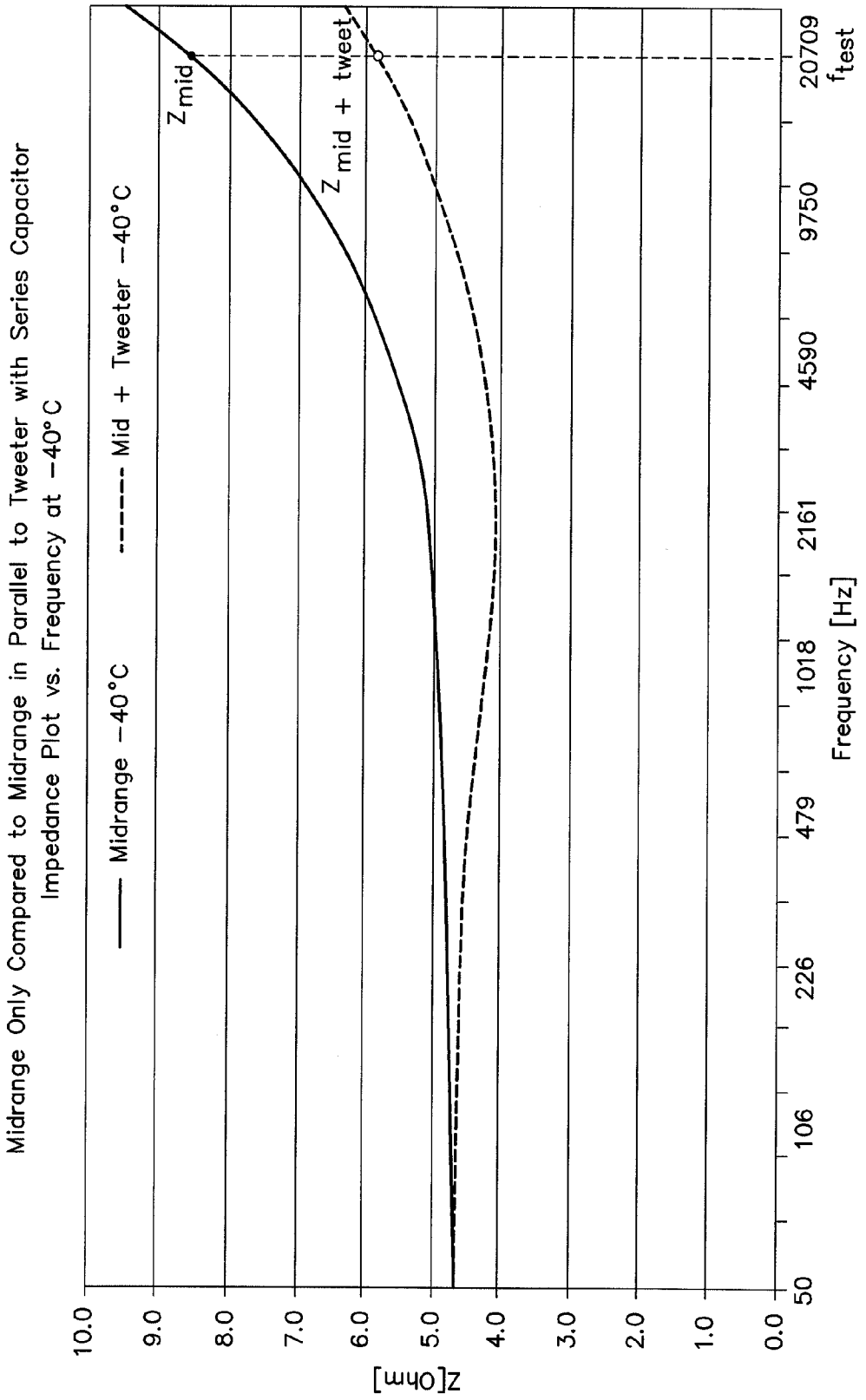

Midrange Only Compared to Midrange in Parallel to Tweeter with Series Capacitor
Impedance Plot vs. Frequency at −40° C
Midrange −40°C
Mid + Tweeter −40°C
Z mid
Z mid + tweet
Z[ohm]
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
50
106
226
479
1018
2161
4590
9750
20709
ftest
Frequency [Hz]

FIG. 15

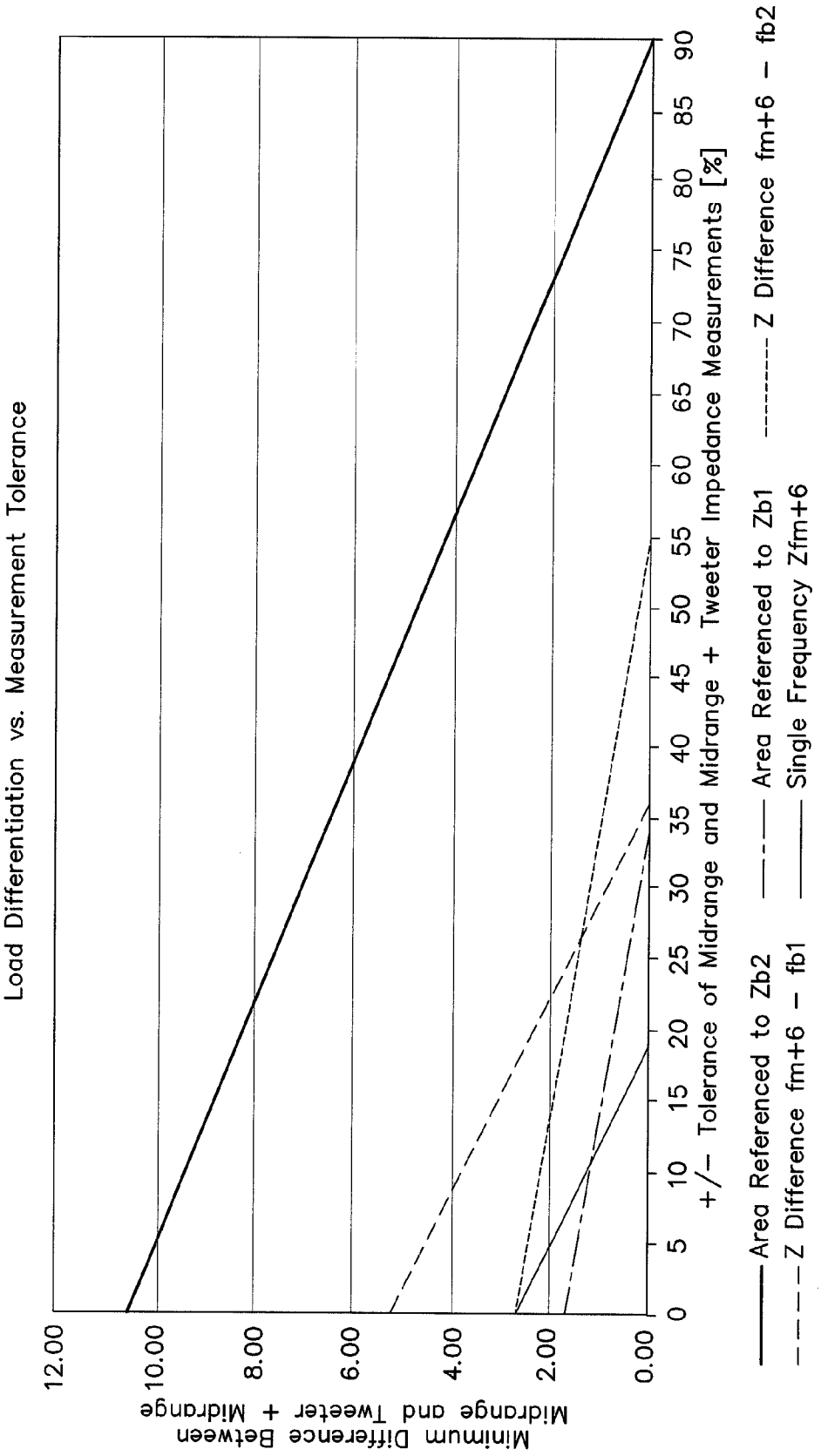

Load Differentiation vs. Measurement Tolerance
Minimum Difference Between Midrange and Tweeter + Midrange
12.00
10.00
8.00
6.00
4.00
2.00
0.00
0
5
10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
90
+/- Tolerance of Midrange and Midrange + Tweeter Impedance Measurements [%]
Area Referenced to Zb2
Area Referenced to Zb1
Z Difference fm+6 - fb2
Z Difference fm+6 - fb1
Single Frequency Zfm+6

FIG. 16

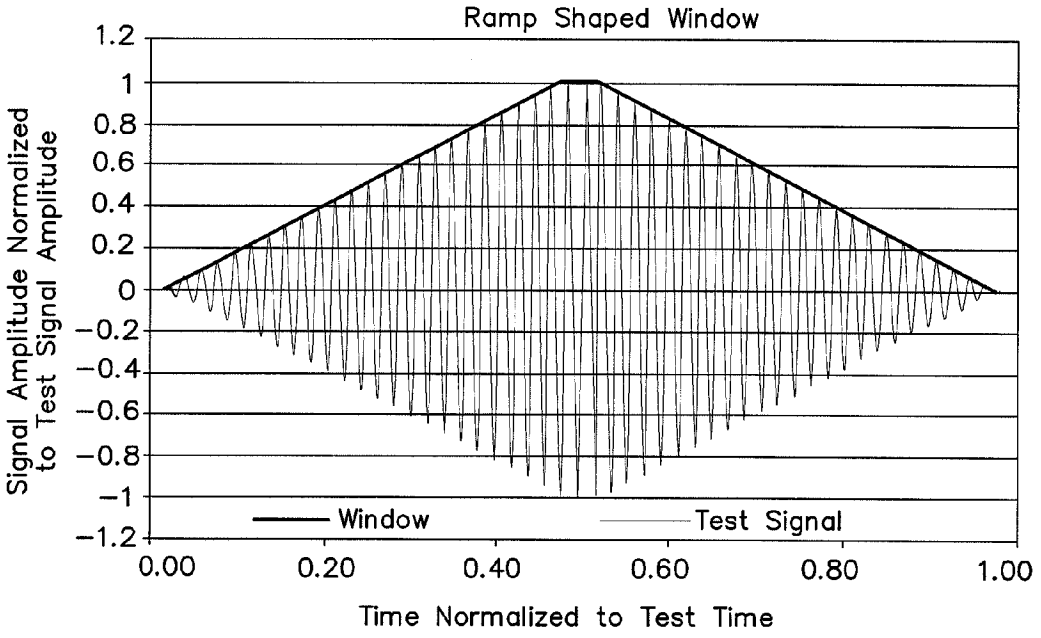

Ramp Shaped Window
Signal Amplitude Normalized to Test Signal Amplitude
1.2
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
−1.2
Window
Test Signal
0.00
0.20
0.40
0.60
0.80
1.00
Time Normalized to Test Time

FIG. 17

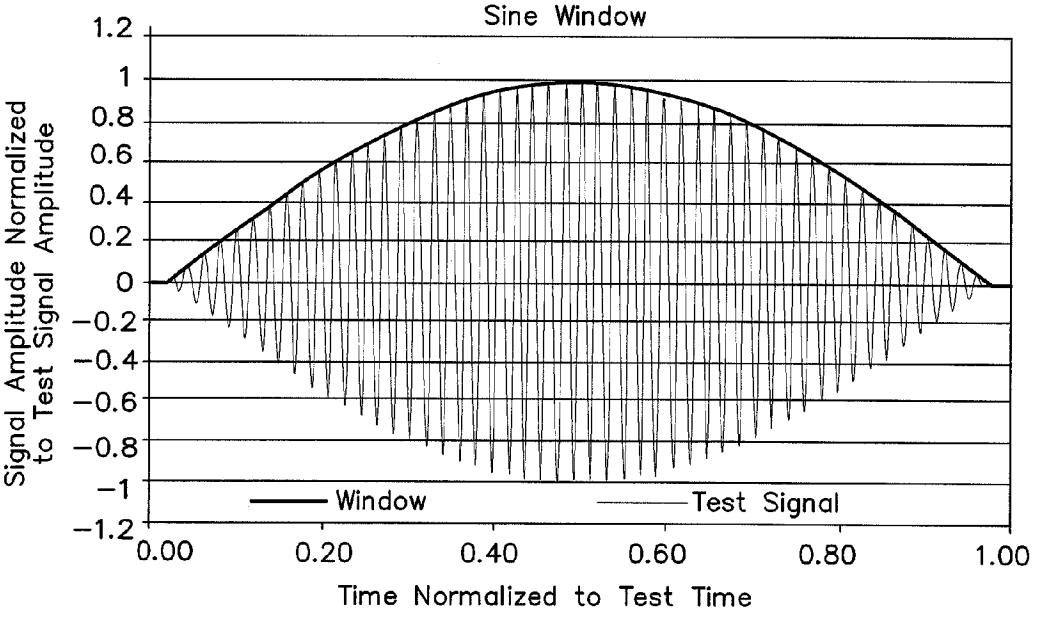

Sine Window
Signal Amplitude Normalized to Test Signal Amplitude
1.2
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
−1.2
Window
Test Signal
0.00
0.20
0.40
0.60
0.80
1.00
Time Normalized to Test Time

FIG. 18

ELECTRICAL LOAD DETECTION APPARATUS

1. CLAIM OF PRIORITY

[0001] This patent application claims priority to European Patent Application serial number 08 008 141.7 filed on Apr. 28, 2008.

2. FIELD OF TECHNOLOGY

[0002] The invention relates to a load detection for a load comprising multiple frequency-dependant sub-loads and evaluating a load comprising multiple frequency-dependant sub-loads.

3. RELATED ART

[0003] During audio system assembly in automobile manufacturing lines and in audio system checks performed in repair shops, it is necessary to test the interconnection between the amplifier and loudspeakers of the audio system to ensure the quality of the audio system. Various wiring problems can be experienced including failure to properly join the harness wiring to the loudspeaker terminals, bent or broken terminals, and pinched or broken wires in the harness.

[0004] Existing speaker detection techniques include what is known as a speaker walk-around test, wherein the audio system is placed into a test mode in which it sequentially sends an output audio signal individually to each loudspeaker while a person listens to determine if proper sound comes from each loudspeaker. However, this procedure is time consuming and it is difficult for the listener to detect a single loudspeaker in the presence of noise.

[0005] It is also known to employ each loudspeaker as a pick-up or microphone to generate a signal for sensing the presence of a properly connected loudspeaker. By forcibly moving a loudspeaker cone, a voltage is created across the loudspeaker. But since a loudspeaker is not optimized to perform as a pick-up, a high sound-pressure level is required to generate a detectible signal (e.g., by slamming a door). However, this method is also time consuming and is not reliable since it is difficult to identify the output signal of a particular loudspeaker under investigation since woofers, midrange speakers, and tweeters are commonly coupled to each other by a crossover network.

[0006] Furthermore, the prior art methods are not well adapted for detecting intermittent speaker connection problems after a vehicle is put into service since they require interaction by a human test operator.

[0007] Therefore, there is a need for automatically detecting of faults in different loudspeakers of a loudspeaker system.

SUMMARY OF THE INVENTION

[0008] A load detection arrangement for a load comprising multiple frequency-dependant sub-loads comprises an impedance measuring unit that is connected to the load and measures a representation of the impedance characteristic of the load; an evaluation unit that calculates a quantity representing the shape of the impedance characteristic of the load, the quantity being insusceptible to frequency independent errors and/or tolerances; a memory unit in which one or more representations of the quantity representing the shape of the impedance characteristic of the load resulting from different configurations of the sub-loads are stored; and a comparison unit that is connected to the evaluation unit to receive a representation of the shape of the currently measured impedance characteristic of the load and to the memory unit to receive the stored representations. The comparison unit compares the measured representation of the shape with each one of the stored representations and, in case that the measured representation matches a stored representation, to identify the configuration of the sub-loads within the load.

DESCRIPTION OF THE DRAWINGS

[0009] The invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, instead emphasis being placed upon illustrating the principles of the invention. Moreover, in the figures, like reference numerals designate corresponding parts. In the drawings:

[0010] FIG. **1** is a block diagram illustration of a signal generator having a load comprising parallel connected sub-loads;

[0011] FIG. **2** is a block diagram illustration of an audio system having a load comprising serial connected sub-loads;

[0012] FIG. **3** is a block diagram illustration of a load detection arrangement using a broadband test signal;

[0013] FIG. **4** is a block diagram illustration of a load detection arrangement using a sequence of narrowband test signals and a comparator;

[0014] FIG. **5** is a block diagram illustration of a load detection arrangement using a sequence of narrowband test signals and a peak detector;

[0015] FIG. **6** is a diagram illustrating an load impedance curve over frequency;

[0016] FIG. **7** is a flow chart illustration of an example of a novel load detection technique;

[0017] FIG. **8** shows a truth table used for load detection in connection with the technique illustrated in FIG. **7**;

[0018] FIG. **9** is a diagram illustrating an impedance-over-frequency curve for a tweeter including a series capacitor at different temperatures;

[0019] FIG. **10** is a diagram illustrating an impedance-over-frequency curve for a midrange loudspeaker at different temperatures, the area between the curve and a base line being shaded;

[0020] FIG. **11** is a diagram illustrating an impedance-over-frequency curve for a parallel circuit of the midrange loudspeaker and the tweeter including the series capacitor at different temperatures, the area between the curve and a base line being shaded;

[0021] FIG. **12** is a diagram illustrating an impedance-over-frequency curve for a midrange loudspeaker at different temperatures similar to FIG. **11**;

[0022] FIG. **13** is a diagram illustrating an impedance-over-frequency curve for a parallel circuit of the midrange loudspeaker and the tweeter including the series capacitor at different temperatures similar to FIG. **11**;

[0023] FIG. **14** is a diagram illustrating the single frequency load detection technique applied to an impedance plot of the midrange loudspeaker;

[0024] FIG. **15** is a diagram illustrating the single frequency load detection technique applied to an impedance plot of the parallel circuit of the midrange loudspeaker and the tweeter including the series capacitor;

[0025] FIG. **16** is a diagram illustrating the allowable tolerances including measurement errors in percent dependent on the load analysis used in order to ensure a reliable load detection;

[0026] FIG. **17** is a diagram illustrating a test signal with a trapezoid shaped window; and

[0027] FIG. **18** is a diagram illustrating a test signal with a sine shaped window.

DETAILED DESCRIPTION

[0028] FIG. **1** is a block diagram illustration of an arrangement **100** (e.g., an audio system) comprising a signal source **1** (e.g., an audio amplifier) supplying an electrical signal to a load **2** that comprises n sub-loads **2.1** to **2.***n* (e.g., loudspeakers) connected in parallel. Each of the sub-loads **2.1** to **2.***n* has a frequency-dependant impedance characteristic $Z_i(f)$ with i=1 . . . n and f=frequency. The impedance $Z_{total}(f)$ of the load **2** is:

$$Z_{total}(f)=1/(1/Z_1(f)+1/Z_2(f)+\ldots+1/Z_n(f))$$

[0029] FIG. **2** illustrates an alternative arrangement **200** that differs from the embodiment illustrated in FIG. **1** in that the n sub-loads **2.1** to **2.***n* of the load **2** are connected in series. The impedance $Z_{total}(f)$ of the load **2** in the arrangement of FIG. **2** is:

$$Z_{total}(f)=Z_1(f)+Z_2(f)+\ldots+Z_n(f).$$

[0030] The load **2** may also be a combination of series and parallel connected sub-loads as discussed below with reference to FIG. **3**. The novel approach is able to detect in case of a parallel connection (FIG. **1**) whether any of the sub-loads **2.1** to **2.***n* is missing (open) or not, and in case of a series connection (FIG. **2**) whether any of the sub-loads is shorted or not. In both cases, each of the sub-loads can be detected independent of all other loads. In the case of parallel and series sub-loads (FIG. **3**), the term "open" applies to sub-loads connected in parallel and "short circuit" applies to sub-loads in series.

[0031] Referring to FIG. **3**, the load **2** comprises, for example, four sub-loads **2.1** (e.g., a low-range loudspeaker), **2.2** (e.g., a capacitor), **2.3** (e.g., a mid-high-range loudspeaker), and **2.4** (e.g., an inductance). The sub-loads **2.1** and **2.2** are connected in parallel as well and the sub-loads **2.3** and **2.4** are connected in parallel. Furthermore, the parallel connected sub-loads **2.1** and **2.2** and the parallel connected sub-loads **2.3** and **2.4** are connected in series forming a kind of H-circuit which is represented by the load **2**. This H-circuit is connected to an impedance measuring unit **3** and adapted to measure a representation of the impedance characteristic of the load **2**. The impedance measuring unit **3** comprises in the present example a test signal source **4** providing test signal comprising, e.g., a plurality of simultaneously transmitted sinusoidal voltages each with a certain, e.g., the same, amplitude (or, alternatively, a broadband white noise signal). The impedance measuring unit **3** further comprises a Fast-Fourier transformation (FFT) unit **5** that performs an FFT on the current flowing through the load **2** in order to provide an impedance characteristic as an impedance curve over frequency. The impedance characteristic may be represented by at least two data words (e.g., 512 pairs of data words) where one of the data words refers to a frequency value and the other to the respective impedance value. The measurement result (i.e., the impedance-over-frequency-curve) is used to calculate a quantity representing the shape of the impedance curve. Therefore, the measurement unit **3** comprises an evaluation unit that is configured to calculate a quantity representing the shape of the impedance characteristic of the load, whereby the quantity is insusceptible to frequency independent errors and/or tolerances. Such quantities may be, for example, the slope of the curve at given frequencies or the area between the curve and a threshold line defining a threshold impedance at a pre-defined frequency.

[0032] In a memory unit **6** representations of the mentioned quantity representing the shape of the impedance characteristics of the load are stored. Each one of the stored quantities represents the shape of the impedance curve over frequency of the load **2** when at least a particular one of the sub-loads **2.1**, **2.2**, **2.3**, and **2.4** is in a fault condition. Assuming that each sub-load can be in one of three conditions, "ok", "open", and "short circuit" and having, in the exemplary arrangement of FIG. **3**, four sub-loads, the number of representations of the quantity stored is 3^4=81. This number corresponds to **81** different configurations of the sub-loads within the load or to the so-called load situations including one representing a proper condition of the load **2**. Accordingly, **80** representations of the shape-quantity (excluding the situation of a proper load) or **81** representations of the shape-quantity (including the situation of a proper load) may be stored in the memory unit **6**. In order to get a fast result if the load is in a proper condition or in a fault condition the arrangement may first (or only) check if the shape-quantity representing a proper condition is met. In case it does not the sub-load being in a fault condition may be identified afterwards if desired.

[0033] The arrangement of FIG. **3** further comprises a comparison unit **7** that is connected to the impedance measuring unit **3** (and thus to the evaluation unit) to receive a representation of the shape of the currently measured impedance characteristic of the load **2** and to the memory unit **6** to receive the stored representations. The comparison unit **7** compares the measured representation with each one of the stored shape-quantities and in case the measured representation matches one of the stored **80** representations corresponding to fault situations it distinctly identifies the sub-load or sub-loads being in a fault condition by the stored **80** representations. In case **81** representations are used it may also identify the proper-load situation. The results are provided by an output signal **8** identifying the sub-load or sub-loads being in a fault condition.

[0034] In the exemplary arrangement shown in FIG. **3** the test signal comprises a multiplicity of simultaneously transmitted sinusoidal voltages. However, the multiplicity of sinusoidal voltages may be transmitted sequentially instead of simultaneously. Sequentially transmitted sinusoidal voltages are used in the arrangements shown in FIGS. **4** and **5**.

[0035] In the arrangement of FIG. **4**, a sine wave generator **9** and an audio amplifier **10** together form the test signal source **4**. The audio amplifier **10** may be the same used in the regular mode for amplifying the useful signals such as music or speech, and has a volume control line **11** to control the volume of a signal supplied to its input. In the test mode, the sine wave generator **9** is connected to this input to provide a sinusoidal signal with a certain frequency that is controllable by a signal on a frequency control line **12**. The audio amplifier **10** provides a sinusoidal voltage to the load **2** via a current sensor **13** measuring the current flowing through the load **2**. Instead of a current sensor a voltage sensor may be used in case that the test signal source provides a test current. A representation of the measured current is supplied to a com-

parator **14** that compares this representation with a threshold **15** representing a current threshold. The result of the comparison is supplied to a control logic unit **16** that is connected to the sine wave generator **9** and the audio amplifier **10** through the frequency control line **12** and the volume control line **11**, respectively, for providing the respective control signals.

[0036] The control logic unit **16** controls the frequency and the signal amplitude of the test signal. The current sensor **13** measures the current that flows into the load **2** and the comparator **14** compares the measured current with the threshold **15**. At each test frequency, the amplifier gain starts at a value where the load current is less then the threshold and is increased in steps that are sufficiently small with respect to the expected load variations for all possible load combinations. When the load current at the given frequency becomes higher than the current threshold for the first time, the corresponding impedance value can be calculated from the current threshold, the output amplitude of the sine wave generator **9** and the amplifier gain. For the following analysis the impedance value itself is not needed and the gain value is sufficient. The gain value for all other test frequencies is determined in the same way.

[0037] The arrangement of FIG. **5** differs from that shown in FIG. **4** in that the comparator **14** in connection with threshold **15** is substituted by a peak detector **17**. Here, the gain of the audio amplifier **10** does not need to be varied. Instead, the impedance of the load **2** is calculated from the sine wave generator output, the (constant) amplifier gain and the peak current determined by the peak detector **17**.

[0038] With reference to FIGS. **6** and **7**, an example is discussed how the control logic unit **16** in the arrangement of FIG. **4** controls the process of identifying sub-loads in a fault condition. FIG. **7** illustrates a process that is used to analyze the load combinations of FIG. **6**. Tweeters and (bass-) midrange loudspeakers coupled by a passive crossover network are commonly used in multi-channel car audio systems. Commonly used amplifiers and loads, e.g., loudspeakers in connection with passive components such as inductors and capacitors, tend to have large tolerances as well as the measurement systems which are supposed to be low-cost.

[0039] However, most of these tolerances are frequency independent so that the absolute impedance values measured may change, but not the shape of the impedance curves. Accordingly, the shape of the curve may be used to differentiate all possible load combinations despite all frequency independent system tolerances. The shape may be, for example, characterized by the slope of the curve at given frequency values or by the area under the curve. By considering such characteristic values representing the shape of the impedance curve (but not the absolute impedance values) the load detection may be designed to be more robust against tolerances. The process discussed with reference to FIG. **7** is explained as a first example that uses the lowest possible frequency resolution of only two test frequencies for impedance measurements. As the involved sub-loads show substantial variations in the shape of the impedance curve when one or more sub-loads are missing or in short circuit state, this resolution is sufficient in the present example. Accordingly, a representation of the shape of the curve is considered not the curve itself, i.e., not the absolute impedance values. Sub-load combinations of higher complexity may require the use of a considerably higher number of test frequencies.

[0040] In the example of FIG. **7** based on the arrangement of FIG. **4**, the rough shape of the impedance curve of FIG. **6** is used to analyze the load **2**. The shape of the impedance curve is thereby roughly represented by the slope of the curve, whereby the slope is approximated by the difference between two impedance values $Z(f_1)-Z(f_2)$. At first the required gain of the audio amplifier **10** is determined to get a load current higher than the current threshold at test frequency f_1 which may be 20 Hz. Therefore, the gain (Gain) which starts at a known value in order to result in a load current lower than the current threshold for all possible tolerances (StartGain) is increased in little steps. The gain increment depends on the gain resolution needed to differentiate all possible load combinations.

[0041] Being beyond the MaxGain point (representing maximum gain) which has to be high enough to ensure that the current threshold can be reached for all possible sub-load combinations of interest at the given frequency (which in case of f_1 is only the midrange including all tolerances) indicates that there is no midrange loudspeaker connected. Otherwise the result is a gain value that trips the current threshold comparator which then is stored in Gain_f**1** and indicates at least the midrange loudspeaker is present. The gain value $Gain\_f_1$ is a representation of the first impedance value $Z(f_1)$. In any case the next step is to repeat the preceding procedure for the second test frequency f_2 which may be 20 kHz. When the current threshold has been reached in the first step the corresponding gain value can be used as the start value for the second test frequency f_2. Otherwise the gain is set back to the originally gain StartGain. If no midrange loudspeaker is properly connected, there is the possibility to exceed the MaxGain again which indicates that the tweeter is also not connected.

[0042] If the current threshold is reached, it indicates that the tweeter is connected only. If the midrange loudspeaker has been detected at frequency f_1 the gain value which results in the load current to get higher then the current threshold for the first time at frequency f_2 is stored in Gain_f**2**, which is a representation of the second impedance $Z(f_2)$. Following the above elaborated idea, the difference between $Gain\_f_1$ and $Gain\_f_2$ (representing the difference $Z(f_1)-Z(f_2)$ being an approximation of the slope) is used to determine whether the tweeter is also connected. The midrange loudspeaker alone exhibits a large increase of impedance between frequencies f_1 and f_2 while the combination of midrange loudspeaker and tweeter shows only a small increase. If the impedance increase is higher than the detection threshold DetectionThreshold then the tweeter is connected. The detection threshold has to take into account all frequency dependent impedance tolerances at frequencies f_1 and f_2 of the combination of the tweeter and the midrange loudspeaker.

[0043] All decisions that have to be made during the analysis of the measurements for the load detection in this example are included in the truth table of FIG. **8**. The truth table may be stored in a memory unit or, as in the present example, be hardwired in the control logic so that the control logic also has the function of a memory. The test frequencies f_1 and f_2 enable noiseless load detection as they may be adapted in frequency and/or amplitude to be inaudible for humans. If acoustical feedback for the test operator is desired for example a frequency f_3 (FIG. **6**) may be used instead of frequencies f_1 or f_2.

[0044] An advantage of the novel arrangement and method of the present invention is the insusceptibility to frequency independent tolerances inherent to the load and the load detection system. Besides this it is based on purely electrical

measurements and is fully automated therefore it saves costs and time. Since no acoustical measurements are needed, it is immune to noise and does not require microphones. But not only the sub-loads established by loudspeakers may be tested using the arrangement and method of the present invention but also the components of the cross-over network. Further, the novel arrangement and method is not restricted to audio systems but is also applicable in all fields where frequency dependent sub-loads (i.e., impedances) occur. A further advantage is that the novel arrangement and the method are relatively insusceptible to any tolerance or measurement errors occurring in the system, e.g., speaker, amplifier, comparator, et cetera.

[0045] According to another embodiment of the above discussed method of load detection based on characteristic "geometrical properties" (i.e., on the shape) of the load impedance curve the load can be analyzed by comparing the area between the impedance curve and a specific impedance base line over a specified frequency range to representations of this area for different load situations.

[0046] One advantage over the example of FIGS. **7** and **8**, where only the difference between two frequencies (as an approximation of the slope) is analyzed, can be seen in the still lower susceptibility to tolerances of the load and of the measurement. Another benefit of this embodiment is an increased measurement accuracy that is achieved by multiple measurements at different frequencies. In this way dynamic errors that change between measurements will be suppressed by averaging.

[0047] FIG. **9** illustrates the impedance of a tweeter connected in series to a capacitor as a function of frequency. The equivalent series resistance (ESR) of the capacitor and also its capacitance vary drastically over temperature. For example, two impedance curves are depicted in the diagram of FIG. **9**, one impedance curve for +20° Celsius and another for 40° Celsius. The tweeter itself also contributes to the total impedance (of the capacitor and tweeter) but its impedance variation over temperature is much lower than that of the capacitor. The example of FIG. **9** is given to illustrate the advantage of considering the "shape" of the impedance curve instead of the absolute impedance values.

[0048] FIG. **10** illustrates the impedance of a midrange loudspeaker at different temperatures. Accordingly, the impedance of the midrange loudspeaker also varies over temperature but variations are not as high as the impedance variations of the tweeter including its series capacitor (cf. FIG. **9**). At −40° Celsius the midrange loudspeaker looses its "resonance hump" but, apart from that, merely exhibits an offset of about 1 ohm to the impedance curve at +20° Celsius. Also illustrated in FIG. **10** is the area between the impedance curve and a "base line" that represents an impedance threshold which is defined as the impedance $Z_{b1}(f_{b1})$ present at a predefined "base frequency" f_{b1}. The symbol $Z_{b1}(f_{b1})$ refers to the impedance curve measured at +20° Celsius whereas the symbol $Z^*_{b1}(f_{b1})$ as well as all other symbols with a superscript asterisk refer to the impedance curve measured at −40° Celsius. Although the absolute impedance values $Z_m(f_m)$ change over temperature, the area between the base line and the impedance curve remains almost constant.

[0049] Similar to the example discussed with reference to FIGS. **6** to **8** the present example makes use of a characteristic quantity that represents the shape of the impedance curve rather than the impedance values themselves. This characteristic quantity may be, for example, the slope of the curve or an approximation thereof as used in the example of FIGS. **6** to **8** as well as the area between the impedance curve and a threshold represented by a base line. The characteristic quantity used in a specific application may represent the shape of the impedance curve only in a limited frequency range which may be sufficient depending on the requirements of the application.

[0050] In the example of FIG. **10** the sought area is defined by the curve and the threshold $Z_{b1}(f_{b1})$ for frequencies greater than the base frequency f_{b1}. In the example of FIG. **12**, which illustrates the same midrange loudspeaker impedance, the area is calculated between the impedance curve and the impedance threshold $Z_{b2}(f_{b2})$ which is determined at the base frequency f_{b2}. The difference between these two base frequencies will be discussed in the analysis of the resulting areas.

[0051] FIGS. **11** and **13** illustrate the combined impedance of the midrange loudspeaker (cf. FIGS. **10** and **12**) connected in parallel to the tweeter with its series capacitor (see FIG. **9**) for temperatures of 20° C. and −40° C. Again the areas between the impedance curves and the impedance base line at Z_{b1} and Z_{b2} are shown for the base frequencies f_{b1} and f_{b2}, respectively. It should be noticed that the measurement frequencies (f_m to f_{m+6}) for FIG. **10** to FIG. **13** are the same. Only the base frequency is changed (f_{b1}, f_{b2}) and therefore the impedance base line changes which results in different areas between the impedance base line and the impedance curves.

[0052] To determine the impedance base line (i.e., the threshold Z_{b1} or Z_{b2}) an impedance measurement at the base frequency f_{b1} or, alternatively, f_{b2} is carried out for example with a test setup as shown in FIG. **4**. The measured impedance Z_{b1} or, alternatively, Z_{b2} defines the impedance base line. Afterwards the impedance at the test frequencies f_m to f_{m+6} is measured in the same way resulting in impedance representations Z_m to Z_{m+6}. After this step the areas A as shown in FIGS. **10** and **11** are calculated with the equation:

$$A = \sum_{n=0}^{N} (Z_{m+n} - Z_{b1}) \text{ with } N = 6 \qquad \text{(EQ. 1)}$$

[0053] For FIGS. **12** and **13** the equation for the resulting area A is:

$$A = \sum_{n=0}^{N} (Z_{m+n} - Z_{b2}) \text{ with } N = 6. \qquad \text{(EQ. 2)}$$

[0054] When using frequency values f_m, f_{m+1}, etc. that are equidistant on the frequency scale of the analyzed impedance curve no multiplication is necessary for computing the area A. If the distances between the (for example logarithmically scaled) test frequencies being geometrically equal this distance can be normalized and set to unity without changing the comparability of the resulting area representations.

[0055] It is important to notice that the geometric properties of the load impedances as shown in FIGS. **10** to **13** are based on a logarithmic scale of the frequency axis. Therefore the test frequencies (f_m to f_{m+6}) need to be spaced logarithmically in order to obtain a valid result in accordance to the areas illustrated in the frequency plots. However, a linear frequency scale can also be used. Furthermore, the frequency values at

which impedance values are measured do not necessarily need to be equidistant in order to provide useful results. However, in this case the resulting "area" value calculated by EQ. 1 or EQ. 2 is not a geometrically interpretable area.

[0056] The number of test frequencies f_{m+n}, (n=0, 1, . . .) is determined by the resolution needed in order to differentiate the impedance curves of all load combinations of interest. For the given example the 7 test frequencies used are sufficient even for large tolerances in the load and the measurement system. This will be analyzed in more detail further below.

[0057] Below, the assessment of the load impedance according to the above example is compared to the classical single frequency load analysis approach. FIG. **14** illustrates the impedance-over-frequency curve of the midrange loudspeaker already mentioned above (cf. FIG. **10**). For a single frequency load analysis the test frequency f_{test} of about 20 kHz has been chosen because it is well within the frequency range that a digital audio system with a 44.1 kHz sampling rate can produce and because the impedance at this frequency is considerably different for either the midrange loudspeaker alone or the parallel circuit of the midrange and the tweeter including a series capacitor. In this way the best possible differentiation for the single frequency method is reached. As can be seen in FIG. **15** the minimum difference between the midrange loudspeaker impedance and the impedance of the parallel circuit of the midrange and the tweeter including the series capacitor that occurs at −40° C. increases with an increasing frequency.

[0058] The principle of the single frequency load analysis is simple measurement of the absolute impedance at the test frequency and a comparison to an impedance threshold that decides whether only the midrange loudspeaker is connected or both the midrange speaker and the tweeter are connected in parallel. As can be seen from FIG. **15**, neglecting any measurement errors and tolerances of the load, a minimum difference of about 2.7 ohms between the two curves exists at the test frequency f_{test}. This enables proper differentiation between the above mentioned load configurations (midrange only or midrange and tweeter) only when the tolerance bands of the possible loads do not overlap at the test frequency. However, this is not the case in practice.

[0059] Unfortunately real world measurement systems show various degrees of measurement accuracy with a tendency for large measurement errors in inexpensive systems implemented in integrated circuits. Furthermore the load itself may show additional tolerances like part to part variation, aging variations, connector contact resistance and so on. Therefore in the following part of the description it is evaluated how the classical single frequency load analysis approach and the novel approach according to an aspect of the invention handle these tolerances and measurement errors.

[0060] The comparison of the different load analysis methods is carried out based on the impedance curves discussed above. For comparison purposes the area between an impedance base line (threshold) Z_{b1} or, alternatively, Z_{b2} and the impedance curves is calculated as explained above (cf. EQ. 1 and EQ. 2). Furthermore, the difference between two impedances at two different frequencies as used in the example of FIGS. **6** to **8** will be evaluated for f_{b1} and f_{b2} each combined with f_m.

[0061] For the comparison the impedance values of the midrange loudspeaker and the parallel circuit of midrange loudspeaker and tweeter including a series capacitor have been varied between 0% to ±90% as it would be the case for a measurement system with measurement errors or frequency independent tolerances of the load. For the resulting tolerance bands the minimum difference between the two compared load situations has been calculated and displayed versus the applied tolerance in FIG. **16**. The point on the abscissa where the minimum difference between the tolerance bands around the two impedance curves to be distinguished becomes zero is the tolerance above which a differentiation between the two load configurations (i.e., midrange speaker alone or midrange speaker and tweeter) is not possible any more.

[0062] As can be seen in FIG. **16** for the present example the single frequency load detection has the highest susceptibility to tolerances and errors. Deviations (due to errors and tolerances) greater than about ±18% from the nominal value result in an unreliable or impossible differentiation between the different load configurations. The method that estimates the slope of the impedance curve by calculating the difference $f_{m+2}-f_{b1}$ works up to deviations of ±34% which is an improvement of tolerance susceptibility of 89%. With an operation limit of about ±36% of tolerances the method that considers the area between the horizontal line at impedance Z_{b1} (threshold) and the impedance curve is a still a bit better.

[0063] Changing the base frequency to f_{b2} results in a maximum possible tolerance of ±55% for the method that considers the slope estimated by calculating the difference between Z_{b2} and Z_{m+6}. For the area method with a base frequency f_{b2} the tolerance can get as high as ±90% before the load differentiation becomes impossible. The susceptibility to tolerances is thus improved by up to a factor of 5 (improvement of 400%) between the classical single frequency load impedance analysis and the method based on the impedance curve shape analysis.

[0064] In case of the load being a loudspeaker it is sometimes desired to make the test signal such that it does not disturb humans and animals or, if possible, to make the test signal even inaudible. As has been noted above frequencies (approx. 20 kHz) outside the human-audible audio band can be used. However, if these frequencies are applied to a loudspeaker in form of a sine wave burst that can be seen as a sine wave multiplied by a rectangular window function, the resulting acoustical signal will be a broad spectrum of frequencies around the test signal frequency that eventually will at least overlap the audible audio band.

[0065] Therefore special window functions may need to be applied that keep the resulting frequency spectrum as narrow as possible. Even if the test frequencies are within the audio band a simple rectangular window can lead to unpleasant pop noises that have to be avoided in some cases. Triangle-, trapezoid-, or sine-shaped window functions have been proven to suppress such pop noise (cf. FIGS. **17** and **18** for respective triangle- or sine-windowed test signals).

[0066] Although various exemplary embodiments of the invention have been disclosed, it will be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the spirit and scope of the invention. It will be obvious to those reasonably skilled in the art that other components performing the same functions may be suitably substituted. Such modifications to the inventive concept are intended to be covered by the appended claims.

What is claimed is:

1. A load detection apparatus for a load comprising multiple frequency-dependant sub-loads, the load detection apparatus comprising:

an impedance measuring unit that is connected to the load and measures a representation of the impedance characteristic of the load, and calculates a quantity representing the shape of the impedance characteristic of the load;

a memory unit in which one or more representations of the quantity representing the shape of the impedance characteristic of the load resulting from different configurations of the sub-loads are stored; and

a comparison unit that is connected to the impedance measuring unit to receive a representation of the shape of the currently measured impedance characteristic of the load and to the memory unit to receive the stored representations;

where the comparison unit compares the measured representation of the shape with the stored representations and, in case that the measured representation matches one of the stored representations the comparison unit identifies the configuration of the sub-loads within the load.

2. The apparatus of claim **1**, where the different configurations of the sub-loads within the load under test comprises at least one configuration in which at least one sub-load is in a fault condition.

3. The apparatus of claim **2**, where the quantity representing the shape of the impedance characteristic of the load is the area, or an approximation thereof, between a measured impedance curve and a base line representing a constant threshold impedance measured at a pre-defined base frequency.

4. The apparatus of claim **2**, where the quantity representing the shape of the impedance characteristic of the load is the slope, or an approximation thereof, of a measured impedance curve at least one pre-defined base frequency.

5. The apparatus of claim **4**, where the slope is approximated as the average slope within a pre-defined frequency interval.

6. The apparatus of claim **1**, where the impedance measuring unit comprises a test signal source that generates a narrowband test signal having a frequency that is varied during load detection, and a current sensor that is connected between the test signal source and the load and is adapted to measure the current flowing from the test signal source into the load during load detection.

7. The apparatus of claim **6**, where the test signal has an amplitude which is varied during load detection at each one of the frequencies the test signal source is tuned to during load detection and where the comparison unit comprises a comparator that compares the measured current through the load to a threshold at each frequency to provide a representation of the impedance characteristics of the load.

8. The apparatus of claim **6**, where the test signal has an amplitude which is constant during load detection at each one of the frequencies the test signal source is tuned to during load detection, and where the comparison unit comprises a peak detector that identifies the peak of the measured current through the load during detection at each frequency to provide a representation of the impedance characteristics of the load.

9. The apparatus of claim **7**, where the comparison unit comprises a control logic unit that controls the frequency and amplitude of the test signal source and compares the representations provided by the comparator, with the result thereof with stored representations.

10. The apparatus of claim **9**, where the stored representations are part of a truth table that further comprises a list identifying the condition of at least some of the sub-loads.

11. The apparatus of claim **10**, where the memory unit is included in the comparison unit.

12. The apparatus of claim **1**, where the impedance measuring unit comprises a signal voltage or current measuring unit.

13. The apparatus of claim **12**, where at least one of the sub-loads is a loudspeaker.

14. A load detection method for a load comprising multiple frequency-dependant sub-loads, the method comprising:

measuring a representation of the impedance characteristic of the load;

calculating a quantity representing the shape of the impedance characteristic of the load;

providing stored representations of the shape of the impedance characteristics of the load resulting from different configurations of the sub-load; and

comparing the calculated quantity of the shape of the current impedance characteristic of the load with each one of the stored representations of the shape and, in case that the measured representation matches a stored representation, identifying the actual configuration of the sub-loads within the load.

15. The method of claim **14**, where the different configurations of the sub-loads within the load under test comprises at least one configuration in which at least one sub-load is in a fault condition.

16. The method of claim **15**, where the quantity representing the shape of the impedance characteristic of the load is the area, or an approximation thereof, between a measured impedance curve and a base line representing a constant threshold impedance measured at a pre-defined base frequency.

17. The method of claim **15**, where the quantity representing the shape of the impedance characteristic of the load is the slope, or an approximation thereof, of a measured impedance curve at least one pre-defined base frequency.

18. The method of claim **17**, where the slope is approximated as the average slope within a pre-defined frequency interval.

19. The method of claim **14**, where the load is an acoustic transducer comprising, as a sub load, at least one loudspeaker, and where the step of measuring a representation of the impedance characteristic of the load comprises providing a test signal having a spectrum that does not overlap with a spectrum audible for humans, whereby the test signal comprises a sinusoidal waveform truncated by a window function.

* * * * *

B.10 Power Distribution Arrangement

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(54) **POWER DISTRIBUTION ARRANGEMENT**

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Publication Classification

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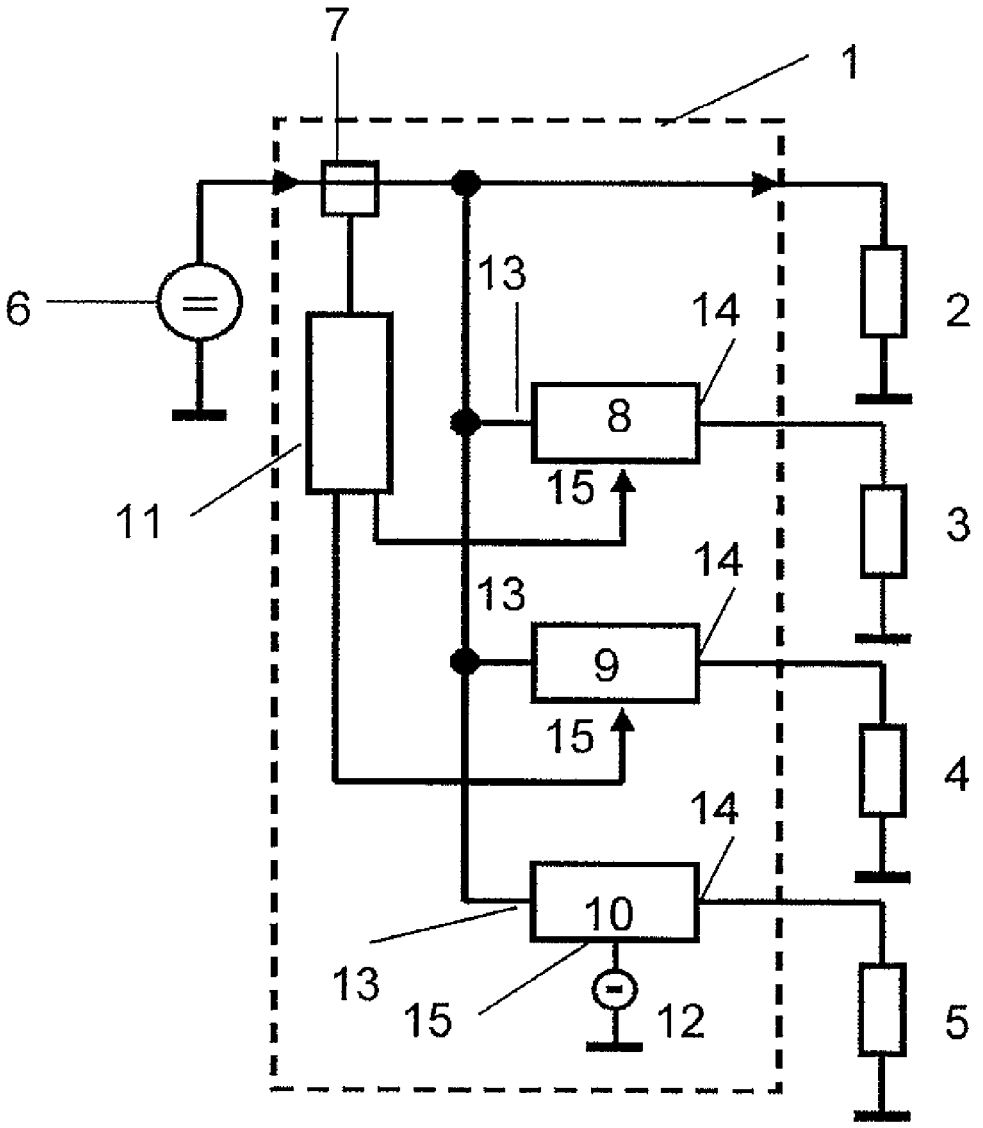
H02H 9/00 (2006.01)

(52) **U.S. Cl.** **361/18**

(57) **ABSTRACT**

An arrangement and a method for distributing power supplied by a power source to two or more of loads (e.g., electrical vehicular systems) is disclosed, where a representation of the power taken by a particular one of the loads from the source is measured. The measured representation of the amount of power taken from the source by the particular one of the loads is compared to a threshold to provide an overload signal in the event the representation exceeds the threshold. Control signals dependant on the occurring of the overload signal are provided such that the control signal decreases the output power of the power circuit in case the overload signal occurs.



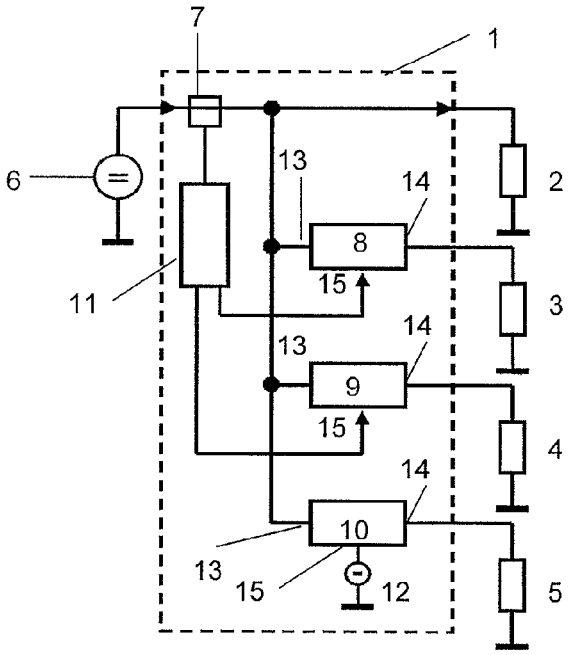


FIG 1

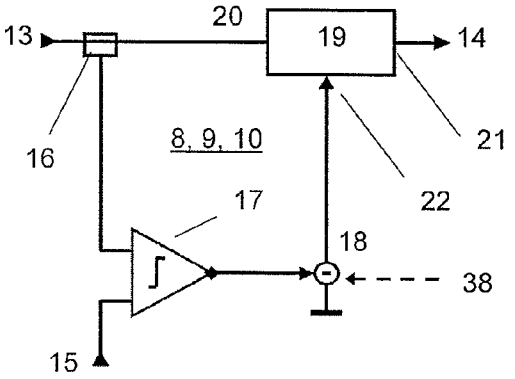


FIG 2

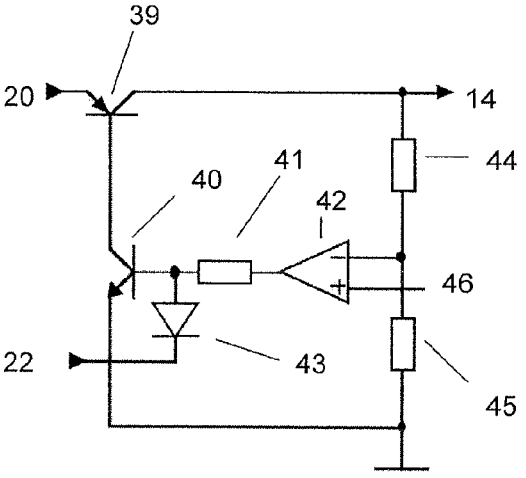


FIG 3

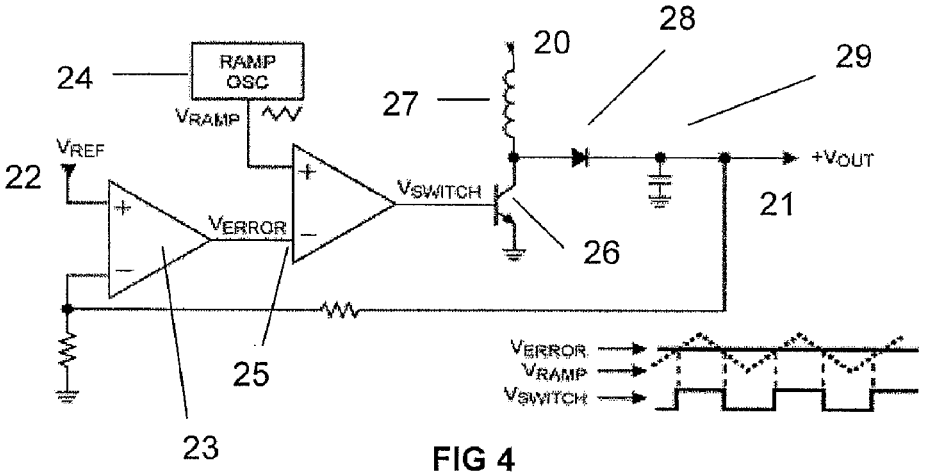
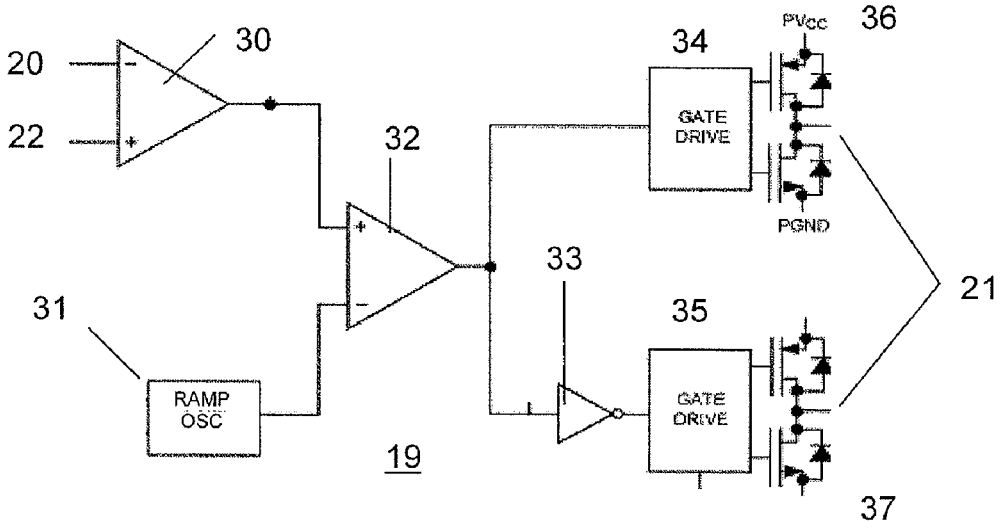

24
RAMP OSC
VRAMP
20
28
29
27
VREF
22
VSWITCH
+VOUT
21
VERROR
26
25
VERROR
VRAMP
VSWITCH
23

FIG 4


20
30
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PVcc
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GATE DRIVE
PGND
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21
31
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RAMP OSC
GATE DRIVE
19
37

FIG 5

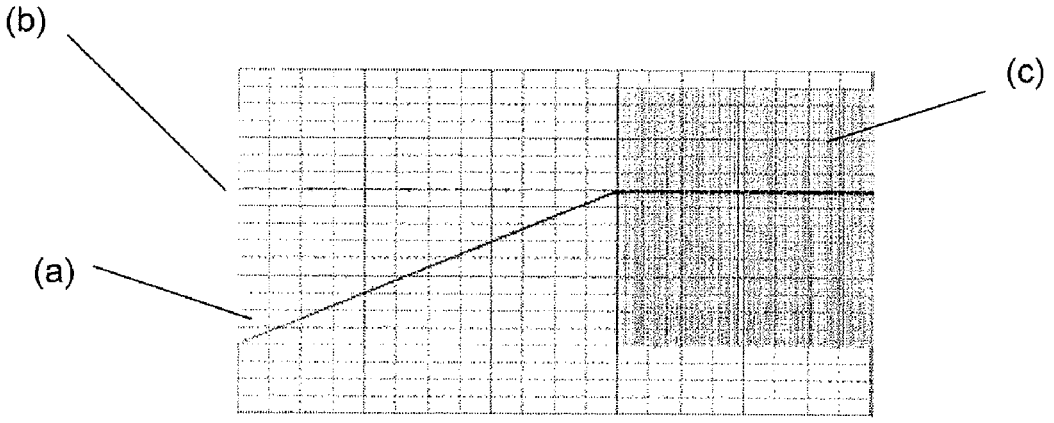

FIG 6

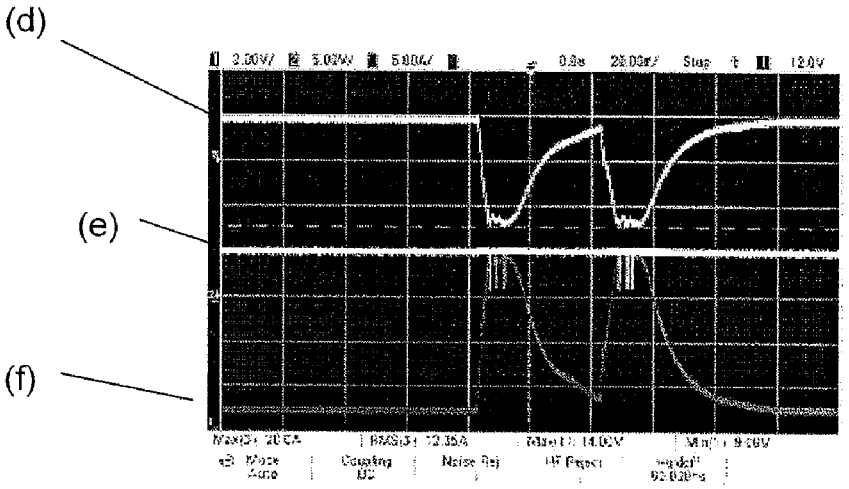

FIG 7

POWER DISTRIBUTION ARRANGEMENT

1. CLAIM OF PRIORITY

[0001] This patent application claims priority to European Patent Application serial number 08 013 706.0 filed on Jul. 30, 2008, which is hereby incorporated by reference in its entirety.

2. FIELD OF TECHNOLOGY

[0002] The present invention relates to the field of a power distribution arrangement to connect a multiplicity of loads to a power source, and a method of distributing power from a power source to a multiplicity of loads.

3. RELATED ART

[0003] Electrical power sources are by nature limited to a finite amount of power they can deliver. Connecting multiple loads to a power source may lead to overload situations where the power demand from the loads exceeds the maximum power that can be supplied by the source. One such power source may be, for example, the power system of a vehicle or aircraft. In this case, the source is established by one or more generators and batteries. The loads in such a vehicle may include motors, actuators, heating, lighting, and electronics. Depending on the situation different combinations of loads are applied to the power source. Selecting a power source for a possible maximum load would be uneconomic and environmentally unfriendly. Otherwise the above mentioned overload situations may occur.

[0004] In particular, when taking into account loads at extreme temperatures or loads with frequently changing power demands the source may be overloaded. In the case of aircraft and automotive applications, safety equipment is more important than comfort equipment. Comfort equipment like window heating, seat heating, air condition or entertainment equipment requires a lot of power from the power source, which may cause the source to be operated over its limit. Therefore, it is necessary to prioritize the loads to ensure operation of the more important equipment. Some of the above mentioned components regulate their output power to the desired level and therefore maintain a constant power demand from their source, even where the source is already saturated. Some of those loads may increase their input currents in case of a decreasing supply voltage such that their output power and, accordingly, their input power remains constant. In critical situations other more important components (e.g., safety equipment) might suffer from this constant power demand while the source is already at its limits. In this case, it is highly desirable to reduce the power of the comfort equipment for safety reasons.

[0005] Voltage sources are known that regulate the output current and limit it to a maximum value, for example, at turn on of power sinks such as power supplies. Other sources are connected to each other by a control channel to adapt the current limit. However, adaptation is limited by the transmission speed of the control channel. The known arrangements do not respond sufficiently fast to input current transients under both, normal or start-up conditions. In contrast, safety equipment is usually built in the hardware to take out any risk of software crashes and to enable the maximum speed of reaction to alerts. Therefore, there is a need for an input power limiting arrangement for limiting power over a wide frequency range or a short period of time.

SUMMARY OF THE INVENTION

[0006] According to one aspect of the invention, a power distribution system includes an input connected to a power source, two or more outputs, each output connected to one of a plurality of loads, and at least one power limiting unit connected between the input and one of the outputs is provided. The power limiting unit includes a power sensor, a power circuit, a comparison unit, and a control unit. The power sensor is connected between the input and the particular one of the outputs, and to measures a representation of the power supplied by the source to the respective load connected to the particular one of the outputs. The power circuit is connected in series to the power sensor, and supplies a regulated electrical output to a respective one of the loads. The power circuit includes a control element that receives a control signal. The comparison unit is coupled to the power sensor to receive the measured representation of the power supplied to the particular one of the outputs, and compare the measured representation to a threshold for providing an overload signal in case the measured representation exceeds the threshold. The control unit is connected to the comparison unit for receiving the overload signal and to the power circuit for providing the control signal and for limiting the control signal to a given value in case the overload signal is received.

[0007] According to another aspect of the invention, a power limiting unit for coupling a power source to at least one electrical vehicular system is provided. The power limiting unit includes a power sensor, a comparator, a controller and a power circuit. The power sensor measures current and/or voltage supplied to the vehicular system from the power source, and provides a measurement signal indicative thereof. The comparator receives and compares the measurement signal and a threshold signal, and provides an overload signal where the measurement signal is greater than the threshold signal. The controller receives the overload signal and provides a control signal associated with a command to draw less power. The power circuit includes a control element that receives the control signal. The power circuit regulates the supplied current and/or voltage to the vehicular system in response to the control signal.

[0008] According to another aspect of the invention, a power distribution system for coupling a power source to a plurality of electrical vehicular systems which includes first and second vehicular systems is provided. The power distribution system includes a power management unit and a plurality of power limiting units. The power management unit provides a threshold signal. Each power limiting unit includes power sensor, a comparator, a controller, and a power circuit. The power sensor measures electrical power supplied to one of the vehicular systems from the power source, and provides a measurement signal indicative thereof. The comparator receives and compares the measurement signal and the threshold signal, and provides an overload signal when the measurement signal is greater than the threshold signal. The controller receives the overload signal and provides a control signal. The power circuit includes a control element that receives the control signal. The power circuit regulates the supplied current and/or voltage to the one of the vehicular systems in response to the control signal.

[0009] According to still another aspect of the invention, a method for distributing power supplied by a power source to

a plurality of electrical vehicular systems is provided. The method includes (i) measuring a representation of the power taken by a particular one of the vehicular systems from the source, (ii) regulating an output power dependant on a control signal, (iii) comparing the measured representation of the power taken from the source by the particular one of the vehicular systems to a threshold for providing an overload signal where the measured representation exceeds the threshold, and (iv) providing control signals dependant on the occurring of the overload signal such that the control signal decreases the output power of the power circuit where the overload signal occurs.

DESCRIPTION OF THE DRAWINGS

[0010] The invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, instead emphasis being placed upon illustrating the principles of the invention. Moreover, in the figures, like reference numerals designate corresponding parts. In the drawings:

[0011] FIG. **1** is a block diagram of an example of a novel power distribution arrangement;

[0012] FIG. **2** is a block diagram of an exemplary power limiting unit for use in the power distribution arrangement of FIG. **1**;

[0013] FIG. **3** is a block diagram of a linear voltage regulator for use in the power limiting unit of FIG. **2**;

[0014] FIG. **4** is a block diagram of a DC-DC converter as a power circuit for use in the power limiting unit of FIG. **2**;

[0015] FIG. **5** is a block diagram of a switch-mode audio amplifier as a power circuit for use in the power limiting unit of FIG. **2**;

[0016] FIG. **6** is a diagram illustrating the results of simulations of the power distribution arrangement shown in FIG. **1**; and

[0017] FIG. **7** is a diagram illustrating the results of measurements of the power distribution arrangement shown in FIG. **1**.

DETAILED DESCRIPTION

[0018] Referring to FIG. **1**, a power distribution system **1** for coupling a plurality of loads, e.g., 2, 3, 4, 5 to a power source **6** comprises a current sensor **7**, a plurality of power limiting units, e.g., 8, 9, 10, a total-power management unit **11**, and a reference voltage source **12**. The loads may be any kind of load such as ohmic, inductive, and capacitive loads as well as combinations thereof. The loads may be established by, e.g., motors, actuators, heating, lighting, electronics, or the like. The power source **6** may be a power net and comprise one or more power generators and/or one or more batteries that are not shown for the sake of simplicity. The power source may be, e.g., a current source or a voltage source. The power limiting units **8**, **9**, **10** limit the power consumed by its respective load to a certain amount, by decreasing the voltage and/or the current supplied to its associated load, accordingly.

[0019] Each of the power limiting units **8**, **9**, **10** includes a power input **13** coupled to the source **6** through the power sensor **7**, a power output **14** connected to the respective load, and a threshold input **15** to receive a threshold representing a value to which the amount of power is to be limited. The threshold inputs **15** of the power limiting units **8** and **9** are connected to the total-power management unit **11** that provides the respective thresholds depending on the total power required by the loads **2**, **3**, **4**, and **5**. The power limiting unit **10** receives a fixed threshold from the reference voltage source **12**. In the present example, voltages are supplied to the threshold inputs **15** of the power limiting units **8**, **9**, **10** to define the respective thresholds, but any other kind of signal is applicable as well.

[0020] In the present example, the highest priority is assigned to the first load **2**, such that it is supplied with all the power it requires as far as this amount of power can be provided by the source **6**. Second highest priority is assigned to the fourth load **5** that is supplied with all the power it requires provided this amount of power is under a fixed limit set by the threshold and the source **6** is able to deliver this amount of power. The second and third loads **3** and **4** have lowest priority and are supplied with each a certain share of the amount of power that is not required by the first and fourth loads **2** and **5**, respectively, and that evaluated by the total-power management unit **11** such that the actual power consumed by the loads **2-5** is measured by a power sensor, in the present example the current sensor **7** but also may be a voltage sensor under certain conditions, and compared to the maximum power that can be provided by the source **6**. The difference between the actual and the maximum power is shared in a fixed or dynamically controlled ratio by the second and third loads **3** and **4**.

[0021] FIG. **2** illustrates the power limiting unit **10** for use in the power distribution system **1** of FIG. **1**. The current sensor **7** (FIG. **1**) is connected to the input terminal **13** and measures the amount of current supplied to the respective load connected to power output terminal **14** and provides a representation thereof, e.g., a voltage that is proportional to the current flowing into the load. This voltage is supplied to a comparator **17**, which compares the voltage representing the load current and, accordingly, the power consumed by the load, to a reference voltage that is applied to the threshold input **15** and that forms a power threshold.

[0022] A control unit, in the present example a controllable voltage source **18**, is connected to the comparator **17**, such that the reference voltage provided by the voltage source **18** is dependent on the current measured by the current sensor **16**. The reference voltage provided by the voltage source **18** is supplied as a control signal to a power circuit **19** that comprises a power input terminal **20**, a power output terminal **21**, and a control signal input **22**. The power circuit **19** may be, for example, an AC-DC converter, a power factor controller, a pulse width modulator or, as discussed below with reference to FIGS. **4**, **5**, and **6**, a linear voltage regulator, a DC-DC converter or switch-mode power amplifier, respectively.

[0023] Thus, a representation of the power consumed by the each of the power limiting circuits **8**, **9** or **10** together with one of the loads **3**, **4**, or **5** is measured by the current sensor **16**. The power circuit **19** regulates its output power dependant on the control signal provided by the voltage source **18**. The control signal depends on an overload signal provided by the comparator **17** to decrease the output power of the power circuit **19** in case the overload signal occurs. The measured representation of the power supplied by the source **6** to the particular load is compared to a threshold and the overload signal is provided in case the representation succeeds/exceeds the threshold.

[0024] Accordingly, the power circuit **19** is connected in series to the current sensor **16**, serving as a power sensor, and supplies a regulated output voltage or a regulated output current or both to the respective load. The power circuit **19**

comprises a control element such as the transistors **26**, **36**, **37**, **39** in the power circuits shown in FIGS. **3**, **4**, and **5**, that receives a control signal. The comparator **17** is coupled to the current sensor **16** and receives a voltage as a measured representation of the power supplied to the particular one of the outputs and compares this representation to a threshold voltage for providing an overload signal in case the representation succeeds the threshold. The controlled voltage source **18** limits the control signal to a given value, e.g., a certain voltage when it receives the overload signal from the comparison unit. The voltage provided by controllable voltage source **18** may be such that the drive transistor(s) is switched off or clamped to provide a maximum output voltage or current when the overload signal occurs may be adjusted by a signal **38**.

[0025] FIG. **3** is a block diagram of the power limiting unit **19** of FIG. **2**. The power input terminal **20** is connected to the emitter of the transistor **39**, whose collector is connected to the power output terminal **14**. The voltage at the power output terminal **14** is fed back via a voltage divider established by resistors **44**, **45**, a differential amplifier **42** connected to a reference voltage **46**, a resistor **41** in the output branch of the amplifier **42**, and a npn bipolar transistor **40** whose emitter collector path is connected between the base of the transistor **39** and ground. The base of the transistor **40** is further connected to the voltage source **18** through a diode **43** and the terminal **22**. The voltages to be provided by the voltage source **18** in the event an overload signal occurs or not, are such that it does not influence the voltage provided by the amplifier **42** when no overload is detected. However, in an overload situation, it is such that the voltage at the base of the transistor **40** is limited to a value that that the transistor **39** is switched off or clamped.

[0026] FIG. **4** is a block diagram of an exemplary DC-DC converter establishing a switch-mode power circuit **19** for use in the power limiting unit of FIG. **2**. Such converter may be of the boost, buck, or inverter (flyback), push-pull, half-bridge, full-bridge, Sepic type or a combination thereof. A common control method, as used in the power circuit **19** of FIG. **4**, uses pulse-width modulation (PWM). In this method, a sample of an output voltage V_{OUT} is taken and subtracted, in a subtractor **23**, from a reference voltage V_{REF} at the reference terminal **22** to generate an error signal V_{ERROR}. This error signal V_{ERROR} is compared to a ramp signal V_{RAMP} received from a ramp oscillator **24** (e.g., a sawtooth oscillator). The comparison takes place in a comparator **25** outputting a digital signal V_{SWITCH} that controls the power switch **26** switching an inductance **27**. The alternating voltage at the junction of the switch **26** and the inductance **27** is rectified by a diode **28** and a capacitor **29** to generate the output voltage V_{OUT}. When the output voltage V_{OUT} changes, the error signal V_{ERROR} also changes and thus causes the threshold of the comparator **25** established by the error signal V_{ERROR} to change. Consequently, the output pulse width (PWM) changes. This duty cycle change then moves the output voltage to reduce the error signal to zero, thus completing the control loop. Changing the duty cycle controls the steady-state output with respect to the input voltage. This is a key concept governing all inductor-based switching circuits.

[0027] FIG. **5** is a block diagram of a switch-mode audio amplifier establishing a power circuit for use in the power limiting unit of FIG. **2**. A switch-mode audio amplifier comprises an input preamplifier **30**, a ramp oscillator **31** (e.g., a sawtooth oscillator), a comparator **32**, and a H-bridge comprising an inverter **33**, two MOSFET drivers **34** and **35**, and two output stages **36** and **37**, each having two MOSFET power transistors. The comparator **32** samples a signal received from the preamplifier **30**, with the oscillator frequency determining the duration of the sampling period. Thus, the oscillator frequency is an important factor in the overall performance of a Class D amplifier. The preamplifier **30** is supplied with the input signal at the terminal **20** and the reference signal at the terminal **22**. The comparator **32** outputs a pulse-width modulated square wave that drives the H-bridge. The H-bridge then outputs the square wave differentially, and provides a low-impedance source to, e.g., a LC filter and a loudspeaker (both not shown) as load.

[0028] The current sensors **7**, **16** (FIGS. **1** and **2**) in the above examples may be any known type, e.g., current sensors comprising Hall elements, inductive sensors, resistive elements (shunts) and the like. The output of such current sensors is usually a voltage that is easier to handle by the circuitry connected downstream of the current sensor. The measured current represents the power consumed by the respective load(s) assuming that the voltage of the source **6** is essentially constant. As the voltage output by the current sensor is proportional to the current to be measured, the voltage is a representation of the power consumed.

[0029] The measured power consumption is compared to an adjustable maximum power threshold represented by the threshold voltage at the terminal **15**, in the following comparator **17**. The maximum power threshold may be adjusted under control of the total-power management unit **11** using adequate algorithms. When an overload situation is detected by the comparator **17** a given stable reference voltage is applied to the power circuit **19** by the control unit **18**. This reference voltage **22** is equal or lower than the one in the regular mode (non-overload situation). In some cases the overload reference voltage may be zero so that the power circuit **19** is switched off. The reference voltage may also be linked to the threshold voltage in a certain manner and, accordingly, be controlled by the total-power management unit **11**. This ensures both, slow software and fast hardware control of the limiting functionality and transfers the signal into the dynamics of the control of the power circuit **19**.

[0030] In the examples illustrated above, the power sensor is connected upstream of the power circuit, i.e., between the input terminal and the power circuit, so that the regulation loop of the power circuit does not include the power sensor and the comparison unit resulting in a very fast response time.

[0031] Major advantages of the novel arrangement and method include a fast response time to a given maximum input energy level; a software independent energy control that better fulfils safety requirements; an input limitation also for high frequent energy demands; and a fast recovery time from overload situations.

[0032] The fast limiting function is activated by an excessive input current being above the specified threshold. The maximum speed of the limiting function depends on the delay of the comparison to the threshold.

[0033] As can be seen from FIG. **6**, the set point is never exceeded, although the voltage source is heavily overloaded. Its simulation results are shown in FIG. **6** where the curve (a) is a representation of the actual input current, line (b) represents the adjusted maximum current reference, and curve (c) shows the reference path to the of the power circuit **19** to control the power consumed.

[0034] Measurements on a prototype verified the simulations and are shown in FIG. **7** where curve (d) depicts the voltage of an overloaded voltage source, curve (f) a current at a peak load demand, curve (e) the response of the control unit thereto.

[0035] Referring again to FIG. **1**, at least one of the loads **3**, **4**, and **5** may be a loudspeaker. In particular, the loudspeaker may be part of a motor vehicle infotainment system. The respective power circuits **8**, **9**, and **10** may be of the type shown in FIG. **2** having power circuits **19** as illustrated in FIG. **3** or **4** and a switch-mode audio amplifier as illustrated in FIG. **5** connected downstream thereof. The respective reference voltages **22** of the power circuit including in a cascaded manner the voltage regulator (shown in FIG. **3** or **4**) and the amplifier (shown in FIG. **5**) are controlled simultaneously by the comparator **17** so that, e.g., both the power circuit and the load are switched off simultaneously and, thus, problems occurring with different load-source situations are avoided.

[0036] Although various exemplary embodiments of the invention have been disclosed, it will be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the spirit and scope of the invention. It will be obvious to those reasonably skilled in the art that other components performing the same functions may be suitably substituted. Such modifications to the inventive concept are intended to be covered by the appended claims.

What is claimed is:

1. A power distribution system comprising an input connected to a power source, two or more outputs, each output connected to one of a plurality of loads, and at least one power limiting unit connected between the input and one of the outputs, the power limiting unit comprising:

a power sensor connected between the input and the particular one of the outputs, and adapted to measure a representation of the power supplied by the source to the respective load connected to the particular one of the outputs;

a power circuit connected in series to the power sensor, and supplies a regulated electrical output to a respective one of the loads, the power circuit comprising a control element that receives a control signal;

a comparison unit coupled to the power sensor to receive the measured representation of the power supplied to the particular one of the outputs, and compare the measured representation to a threshold for providing an overload signal in case the measured representation exceeds the threshold; and

a control unit connected to the comparison unit for receiving the overload signal and to the power circuit for providing the control signal and limiting the control signal to a given value in case the overload signal is received.

2. The arrangement of claim **1**, where the power sensor comprises a current sensor and the measured representation of the power supplied to the load connected to the particular one of the outputs is a voltage that is proportional to the current measured.

3. The arrangement of claim **2**, where the comparison unit compares the voltage representing the current measured to a threshold voltage.

4. The arrangement of claim **1**, where the control signal provided to the power circuit is a reference voltage.

5. The arrangement of claim **4**, where, in case the measured representation exceeds the threshold, the value of the control signal, is lower than in a non-overload mode of operation.

6. The arrangement of claim **1**, where the power circuit comprises a DC-DC converter.

7. The arrangement of claim **1**, where the power circuit comprises a switch-mode power amplifier.

8. The arrangement of claim **1**, where the regulated electrical output of the power circuit is set by the control signal in case of an occurrence of an overload signal to a value below the power represented by the threshold.

9. The arrangement of claim **1**, where at least two power limiting units are connected between the input and each of the at least two power limiting units uniquely therewith; each power limiting unit having a particular threshold corresponding to characteristics of the respective load and a priority assigned to the load.

10. The arrangement of claim **1**, further comprising a power management unit that provides the threshold to the power limiting units.

11. The arrangement of claim **10**, where the power management unit evaluates the total power supplied by the power source and sets the thresholds according to the priority and the power available.

12. The arrangement of claim **9**, where the thresholds are fixed.

13. The arrangement of claim **1**, where the control signal is such that the control element is switched off.

14. The arrangement of claim **1**, where the power sensor is connected electrically upstream of the power circuit.

15. A method for distributing power supplied by a power source to a plurality of electrical vehicular systems, comprising:

measuring a representation of the power taken by a particular one of the vehicular systems from the source;

regulating an output power dependant on a control signal;

comparing the measured representation of the power taken from the source by the particular one of the vehicular systems to a threshold for providing an overload signal when the measured representation exceeds the threshold; and

providing control signals dependant on the occurring of the overload signal such that the control signal decreases the output power of the power circuit where the overload signal occurs.

16. A power limiting unit for coupling a power source to at least one electrical vehicular system, the power limiting unit comprising:

a power sensor that measures current and/or voltage supplied to the electrical vehicular system from the power source, and provides a measurement signal indicative thereof;

a comparator that receives and compares the measurement signal and a threshold signal, and provides an overload signal when the measurement signal is greater than the threshold signal;

a controller that receives the overload signal and provides a control signal associated with a command for less electrical power; and

a power circuit that includes a control element that receives the control signal, which power circuit regulates the supplied current and/or voltage to the vehicular system in response to the control signal.

17. The power limiting unit of claim **16**, where the power circuit comprises a DC-DC converter.

18. The power limiting unit of claim **16**, where the power circuit comprises a switch-mode power amplifier.

19. The power limiting unit of claim **16**, where the power circuit is configured to maintain the supplied current and/or voltage below the threshold signal where the measurement signal is greater than the threshold signal.

20. A power distribution system for coupling a power source to a plurality of electrical vehicular systems which includes first and second vehicular systems, the power distribution system comprising:

a power management unit that provides a threshold signal; and

a plurality of power limiting units each uniquely associated with one of the plurality of electrical vehicular system, each unit comprising

a power sensor that measures electrical power supplied to the associated one of the electrical vehicular systems from the power source, and provides a measurement signal indicative thereof;

a comparator that receives and compares the measurement signal and the threshold signal, and provides an overload signal when the measurement signal is greater than the threshold signal;

a controller that receives the overload signal and provides a control signal; and

a power circuit that includes a control element that receives the control signal, which power circuit regulates the electrical power to the one of the vehicular systems in response to the control signal.

21. The power distribution system of claim **20**, where the power circuit comprises a DC-DC converter.

22. The power distribution system of claim **20**, where the power circuit comprises a switch-mode power amplifier.

23. The power distribution system of claim **20**, where the plurality of power limiting units includes first and second power limiting units, and where the threshold received by the comparator in the first power limiting unit is different than the threshold received by the comparator in the second power limiting unit.

24. The power distribution system of claim **20**, further comprising a total power sensor that measures electrical power collectively supplied to the plurality of vehicular systems from the power source, and provides a total measurement signal indicative thereof.

25. The power distribution system of claim **24**, where the power management unit sets the thresholds received by the comparators in the power limiting units according to priority assigned to each of the power limiting units and the total measurement signal.

26. The power distribution system of claim **24**, where the total power sensor is located upstream of the power circuits in the power limiting units.

27. The power distribution system of claim **20**, where the power management unit provides a threshold signal to each power limiting unit.

28. The power distribution system of claim **27**, where at least one of the threshold signals is fixed.

* * * * *

B.11 Controllable Circuit

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(54) **CONTROLLABLE CIRCUIT**

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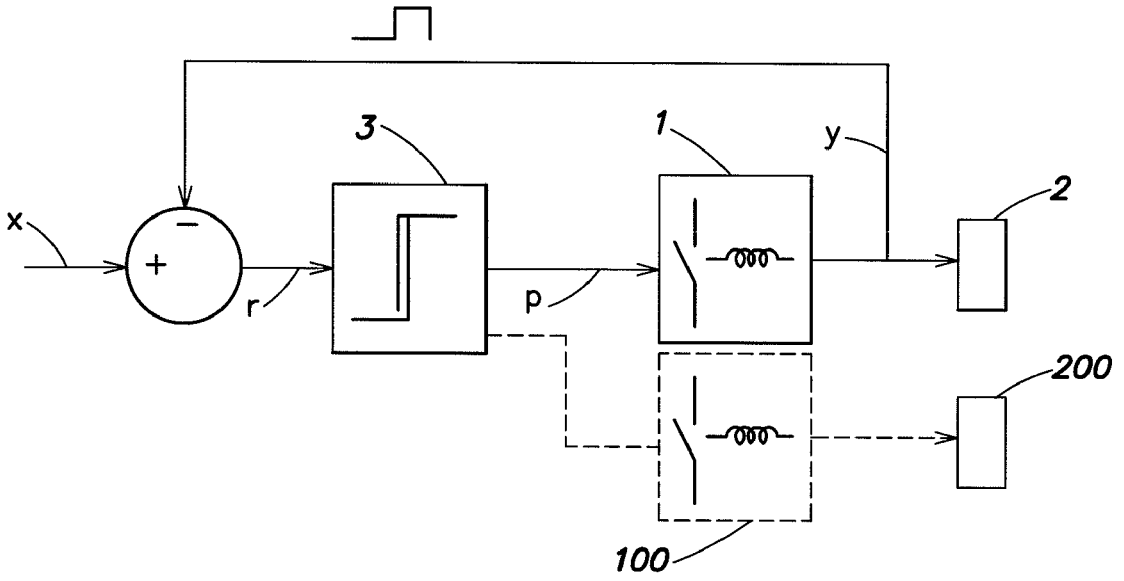
G05F 1/10 (2006.01)

(52) **U.S. Cl.** **323/282**

(57) **ABSTRACT**

A switch-mode power circuit comprises a controllable element and a control unit. The controllable element is configured to control a current in response to a control signal supplied to the controllable element. The control unit is connected to the controllable element and provides the control signal. The control unit comprises a first signal processing unit, a second signal processing unit, and a combiner unit. The first signal processing unit has an output and is supplied with a first carrier signal and an input signal. The second signal processing unit has an output and is supplied with a second carrier signal and the input signal. The combiner unit is connected to the first and second signal processing units combining the outputs of the first and the second signal processing units to form a signal representative of the control signal.



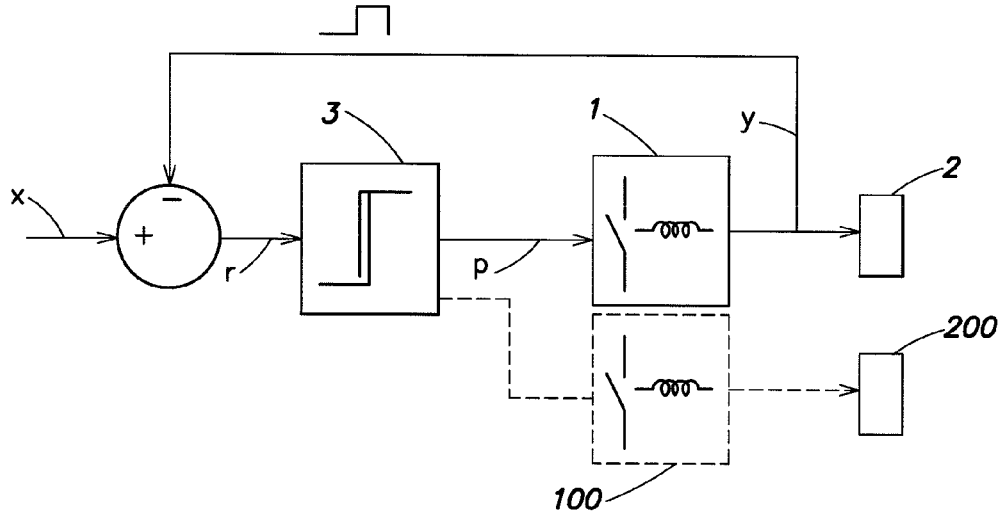
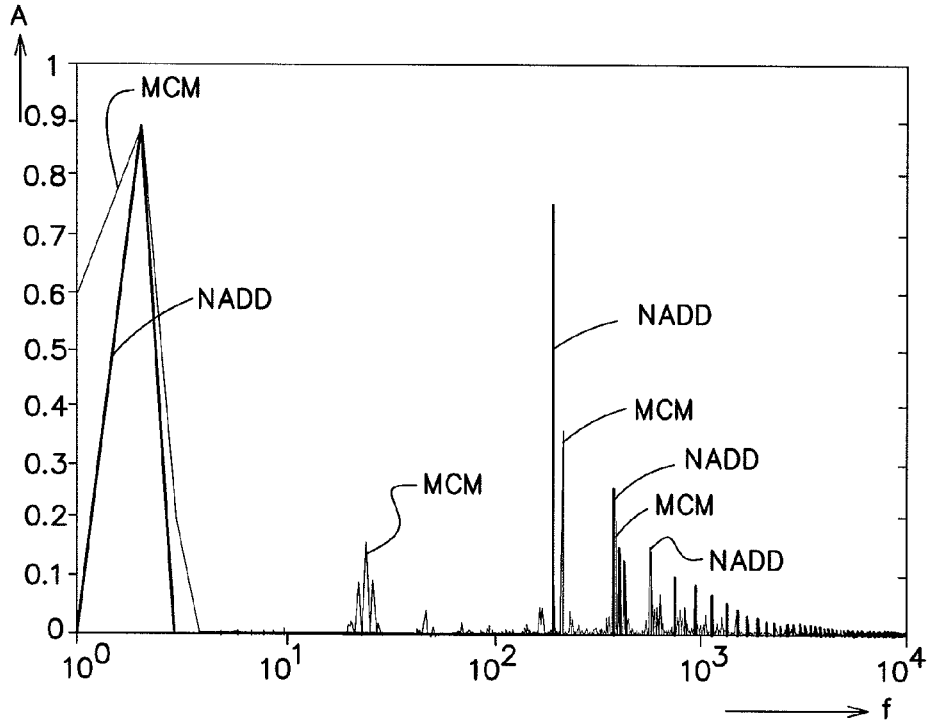

3
1
y
2
x
+
−
r
p
200
100

FIG. 1


A
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
MCM
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10^3
10^4
f

FIG. 2

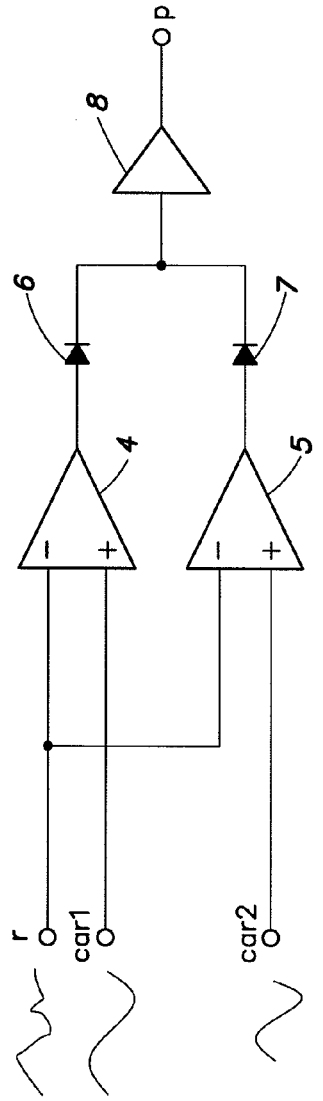


FIG. 3

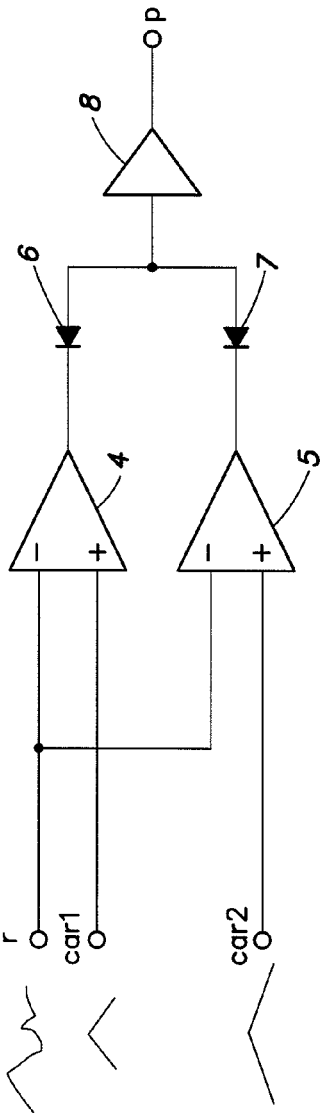


FIG. 4

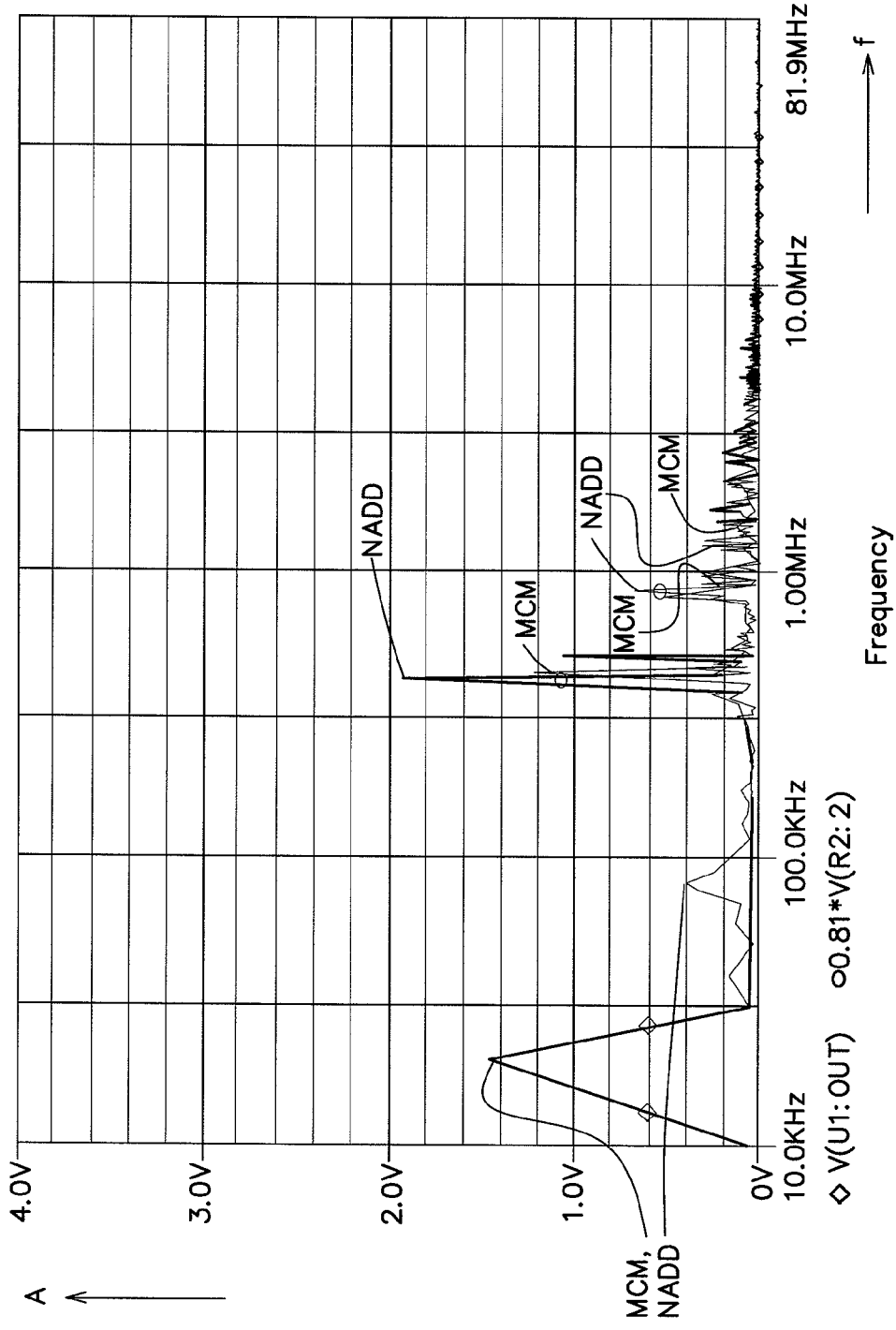

4.0V
3.0V
2.0V
1.0V
0V
A
10.0KHz
100.0KHz
1.00MHz
10.0MHz
81.9MHz
f
Frequency
◇ V(U1:OUT)
○0.81*V(R2:2)
NADD
MCM
NADD
MCM
MCM
MCM,
NADD

FIG. 5

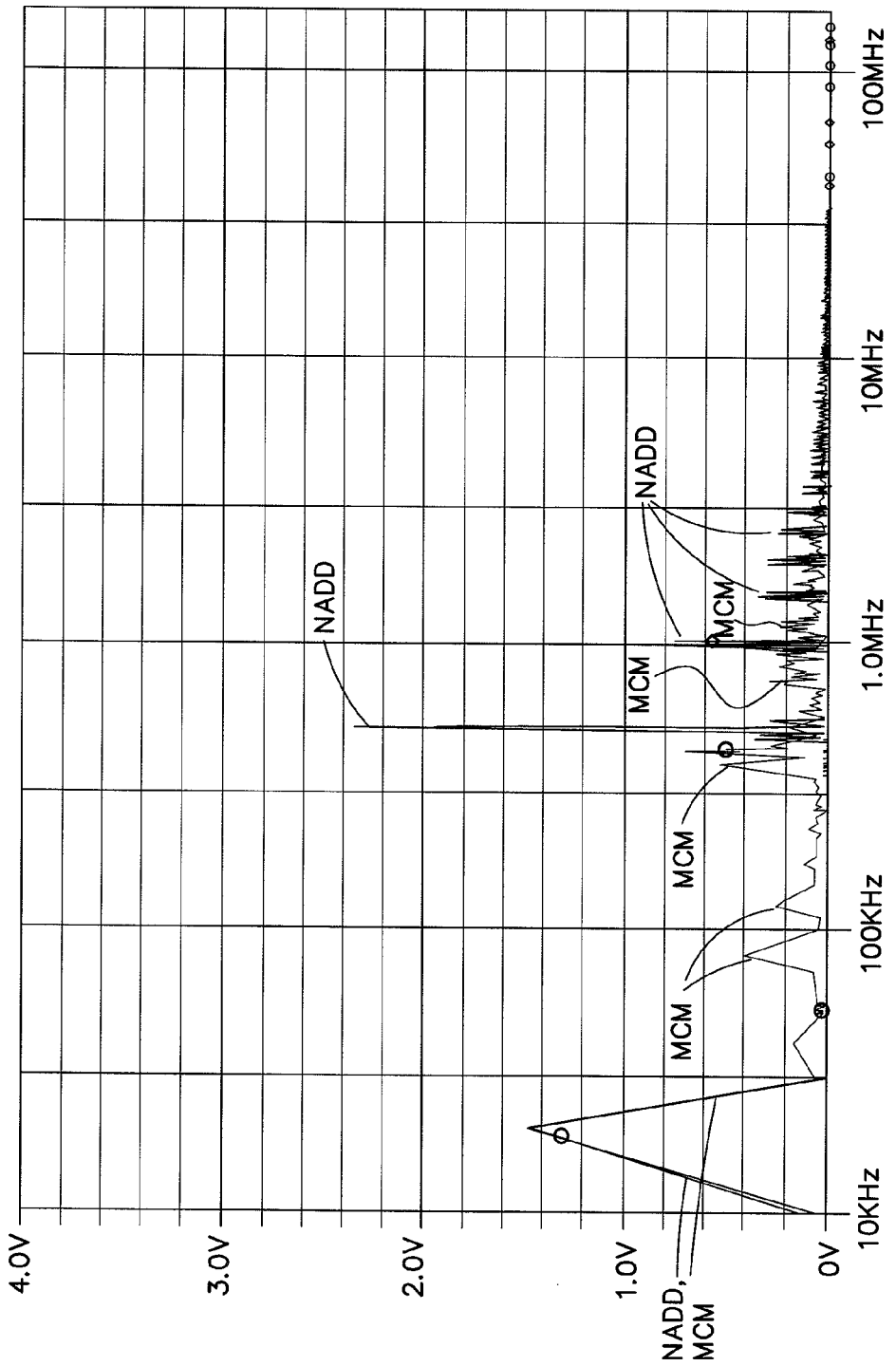

4.0V
3.0V
2.0V
1.0V
0V
NADD, MCM
10KHz
100KHz
1.0MHz
10MHz
100MHz
Frequency
NADD
MCM
MCM
MCM
NADD
MCM
NADD
o 0.85*V (R2:2)
◇ V(D1:2)

FIG. 6

OR

in_1	in_2	out
0	0	0
0	1	1
1	0	1
1	1	1

Mean Value = 75% Ones

AND

in_1	in_2	out
0	0	0
0	1	0
1	0	0
1	1	1

Mean Value = 25% Ones

FIG. 7

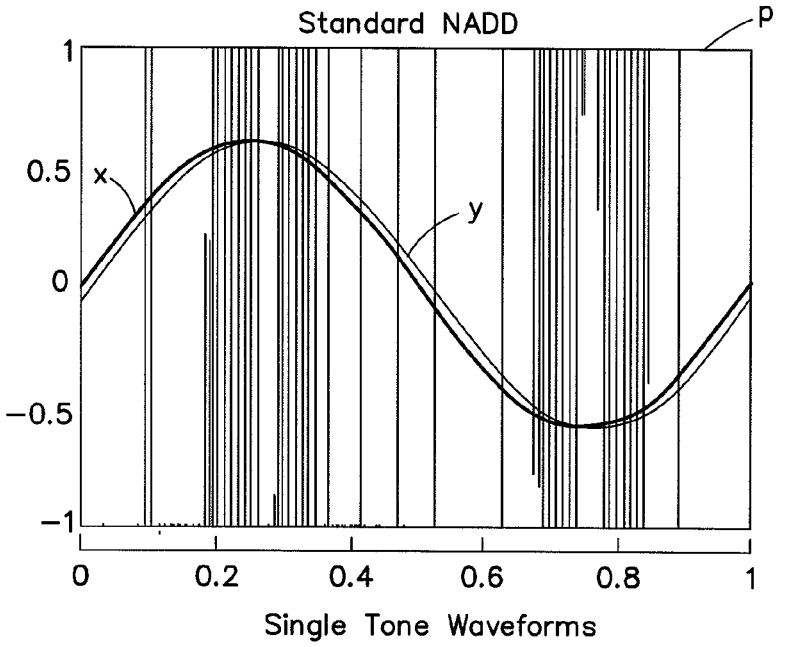

Standard NADD
p
1
0.5
0
−0.5
−1
x
y
0
0.2
0.4
0.6
0.8
1
Single Tone Waveforms

FIG. 8A

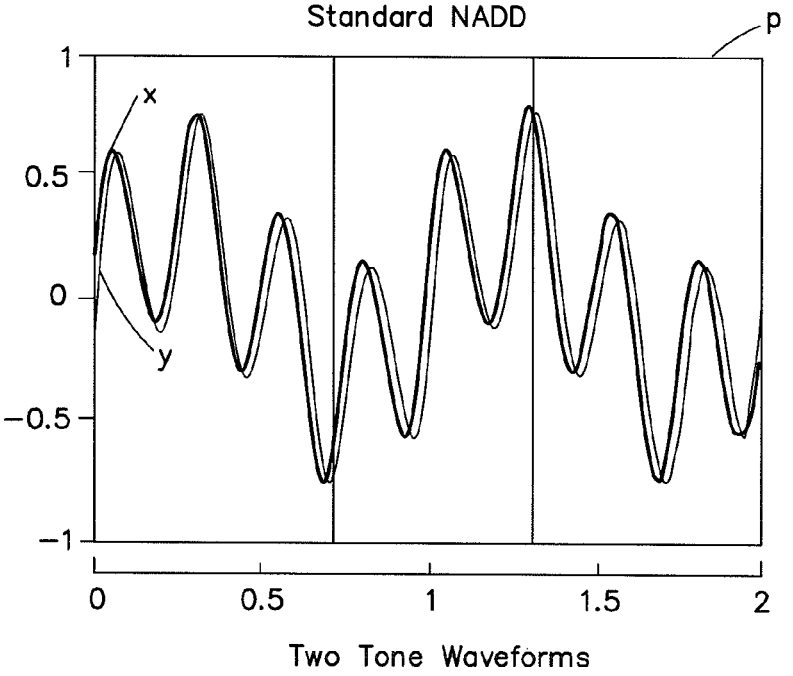

Standard NADD
p
1
0.5
0
−0.5
−1
x
y
0
0.5
1
1.5
2
Two Tone Waveforms

FIG. 8B

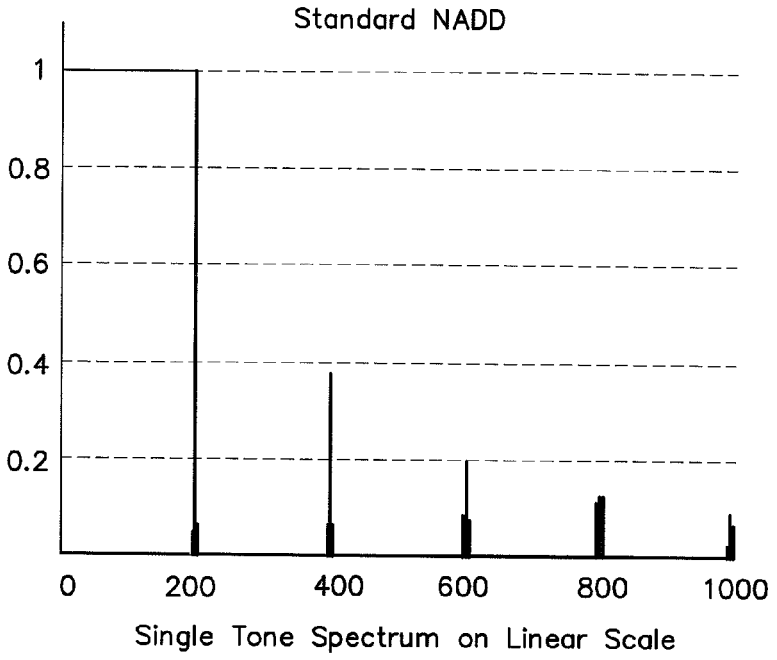

Standard NADD
1
0.8
0.6
0.4
0.2
0
200
400
600
800
1000
Single Tone Spectrum on Linear Scale

FIG. 8C

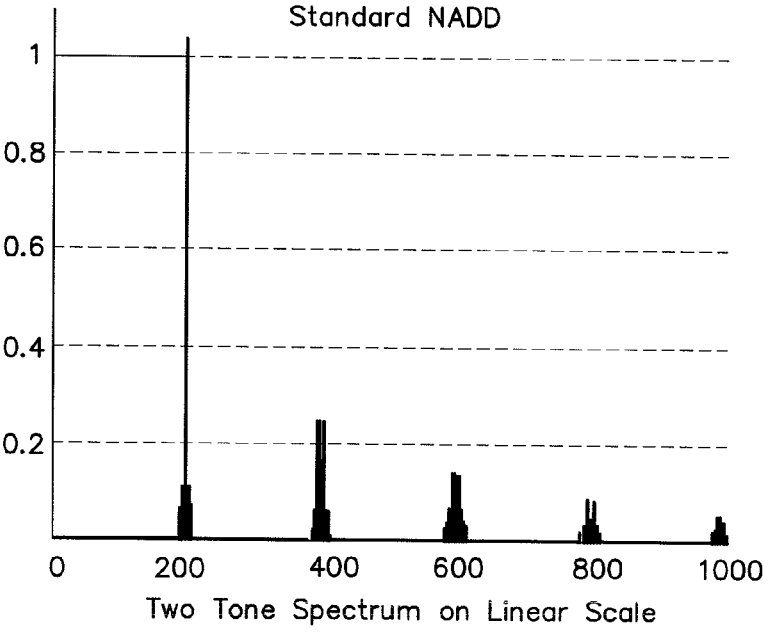
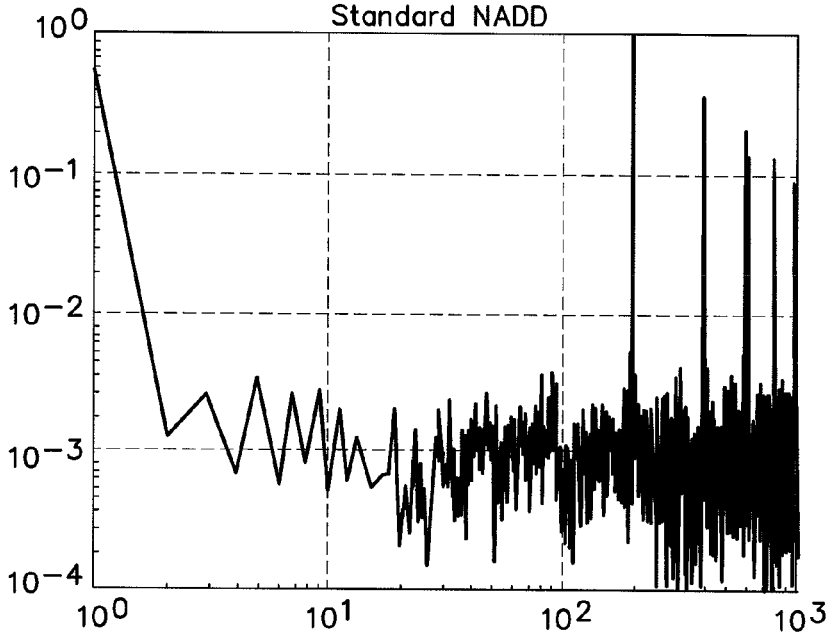
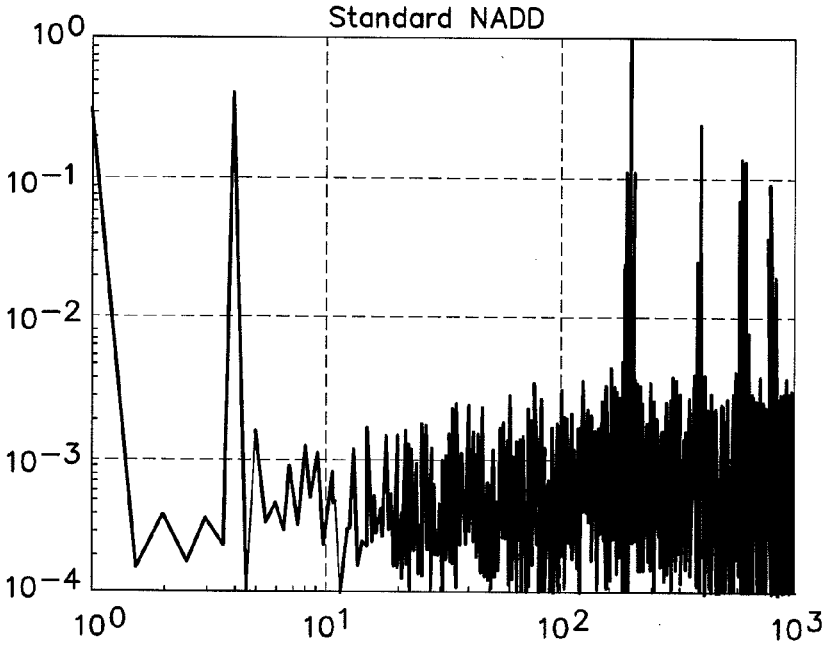

Standard NADD
1
0.8
0.6
0.4
0.2
0
200
400
600
800
1000
Two Tone Spectrum on Linear Scale

FIG. 8D



Single Tone Spectrum
on Logarithmic Scale
$\chi = 0.6 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$

FIG. 8E



Two Tone Spectrum
on Logarithmic Scale
$\chi = 0.35 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4\ \text{Hz} \cdot t)$

FIG. 8F

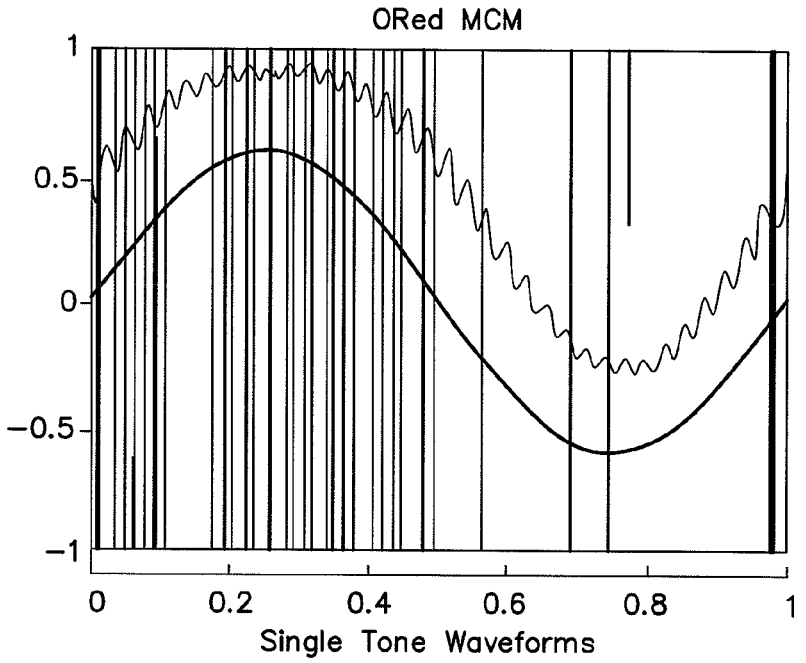

ORed MCM
1
0.5
0
−0.5
−1
0
0.2
0.4
0.6
0.8
1
Single Tone Waveforms

FIG. 9A

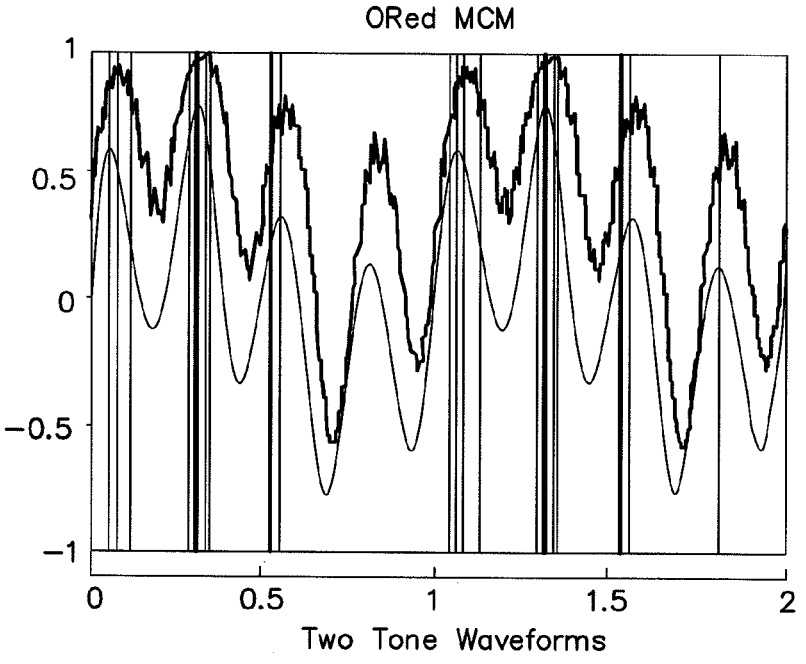

ORed MCM
1
0.5
0
−0.5
−1
0
0.5
1
1.5
2
Two Tone Waveforms

FIG. 9B

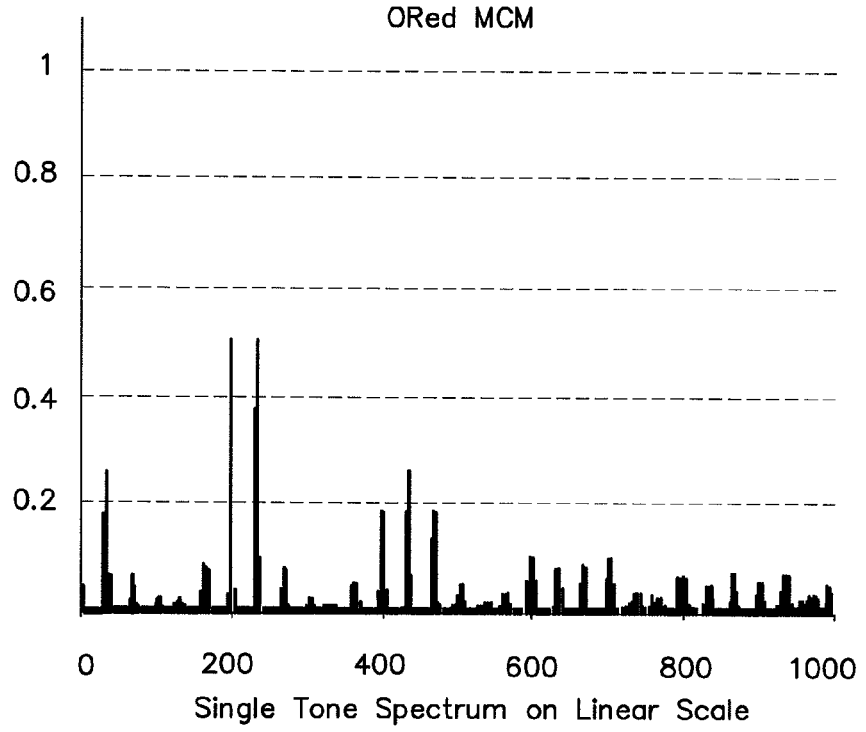

ORed MCM
1
0.8
0.6
0.4
0.2
0
200
400
600
800
1000
Single Tone Spectrum on Linear Scale

FIG. 9C

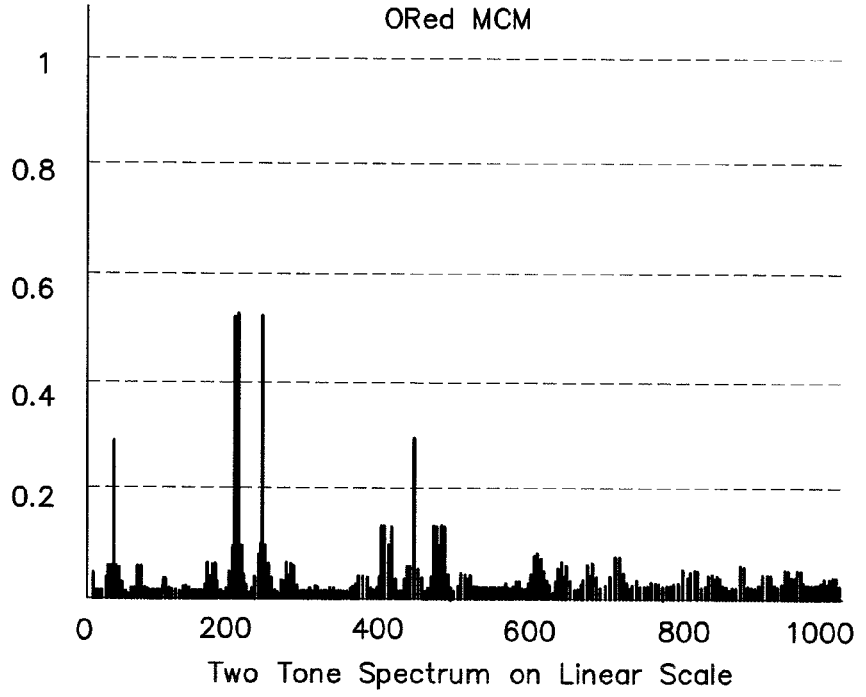
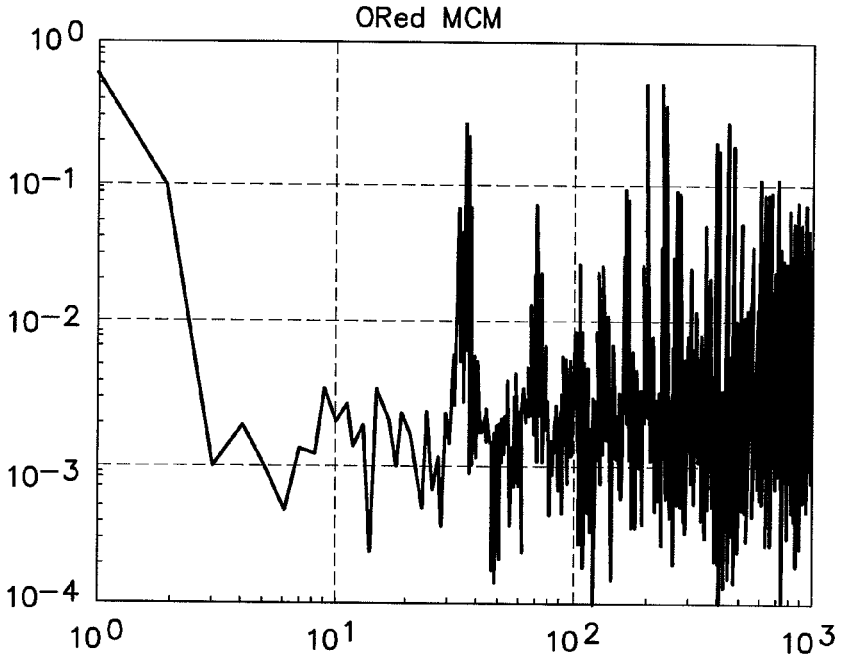
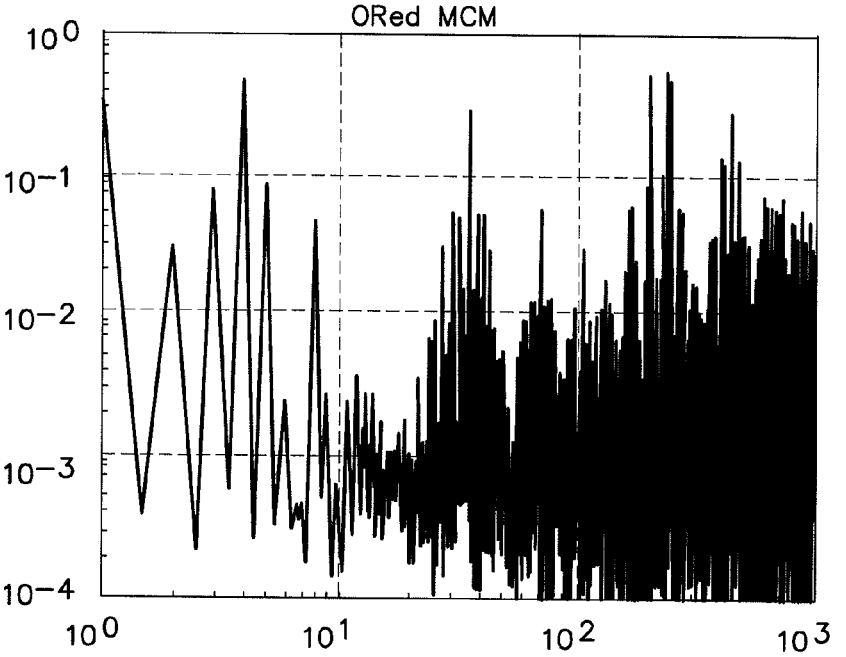

ORed MCM
1
0.8
0.6
0.4
0.2
0
200
400
600
800
1000
Two Tone Spectrum on Linear Scale

FIG. 9D



Single Tone Spectrum
on Logarithmic Scale
$X = 0.6 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$

FIG. 9E



Two Tone Spectrum
on Logarithmic Scale
$X = 0.35 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4\ \text{Hz} \cdot t)$

FIG. 9F

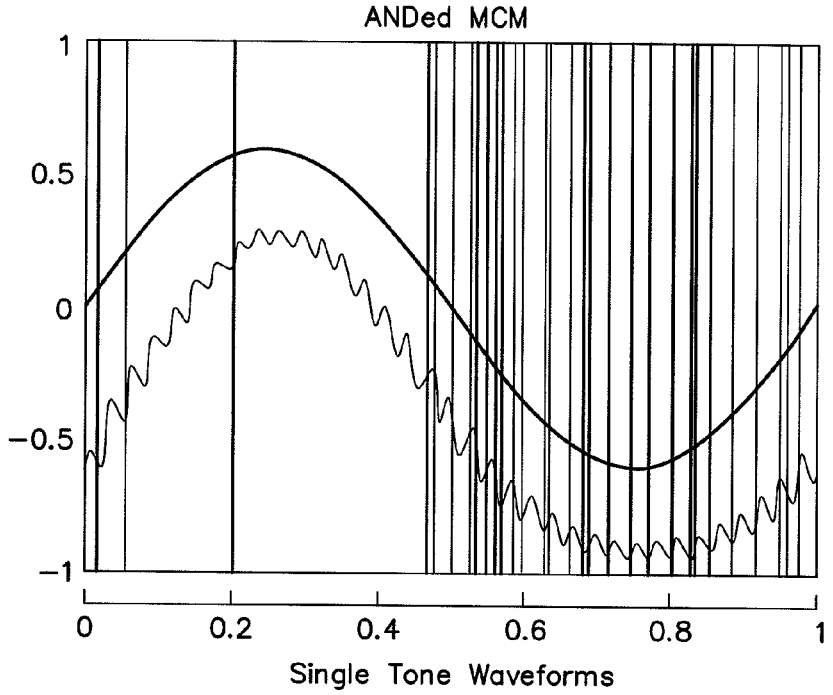


FIG. 10A

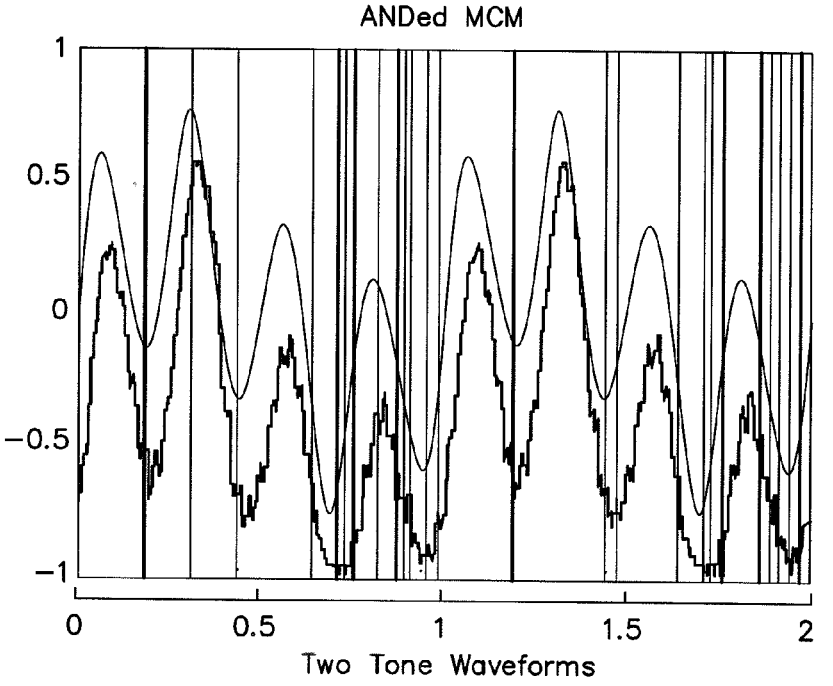


FIG. 10B

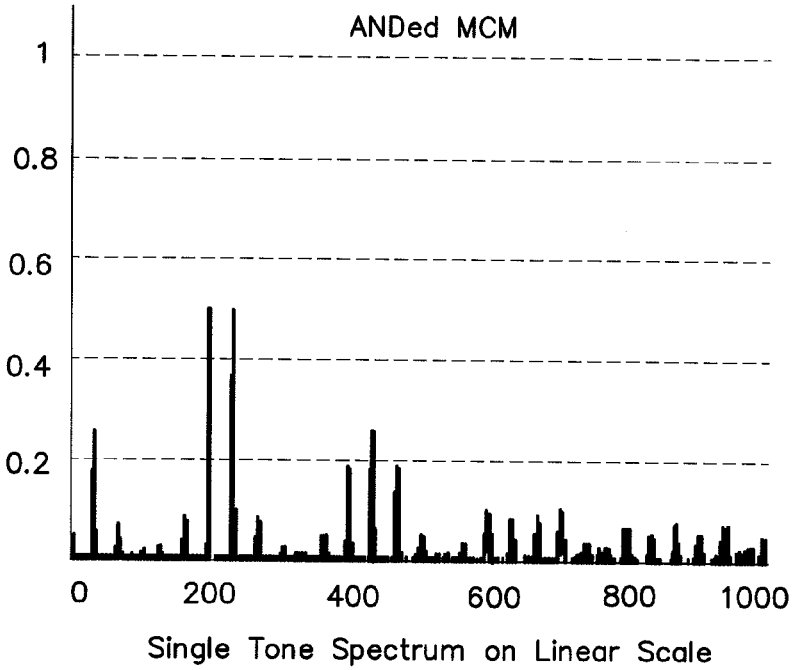


FIG. 10C

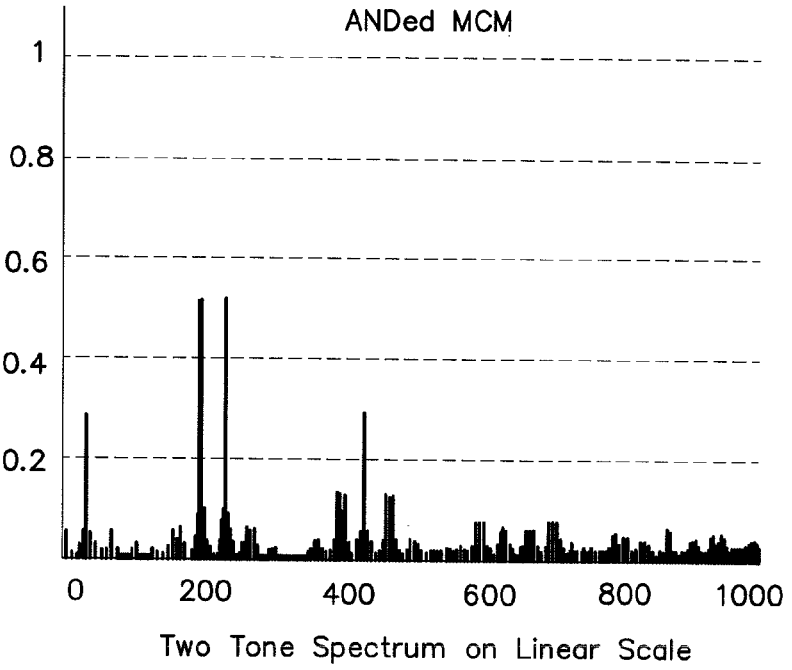
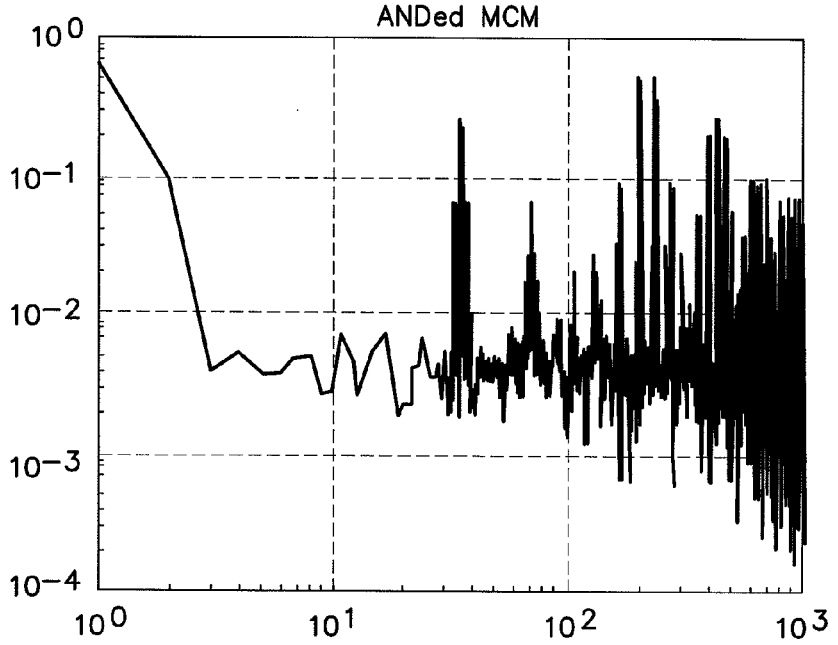
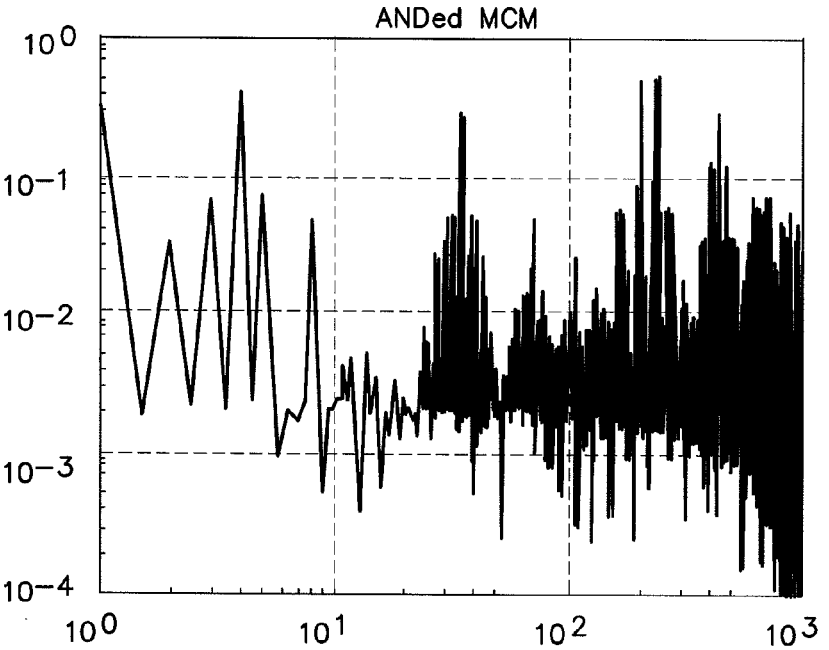


FIG. 10D



Single Tone Spectrum
on Logarithmic Scale
$X = 0.6 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$

FIG. 10E



Two Tone Spectrum
on Logarithmic Scale
$X = 0.35 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4\ \text{Hz} \cdot t)$

FIG. 10F

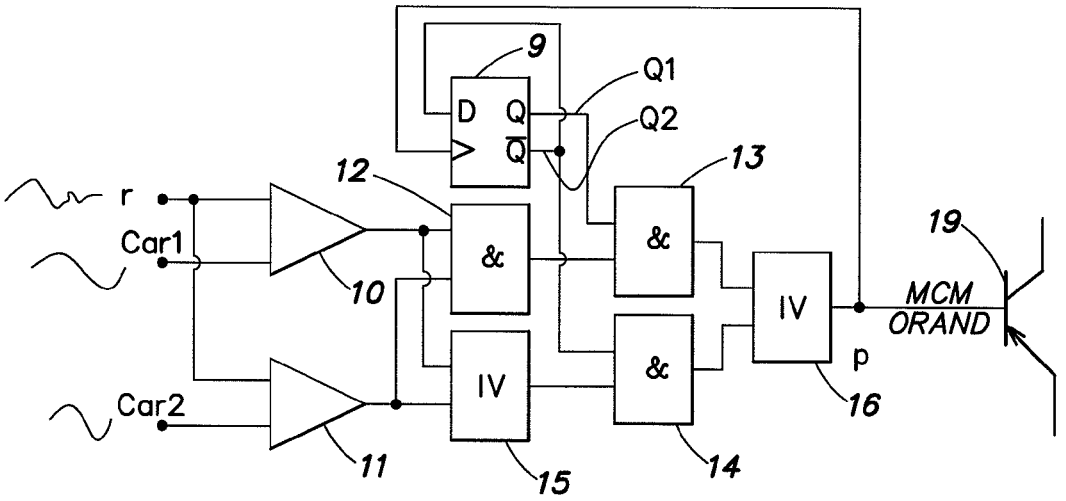

9
Q1
Q2
D
Q
12
13
r
Car1
&
&
19
MCM
ORAND
IV
10
&
p
Car2
IV
16
11
15
14

FIG. 11

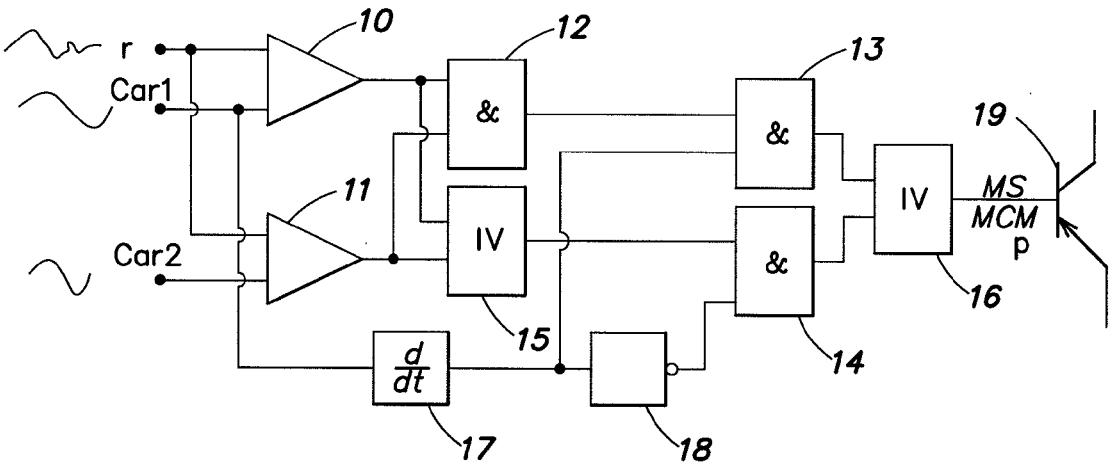

10
12
13
r
Car1
&
&
19
IV
MS
MCM
p
11
IV
&
Car2
16
15
d/dt
14
17
18

FIG. 13

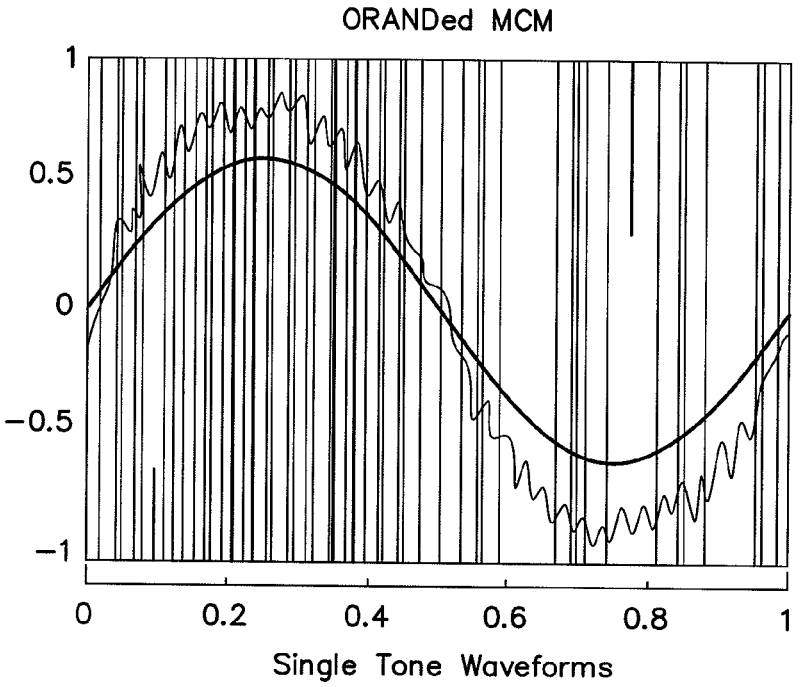


FIG. 12A

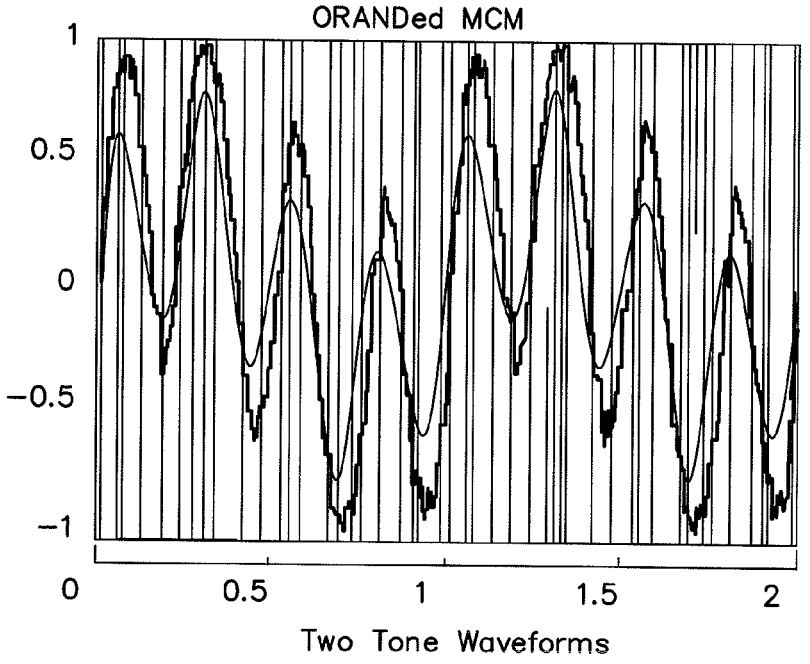


FIG. 12B

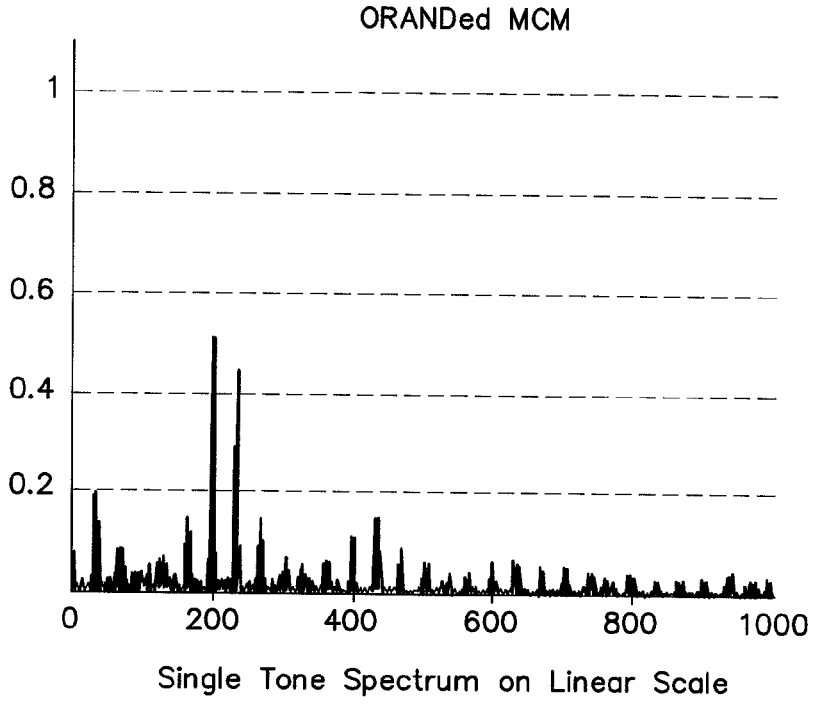


FIG. 12C

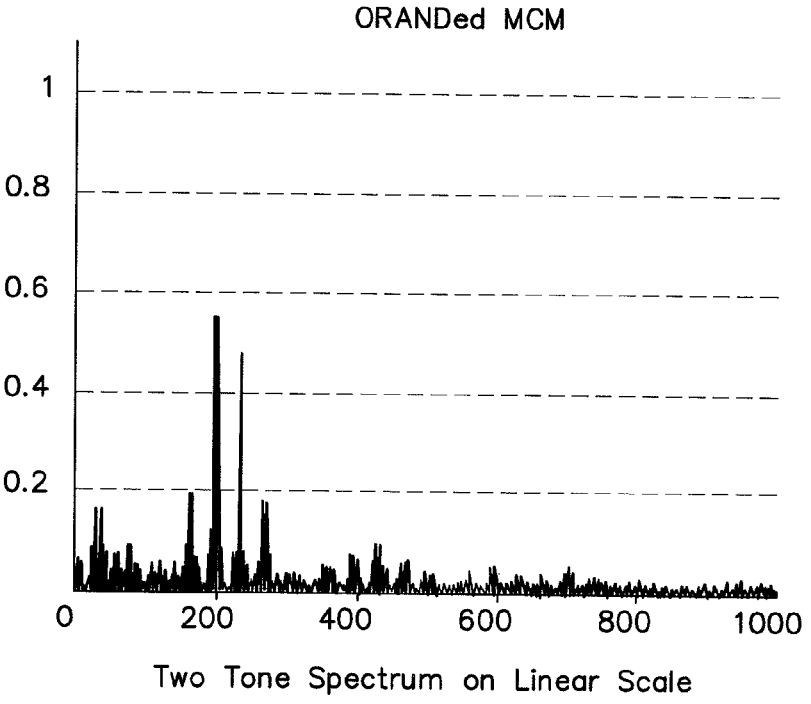
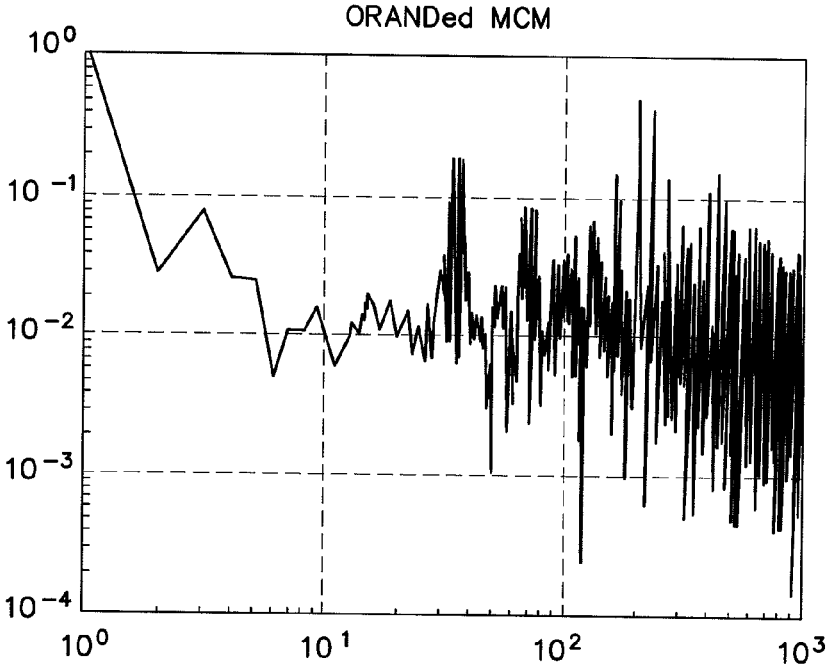


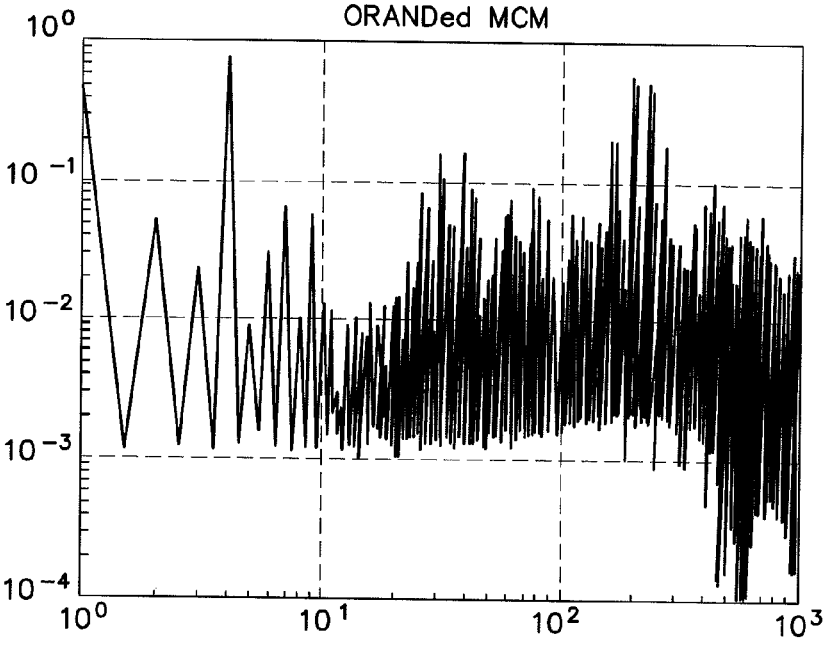
FIG. 12D



Single Tone Spectrum on Logarithmic Scale

$x = 0.6 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$

FIG. 12E



Two Tone Spectrum on Logarithmic Scale

$x = 0.35 \cdot \sin(2 \cdot \pi \cdot 1\ \text{Hz} \cdot t)$
$+0.45 \cdot \sin(2 \cdot \pi \cdot 4\ \text{Hz} \cdot t)$

FIG. 12F

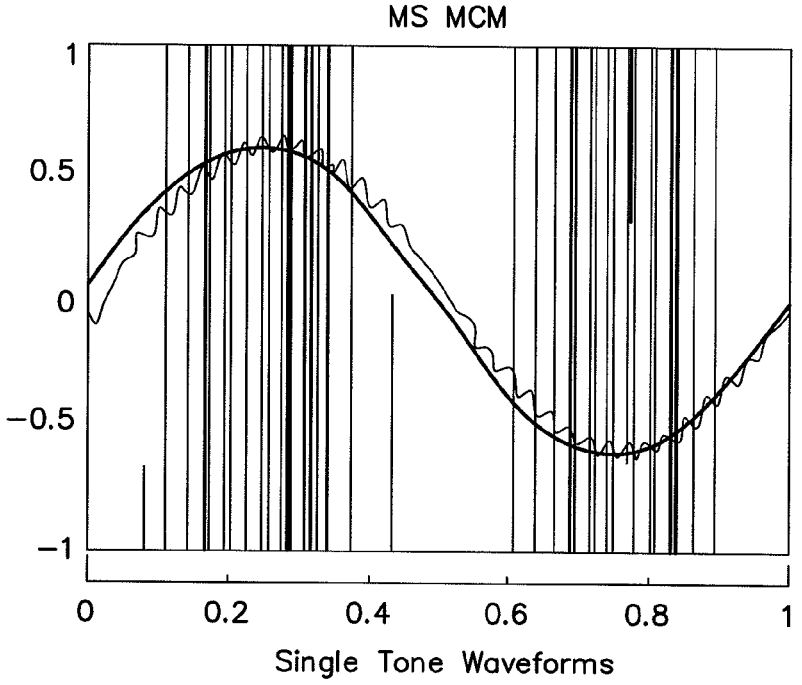


FIG. 14A

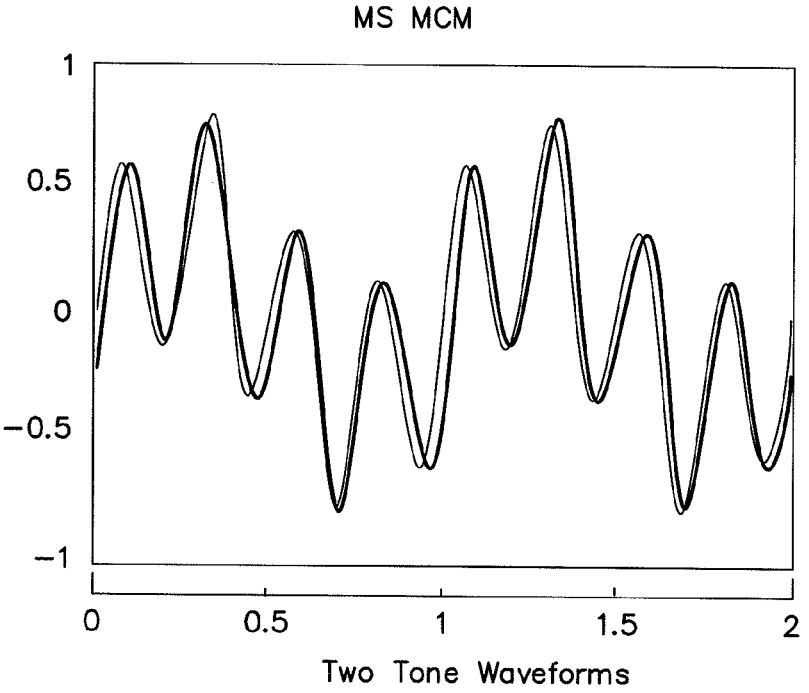


FIG. 14B

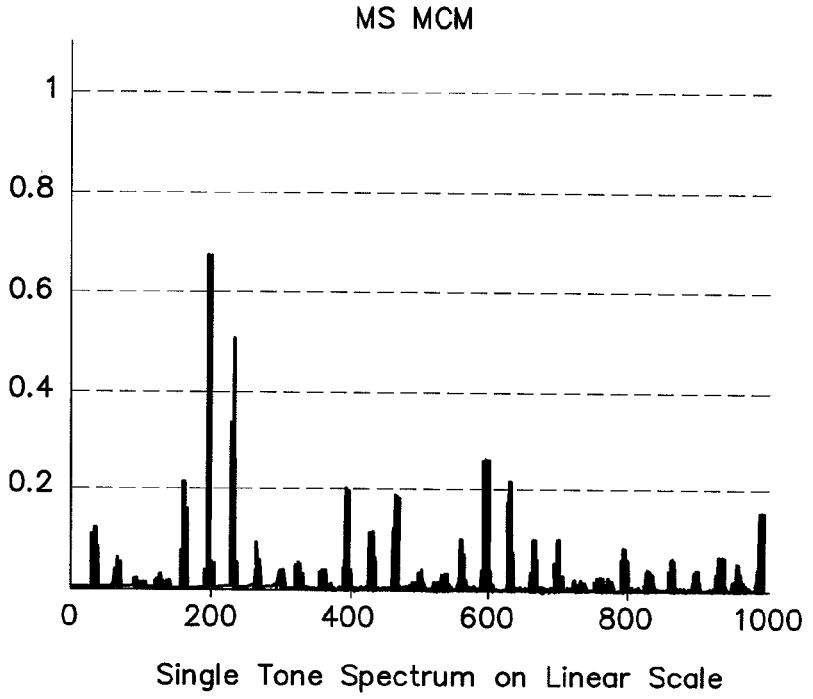


FIG. 14C

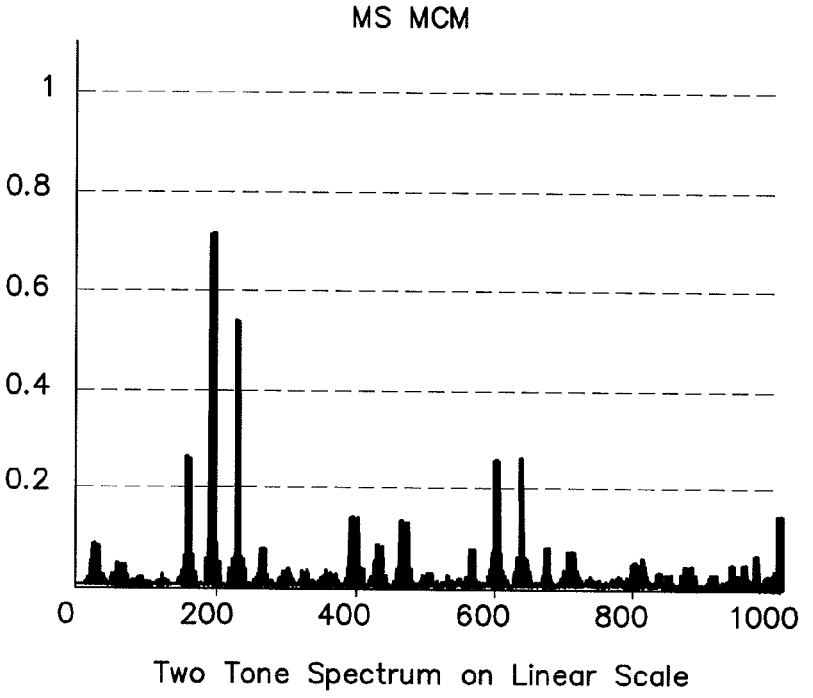


FIG. 14D

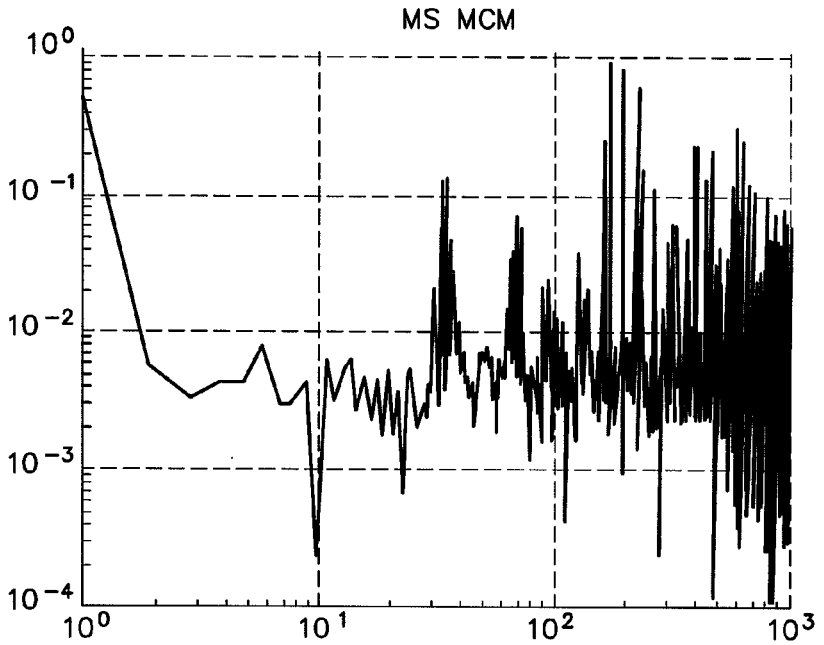


FIG. 14E

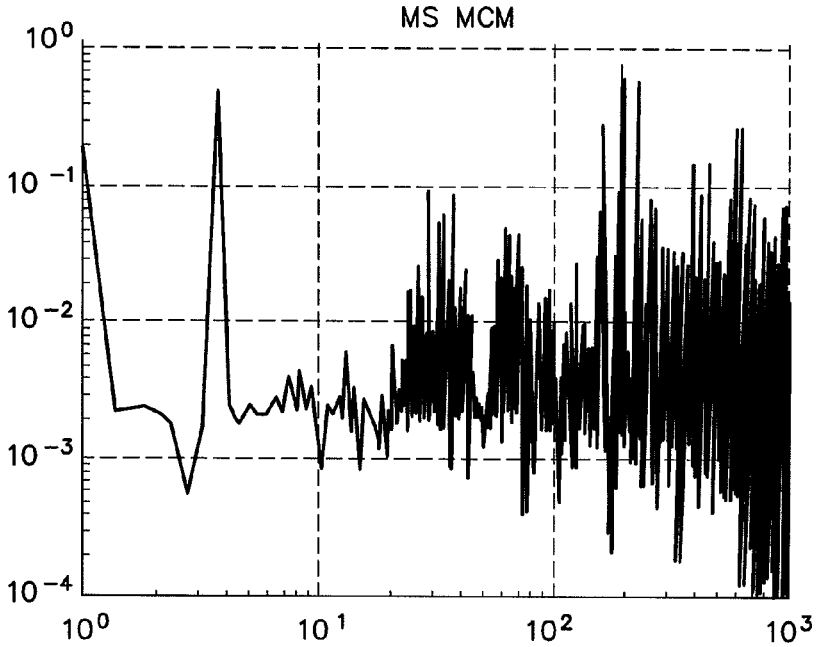


FIG. 14F

CONTROLLABLE CIRCUIT

CLAIM OF PRIORITY

[0001] This patent application claims priority to European Patent Application serial number 07 021 329.3 filed on Oct. 31, 2007.

FIELD OF THE INVENTION

[0002] This invention relates to control circuits, and in particular to switch-mode power circuits.

RELATED ART

[0003] Switch-mode power circuits generate a broad band spectrum due to their high speed signals. Such broad band spectral components can disturb other electronic equipment like receivers used in communication systems. Approaches to lower high frequency signal contents in switch-mode power circuits lead to extensive filter components and shielding. The filter components are bulky, expensive and dissipative due to the need to be designed for high voltage and current levels. The implementation of shielding is difficult as the mechanical efforts need to be combined with electrical isolation due to different electrical potentials on various conductive elements of power components. Consequently, compromises are made between good thermal design and good electrical design.

[0004] There is a general need to improve switching power circuits for the reasons outlined above.

SUMMARY OF THE INVENTION

[0005] A switch-mode power circuit comprises a controllable element and a control unit. The controllable element controls a current in response to a control signal provided by the control unit. The control unit comprises a first signal processing unit, a second signal processing unit, and a combiner unit. The first signal processing unit has an output and is supplied with a first carrier signal and an input signal. The second signal processing unit has an output and is supplied with a second carrier signal and the input signal. The combiner unit is connected to the first and second signal processing units combining the outputs of the first and the second signal processing units to form a signal representative of the control signal.

DESCRIPTION OF THE DRAWINGS

[0006] The invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, instead emphasis being placed upon illustrating the principles of the invention. Moreover, in the figures, like reference numerals designate corresponding parts. In the drawings:

[0007] FIG. **1** is a block diagram illustration of a switch-mode power circuit;

[0008] FIG. **2** is a diagram showing a comparison between a single carrier modulated signal and a multi carrier modulated signal;

[0009] FIG. **3** is a block diagram illustration of an ORed multi carrier modulator arrangement;

[0010] FIG. **4** is a block diagram illustration of an ANDed multi carrier modulator arrangement;

[0011] FIG. **5** shows simulation results of ORed MCM with two carriers;

[0012] FIG. **6** shows simulation results of ORed MCM with three carriers;

[0013] FIG. **7** shows the statistical distribution of ones and zeros in OR and AND operations;

[0014] FIGS. **8A-8F** show waveforms and spectra of a known single carrier modulation;

[0015] FIG. **9** shows waveforms and spectra of an ORed multi carrier modulation;

[0016] FIG. **10** shows waveforms and spectra of an ANDed multi carrier modulation;

[0017] FIG. **11** is a block diagram illustration of a circuit arrangement that switches after each output pulse between ORed modulation and ANDed modulation;

[0018] FIG. **12** shows waveforms and spectra of the two-carrier modulation arrangement of FIG. **11**;

[0019] FIG. **13** is a block diagram illustration of a circuit arrangement that switches dependant on a master carrier; and

[0020] FIG. **14** shows waveforms and spectra of the two-carrier modulation arrangement of FIG. **13**.

DETAILED DESCRIPTION

[0021] FIG. **1** is a block diagram illustration of an example of a switch-mode power circuit comprising, as a controllable element, a controllable switch **1** that switches a current through a load **2** dependant on a control signal p supplied to the switch **1** by a control unit **3** connected to the switch **1**. The switch **1** may be, for example, a transistor such as a bipolar transistor, a MOS field effect transistor or other suitable transistors. In other examples, the control signal and an inverted control signal may control an array of switches **1**, **100**, for example, configured in a half bridge or a full bridge arrangement. The load **2**, for example, may be a coil of a switched power supply, a voice coil of a loudspeaker, an ohmic load provided by a heating element, or other suitable switch-mode power circuits. The control unit **3**, for example, comprises, as a signal processing unit, a modulator arrangement. In one example, the modulator arrangement is configured as a frequency or pulse width modulator arrangement providing a signal p whose frequency or pulse width is dependant on a modulation signal r. The modulation signal r, supplied to the control unit **3**, forms an input signal illustrated in equation 1:

$$r=a(y-x) \tag{1}$$

where x is a modulation signal and y is a rectangular signal that is supplied to the load **2** and forms a carrier signal clocking the switch-mode power circuit. In other examples, the signal p or the inverted signal p is also supplied to the at least one additional switch **100** switching a load **200**. In a further example, where the switches **1**,**100** are configured in a bridge circuit, the switch **100** may also switch the load **2**.

[0022] Conventional switch power circuits comprise modulator arrangements that use no carrier or only one carrier signal to be, for example, frequency modulated or pulse width modulated (PWM). These conventional switch power circuits create high frequency (HF) bands at multiples of the carrier frequency and their sidebands. Whereas, the disclosed arrangements use at least two carriers with different frequencies resulting in multiple HF bands, which in some examples may overlap. Such modulator arrangements are referred to as multi-carrier modulators (MCM) in the following description. The carriers are fed into different modulators and combined with a reference signal r. To drive a power switch, for example a transistor, the outputs of the several modulators are combined into a resulting bit stream. Examples of combina-

tions of two or more modulators and their attributes are described below, whereby comparators serve as modulators. In examples having more than two modulators, the AND or OR gates may have more than two inputs.

[0023] A simple decision rule may be an OR operation or an AND operation of the comparator outputs. In one example, the rules that determine whether the output of the modulator arrangement is low or high in the time domain are illustrated in equation 2 as follows:

p=1 if r<car1 or r<car2

p=0 else

p=1 if r<car1 & r<car2

p=0 else

[0024] where p is the bit-stream output, r is the reference signal and car**1** and car**2** are the two carrier signals. However, the arrangement is not limited to two carriers. In other examples, the directions of the inequality can be changed, resulting in a phase shift of 180°.

[0025] FIG. **2** is a diagram illustrating a comparison between a single carrier modulated signal and a multi carrier modulated signal combined with an OR. The modulation signal, for example at a frequency f of 2 Hz, maintains its full amplitude A while the carriers and its sidebands have an amplitude half of A when using multi-carrier modulation (MCM) such as an ORed (i.e., combined by an OR operation) multi carrier modulation instead of a single-carrier modulation such as, for example, a known natural sampled, double side modulated pulse width modulation (NADD). In this example, the ORed MCM has twice as many peaks as the NADD. The intermodulation between the two carriers and their side bands define an additional spectral component. In some examples, the intermodulation is beneficial because energy may be put into a band where communication systems available in the market do not operate, for example, basebands of cellular phones have cut-off frequencies below this frequency range. The utilization of this out-of-band intermodulation (OIM) band can be adjusted by the distance of the two carriers in frequency and/or the bandwidth around them.

[0026] FIG. **3** is a block diagram illustration of an example of an ORed MCM arrangement using comparators **4**, **5** as modulators and standard diodes **6**, **7** operated as wired OR gates. The comparators **4**, **5** each have two inputs and an output, where the inputs of each comparator are supplied with the reference signal r and one of the carrier signals car**1**, car**2**, respectively. The signal r may have any kind of waveform and signals car**1**, car**2** may be, for example, sinusoidal signals. The outputs are OR wired by diodes **6**, **7** such that the cathodes of the diodes **6**, **7** are connected together forming an output for the control signal p. The example in FIG. **4** differs from the example in FIG. **3** in that the diodes **6**, **7** have opposite polarities (i.e., the anodes are connected together forming an AND gate) and that the carrier signals car**1**, car**2** have a triangular waveform. Where, in the examples in FIGS. **3** and **4**, the voltage drop across the diodes **6**, **7** is disadvantageous, the signal can be retriggered with a driver **8** (e.g., a Schmitt trigger, inverter, comparator, amplifier, etc.) connected downstream of the OR gate or the AND gate established by diodes **6** and **7**. Pull-up or pull-down resistors, after the diode logic, may be applied dependent on the input attributes of the following stage.

[0027] FIG. **5** illustrates the results of a simulation using models of the particular physical components which match the calculation results illustrated in FIG. **2**. The signal was retriggered in this simulation as shown in FIGS. **3** and **4**. The ORed and the ANDed MCMs may be extended to N carriers, where N is an integer number. For each additional carrier, the peaks of the fundamentals are lowered by a=1/N, while the number of peaks increase by N.

[0028] FIG. **6** illustrates the behaviour of an example of a switch-mode power circuit when increasing the number of carriers to three. Both ANDed and ORed MCMs generate a direct current (DC) offset. The offset results from the statistical distribution of highs and lows in the two logical operations shown in the truth tables in FIG. **7**. In the present example, a XOR logic operation has a 50% occurrence resulting in no DC offset. However, the XOR has 50% redundancy in its truth table due to its symmetry, where the symmetry results in a doubling of the frequency of the modulation signal at the output. This is for some applications less desirable. Both, ANDing and ORing MCMs have an adequate amount of second order total harmonic distortion (THD2nd). These modulator topologies are adequate, due to low complexity, for power supplies with low line and load regulation demands. Amplifiers with low distortion demands and high EMI requirements may also benefit from these modulation schemes.

[0029] FIGS. **8**A to **8**F illustrate examples of waveforms and spectra in a single carrier modulation. FIG. **8**A illustrates the waveforms of signals r, p and y for a sinusoidal stimulation r. FIG. **8**C illustrates the spectrum of a waveform of signals p as illustrated in FIG. **8**A on a linear frequency scale. FIG. **8**E illustrates the spectrum of a waveform of signals p as illustrated in FIG. **8**A on a logarithmic scale. FIG. **8**B illustrates the waveforms of signals r, p and y for two superimposed sinusoidal stimulations of r. FIG. **8**D illustrates the spectrum of a waveform p as illustrated in FIG. **8**B on a linear frequency scale. FIG. **8**F illustrates the spectrum of a waveform of signals p as illustrated in FIG. **8**B on a logarithmic scale. In some examples, it may be desirable that no spectral component occur other than the reference signal r supplied to the modulator in the audio band, for example between 20 Hz and 20 kHz.

[0030] FIGS. **9** and **10** illustrate waveforms and spectra for ANDed and ORed multi carrier modulations, respectively. In the spectrum of the signal p that controls a transistor **19**, the frequency of the reference signal r has the same amplitude as in a single carrier system. However, the amplitude of higher frequency components is reduced by half.

[0031] Another approach to cancel the undesired DC effects of ORing and ANDing, as described above, is to switch after each resulting pulse between the ORed PWM result and the ANDed PWM result. An example of a circuit arrangement implementing the aforementioned technique is illustrated in FIG. **11**. An MCM arrangement comprises comparators **10**, **11** as modulators and standard AND gates **12**, **13**, **14** and OR gates **15**, **16**. The comparators **10**, **11** each include two inputs and an output where the inputs of each comparator are supplied with the reference signal r and one of the carrier signals car**1**, car**2**, respectively. The outputs are fed into an OR gate and into an AND gate by gates **12** and **15**.

[0032] The example in FIG. **11** further comprises a sampling element **9**, having a clock input >, a data input D, an output Q**1** and an inverted output Q**2**. The data input D of the sample element **9** is supplied with a signal from the inverted

output Q2 of the sample element **9**. The inputs of AND gate **13** are connected to the outputs of the sampling element **9** and the AND gate **12**. The inputs of AND gate **14** are connected to the outputs of the sample element **9** and the OR gate **15**. The inputs of OR gate **16** that provides the load signal y are connected to the outputs of the AND gates **13** and **14**.

[0033] The sampling element **9**, for example, a D-type flip-flop, alternately allows only one of the ORed PWM and the ANDed PWM to pass. For further lowering of high frequency peaks according to equation 2, ORing and ANDing PWMs can have multiple inputs coming from multiple comparators, where each input has its own carrier. In some examples, applying an OR-ANDed MCM causes the DC as well as the second order harmonic distortion THD2nd to vanish. However the OR-ANDed MCM may increase the third order harmonic distortion THD3rd. Additionally, the gain of such arrangement is higher than 1.

[0034] FIG. **12** illustrates examples of waveforms and spectra of the two-carrier modulation arrangement in FIG. **11**. The high frequency peaks are suppressed and the intermodulation frequency is reduced to zero. The side bands have a distance from the carrier that is equal to the frequency of the reference signal r. OR-ANDed MCM can be used for switch-mode power supplies as well as amplifiers or any other kind of PWM driven application because there is no DC component in the spectrum. The intermodulations in the audio band (e.g., 20 Hz-20 kHz) resulting from, for example, two sinusoidal carrier signals are reduced so that this type of switch-power circuit can also be used in frequency converter applications, for example, to convert a 400 Hz aircraft power supply to a 50 Hz or 60 Hz in audio applications.

[0035] FIG. **13** illustrates an example of a Master-Slave (MS) MCM that includes a master carrier and one or more slave carriers where the slope of the master carrier determines whether the ORed MCM or the ANDed MCM is passed into the single bit stream forming the signal p. The arrangement in FIG. **13** differs from the arrangement illustrated in FIG. **11** in that the sample element is substituted by a differentiating element **17** that is supplied with carrier car**1** (master carrier) and provides a differentiated signal to AND gate **13** and an inverted (by means of an inverter **18**), differentiated signal to AND gate **14**, via the inverter **18**. In other examples, instead of differentiating the carrier signal car**1**, a differentiated carrier signal may be used that is supplied to the comparator **10** via an integrator. This arrangement allows for a very high linearity while still lowering the complete out-of-band spectrum as illustrated in FIG. **14**. This arrangement is capable of driving any kind of PWM system, including high-class switch-mode, for example audio, power amplifiers and power supplies.

[0036] The multi-carrier modulation lowers the amplitude of the whole spectrum of a switch-mode modulator while keeping the in-band performance, uses more frequencies and is relatively easy to implement and therefore it saves cost, space, and complexity in switch-mode power circuits.

[0037] Although various exemplary embodiments of the invention have been disclosed, it will be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the spirit and scope of the invention. It will be obvious to those reasonably skilled in the art that other components performing the same functions may be suitably substituted. Instead of comparators, for example, multipliers or differential amplifiers may be used as modulators. Further, the methods of the invention may be achieved in either all software implementations, using the appropriate processor instructions, or in hybrid implementations that utilize a combination of hardware logic and software logic to achieve the same results. Such modifications to the inventive concept are intended to be covered by the appended claims.

What is claimed is:

1. A circuit comprising:

a controllable element that controls a load current in response to a control signal supplied to the controllable element; and

a control unit connected to the controllable element and providing the control signal, the control unit comprising

a first signal processing unit having an output and supplied with a first carrier signal and an input signal;

a second signal processing unit having an output and supplied with a second carrier signal and the input signal; and

a combiner unit connected to the first and second signal processing units combining the outputs of the first and the second signal processing units to form a signal representative of the control signal.

2. The circuit of claim **1**, where the controllable element comprises a controllable switch configured to switch the load current on and off dependant on the control signal and where the combiner unit comprises a logic unit that combines the outputs of the first and the second signal processing units to form a binary signal representative of the control signal.

3. The circuit of claim **2**, where the logic unit provides at least one of an OR operation, an AND operation and an OR-AND operation.

4. The circuit of claim **3**, where

the logic unit further comprises a first AND gate, a first OR gate and a second OR gate, each gate having at least two inputs and an output;

the inputs of the first AND gate and the first OR gate are each coupled with the outputs of the first and the second signal processing units; and

the outputs of the first AND gate and the first OR gate are coupled with the inputs of the second OR gate, the second OR gate having an output providing the control signal.

5. The circuit of claim **4**, where

one of the first and the second carrier signals is a master carrier signal having a slope; and

the output of at least one of the first AND gate and the first OR gate provides the control signal that is a function of the slope of the master carrier signal.

6. The circuit of claim **4**, where

the logic unit further comprises a second AND gate and a third AND gate, each gate having two or more inputs and an output;

the second AND gate is supplied with a differentiated master carrier element and the output of the first AND gate;

the third AND gate is supplied with an inverted differentiated element and the output of the first OR gate; and

the second OR gate is connected to the outputs of the second and the third AND gates, the second OR gate providing the control signal.

7. The circuit of claim **6**, where the control signal further comprises alternating pulses from the first OR gate and the first AND gate.

8. The circuit of claim **7**, where

the logic unit further comprises a second AND gate, a third AND gate, and a sample element, each gate and the sample element having one or more inputs and an output;

one input of the sample element is supplied with an inverted output signal of the sample element;

the second AND gate is connected to the outputs of the sample element and the first AND gate;

the third AND gate is connected to an inverted output of the sample element and the output of the first OR gate; and

the second OR gate is connected to the outputs of the second and the third AND gates and provides the control signal.

9. The circuit of claim **2**, where each of the first and the second signal processing units further comprise comparators, each comparator having inputs and an output, the inputs supplied with the input signal and one of the carrier signals.

10. The circuit of claim **2**, where the first and the second signal processing units are adapted to generate pulse width modulated signals.

11. The circuit of claim **1**, where the first and the second carrier signals have at least one of a rectangular, a sinusoidal, and a triangular waveform.

12. The circuit of claim **11**, where the first and the second carrier signals are clock signals having a rectangular waveform.

13. The circuit of claim **1**, where the first carrier signal frequency is different than the second carrier signal frequency.

14. The circuit of claim **1**, where the controllable element comprises a transistor.

15. The circuit of claim **1**, where the signal processing unit comprises a modulator.

* * * * *

B.12 Internal Report: Curent Driven Power Stages

Internal Report: Current Driven Power Stages, Technical University of Denmark, DTU 92501-10, 2010, linked to chapter 6

Internal Report: Curent Driven Power Stages

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***Abstract*—This documentation describes two current driven power stages to convert power from one or more current sources into a regulated load current or voltage. One special application is to amplify an audio signal to drive a loudspeaker, where the power is taken from one or more current sources. The function of the topologies is described. The component stresses are derived and an efficiency estimation is given. The concept is proofed by waveforms through experimental result.**

I. Introduction

Traditional power stages of converters are driven by voltage sources (VDP) as shown in section II. All of those topologies (like buck, boost, flyback, push-pull, half bridge, full bridge, SEPIC at al.) carefully avoid shorting their energy source. On the output side, they conventionally provide a voltage to a load. In very special cases it is less desired to have a controlled output voltage rather than a controlled output current. One of those are audio power amplifiers. Their loads are transducers which use the current to create a force moving air masses and therefore generate sound pressure. The transfer function from the electrical into mechanical parameters is given by equation I.1.

Equation I.1 Force of a transducer

$$F = Bl \cdot I$$

In this equation Bl is given by the transducers parameters as magnetic field B and displacement l to generate the force F by means of electrical current I through the voice coil.
To best serve this characteristic of transducers it is desirable to build amplifiers which are supplying a controlled current to the speaker and to further ease the current processing by the power stage of the amplifier it is desirable to supply this stage with current instead of voltage.
Section III shows examples of realizing such current driven power stages and explains there operations. Section IV elaborates on the differences between voltage and current driven power stages (VDPs and CDPs) including the requirements on the components followed by a description of possible fault handling and the ease to handle them in CDPs. It includes a quantitative comparison on the filter design criteria revealing further advantages of CDPs and finally naming the differentiators of the novel family of circuit configurations to existing state-of-the art. Section V presents experimental results from one of the explained stages. Rounding up, section VI sums the characteristics of the novel derived topologies current driven power stages (CDP) up and concludes the description with a brief summary.

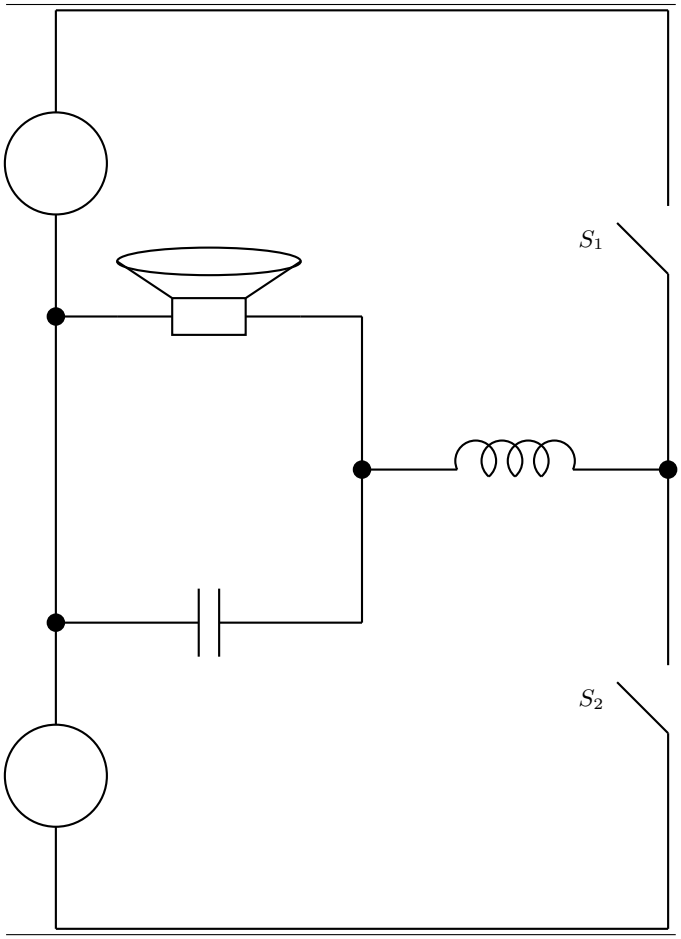
II. Voltage Driven Power Stage (VDP) Topologies

The state of the art converter topologies are operated from voltage sources. This section will give a short overview of a half bridge and a full bridge buck-type converter and boost-type converters.

A. Buck Voltage Driven Power Stages (VDP)

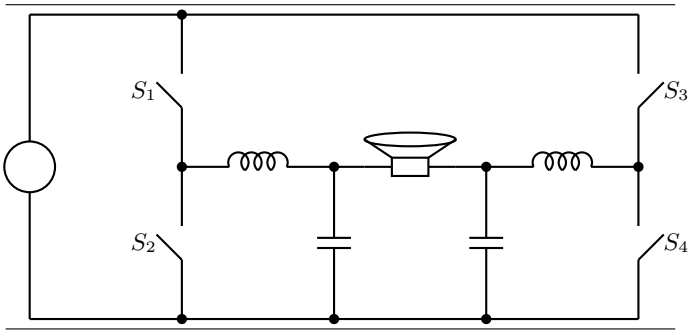
A commonly known circuit configuration for various applications - like efficient power regulators and audio power amplifiers - is shown in figure 1. It consists of two voltage sources, two switches and an output filter, comprising an inductor and a capacitor. The load is shown as a loudspeaker as one particular implementation of this circuit topology. The switches S_1 and S_2 are alternating closed in a manner that they are never both closed at the same time. This way, it is either the voltage of the upper voltage source or the lower voltage source, which is applied across the output filter and load network. By controlling the time intervals, for applying either one of the source voltages through the switches to the filter and load, the desired averaged output signal can be adjusted.

Fig. 1 Principal schematic of a voltage driven power stage (VDP) in half bridge buck configuration.



An extension is shown in figure 2. It saves one voltage source and applies the only remaining voltage source alternatively to the left and right side of the load utilizing two of the above named output filters. Through this operation, the differential voltage across the load can be controlled in the same manner as stated above. The basic operation of the circuit closes switches S_1 and S_4 simultaneously to apply one polarity across the load and closes switches S_2 and S_3 accordingly to apply the other polarity across the load. An extension of the principal of operation is, to close either switches S_1 and S_3 or S_2 and S_4 simultaneously, to apply neither one of the polarities and still keep a freewheeling path for the inductors.

Fig. 2 Principal schematic of a voltage driven power stage (VDP) in full bridge buck configuration.

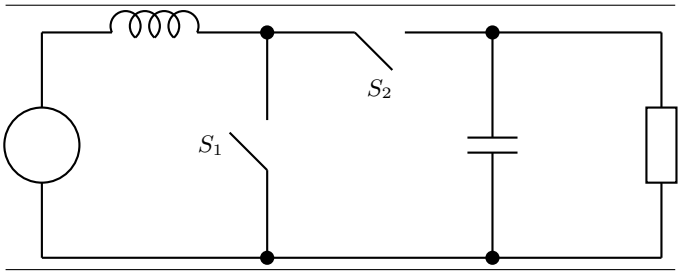


Both of those circuit configurations are capable of applying voltages up to the supply voltage across the load. The average voltage across the load is proportional to the turn-on times of the switches.

B. Boost Voltage Driven Power Stages (VDP)

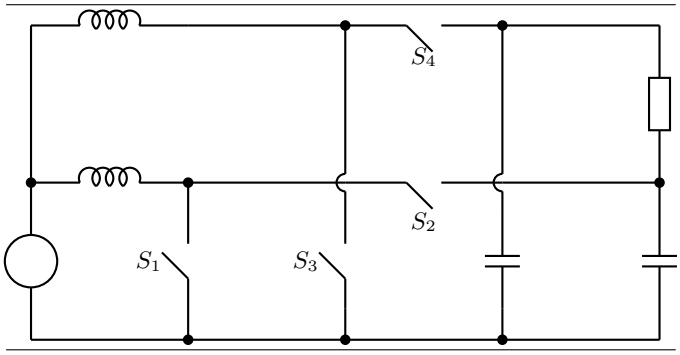
Another way of combining voltage sources, filter elements and loads is, to put the switch configuration between the energy storing components, comprised through the inductor and the capacitor as shown in figure 3. The switches are operated alternating again, where at no instance of time both of them are turned on simultaneously. As long as switch S_1 is turned on, the inductor is getting magnetized and the load is discharging the capacitor. When switch S_2 is turned on, the inductor is freewheeling (demagnetizing) and charging the capacitor. The inductor current might or might not reach zero during that operation condition. This configuration only allows for voltages across the load, which are bigger than the voltage of the only source.

Fig. 3 Principal schematic of a voltage driven power stage (VDP) in half bridge boost configuration.



The same extension as in the buck derived topologies in section II-A can be applied to boost derived topologies. The resulting circuit is shown in figure 4. The number of inductors, capacitors and switches doubles also here. The basic operation of one set of circuits is the same as in the half bridge configuration, while the voltage across the load is again the differential voltage across the resistor. This way also voltages lower than the input voltage can be achieved. Again here the two sets of switches can be operated synchronized or uncorrelated allowing for a total number of 4 different conduction paths under the premise that S_1 and S_2 as well as S_3 and S_4 are never turned on simultaneously.

Fig. 4 Principal schematic of a voltage driven power stage (VDP) in full bridge boost configuration.



The averaged output voltage of the two boost-derived circuit topologies are hyperbolically dependent on the turn-on times of the switches.
To adopt for current sources as the energy input of the converter changes can be made to the traditional converters. The following list is documenting them:

- [1] is showing the operation of a voltage driven power stage as a current source representation.
- [2] is demonstrating how to rework a voltage driven isolated power stage to be used for current sources.
- [3] turns the current source into voltage sources by adding a capacitor at the input. By these means a voltage driven power stage can be used after the capacitor.

No topology was found by the authors, which can directly convert energy from a current source. This challenge will be solved in section III.

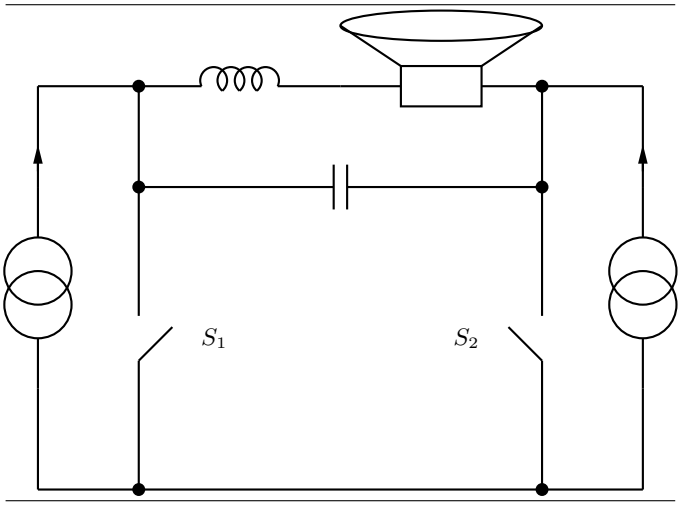
III. Current Driven Power Stage (CDP) Topologies

Basically two different topologies of voltage driven buck converters have been used so far in the art for driving a transducer: half bridges and full bridges. Both of those topologies can be converted into current driven power stages (CDP). The first part of this section accomplishes the schematics and functions of those two converter types as well as there basic functionality. The second section explores the same interest for a rarely in audio amplifiers used boost converters. This forms a new set of circuit topologies enabling the use of current sources to be directly applied to a given load under regulated conditions.

A. Buck derived Current Driven Power Stages (CDP)

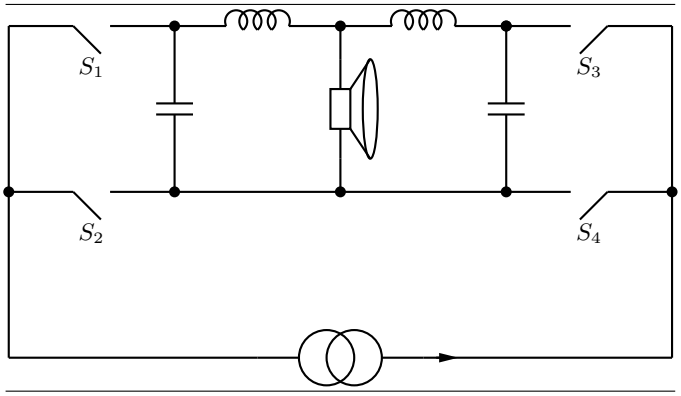
Figure 5 shows the half bridge current driven power stage. It comprises a set of switches applying the current of two current sources to the output filter and the load. The output filter is formed by an inductor and a capacitor. The load is shown as a loudspeaker again, as one of its possible applications is an audio amplifier without loose of generality. When either one of the switches is open, the current from the source, parallel to this switch, is flowing through the output filter and the load. By turning the other switch off, the opposite polarity of current can be applied to the same circuit. Both switches must not be turned off simultaneously.

Fig. 5 Principal schematic of a current driven power stage (CDP) in half bridge buck configuration.



Another implementation allowing for both signal polarities through the load is, using twice as many output filter elements, twice as many switches but only one current source. This corresponds to a current driven power stage (CDP) in full bridge configuration as shown in figure 6. The conduction path for the first polarity of load current is through the closed switches S_1 and S_4. Accordingly the other polarity is applied through closing switches S_2 and S_3. All four switches may be closed simultaneously, however opening all of them at the same time is not desired. Additionally the power stage can be operated in a manner, that no signal is delivered to the load by either closing S_1 and S_3 or S_2 and S_4 simultaneously.

Fig. 6 Principal schematic of a current driven power stage (CDP) in full bridge buck configuration.

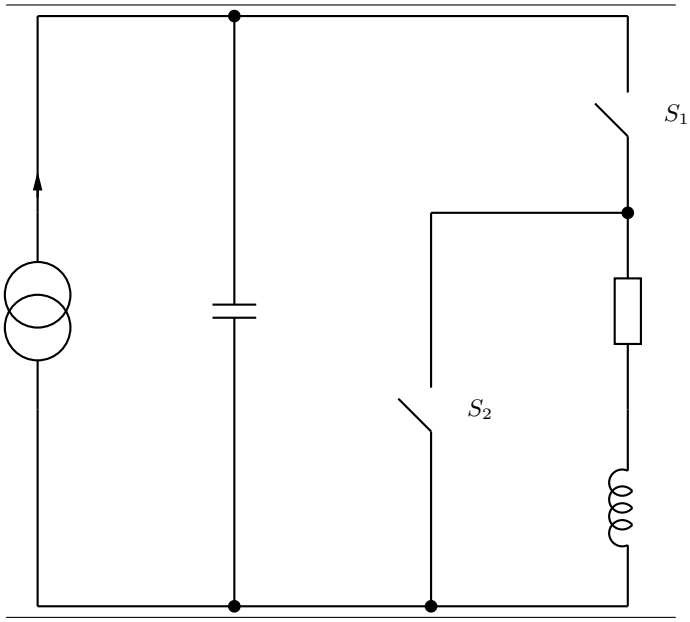


Both of those configurations allow load currents up the current provided by the sources. When controlled in an on off manner, the average current through the load is proportional to the off-times of the switches.

B. Boost derived Current Driven Power Stages (CDP)

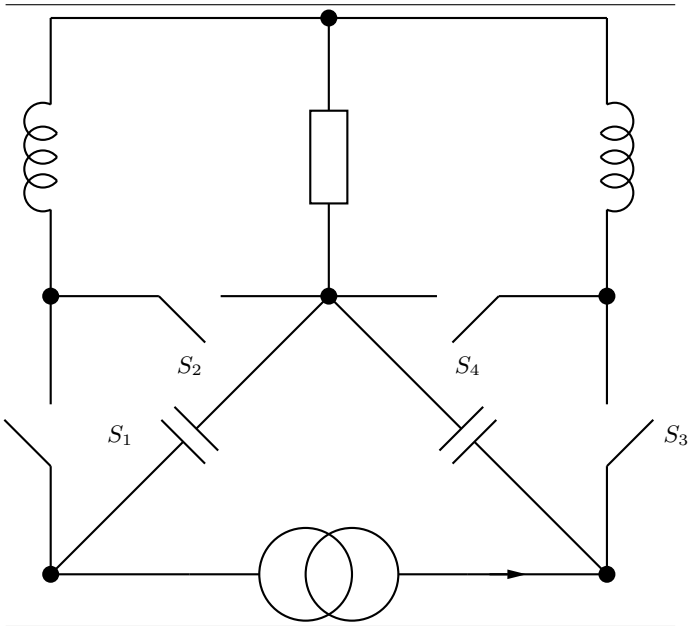
Splitting the output filter components, utilizing their energy storage ability and controlling them by switches placed in between of them allows the realization of boost-derived current driven power stages (CDP). The half bridge version is shown in figure 7. Opening switch S_1 charges the capacitor from the current source. During this time switch S_2 must be closed to provide a freewheeling path for the inductor. Closing switch S_1 provides now both, the current from the current source as well as the charges form the capacitor to the series configuration of load and inductor as soon as switch S_2 is opened. Through this operation the current flowing through the load is equal or higher than the current of the source. Both switches must not be turned off simultaneously.

Fig. 7 Principal schematic of a current driven power stage (CDP) in half bridge boost configuration.



As the load current can only be equal or greater than the source current in the half bridge configuration, a circuit is desirable, which can provide also lower currents than the source current through the load. The full bridge current driven power stage (CDP), providing this ability, is shown in figure 8. It consists of twice as many filter components and switches as the half bridge. The two switch pairs S_1 and S_2 as well as S_3 and S_4 must not be opened simultaneously. Both of those pairs can however be operated independent or correlated. Opening S_1 (or S_3 respectively) allows charging the capacitor connected to the respective switch from the current source. During this time the according inductor load path can freewheel through S_2 (or S_4 respectively). Closing S_1 (or S_3) and opening S_2 (or S_4) allows both, the current from the source as well as the stored charges in the capacitor to flow through the load. As the stored energy in the capacitors are of opposite polarity the output current polarity can be controlled in either direction.

Fig. 8 Principal schematic of a current driven power stage (CDP) in full bridge boost configuration.



The average current through the load is hyperbolically dependent on the turn-off times of the switches.

IV. Perspective

The different approaches to provide energy to a given - either through voltage driven power stages (VDPs) or current driven power stages (CDPs) gives different criteria for the design of the circuit. This section will put them into perspective with respect to component requirements and protection circuitries. For some applications one or the other is preferable for implementation. The qualitative advantages for the current driven power stages (CDPs) will be shown and their novelty factor will be given. The characteristics in this section focus on the comparison of the respective buck-derived half bridge configurations without loose of generality.

A. Component Requirements

The voltage driven power stage (VDP) in half bridge buck-derived configuration requires switches, which can withstand the voltage of both voltage sources simultaneously, as it is applied to either one of them, when the other one is turned on. Either one of the switches has to carry the desired maximum load current.
In the current driven power stage (CDP) in half bridge buck-derived configuration, either of the switches has to carry the sum of the current sources current as both of them will flow simultaneously through one switch if the other one is turned off. The voltage stress on either of the switches is equal to the maximum desired voltage across the load.
New advances in semiconductor technology, for example silicon-carbide, fit well with the current driven power stage. Another perspective in semiconductors is the fact that small-signal stages in integrated analogue electronics are preferably controlled by current sources. The here described circuits allow the same principles to be used in large-signal integrated circuits as well.

B. Current Sources

A current source can either be a natural source, like a solar panel, or any type of power supply regulating its output current instead of its output voltage. In many supply topologies, this can remove bulky output capacitors and shrink the size of the supply.

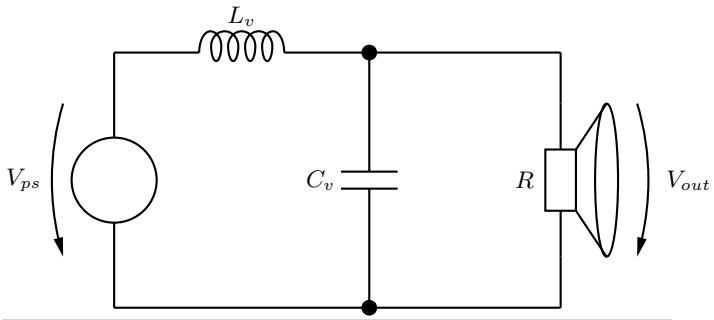
C. Protection

The protection circuitry is a major difference between the type of power stage in use: while voltage driven power stages (VDPs) require bidirectional current sensing in the power path, the current driven power stages (CDPs) need to measure a voltage. While the first approach required power components, the second one can deal with common and cheap small-signal circuitry. A fast reacting and cheap comparator can be used to sense the voltage level across each switch and differentially across the output filter and take action to prevent destruction in case of overload.

D. Quantitative Improvement

Another significant difference between the voltage and current driven half bridge power stage is the physical size of its output filter components. Comparing capacitors and inductors, it turns out, that a 1 µH inductor is always bigger than a 1 µF capacitor. As the filter for most applications needs to be a low pass and the quality of the filter is comprised by stability requirements on the converter in case of a regulated output, the choice of inductor L and capacitor C value is set for a given load resistance R.
This section is deriving the values for the output filter components for a given quality factor and resonance frequency in both, voltage driven and current driven power stage configurations. The two filter configurations are given in figure 9 and 10 respectively.

Fig. 9 Output filter for half bridge voltage driven power stage (VDP).



The corresponding transfer function for the voltage driven power stages (VDPs) output filter from figure 9 is given in equation IV.1.

Equation IV.1 Transfer function of the voltage driven power stages (VDPs) output filter

$$\underline{H}_v(\underline{s}) = \frac{V_{out}}{V_{ps}} = \frac{1}{1 + \underline{s}\frac{L_v}{R} + \underline{s}^2 L_v C_v}$$

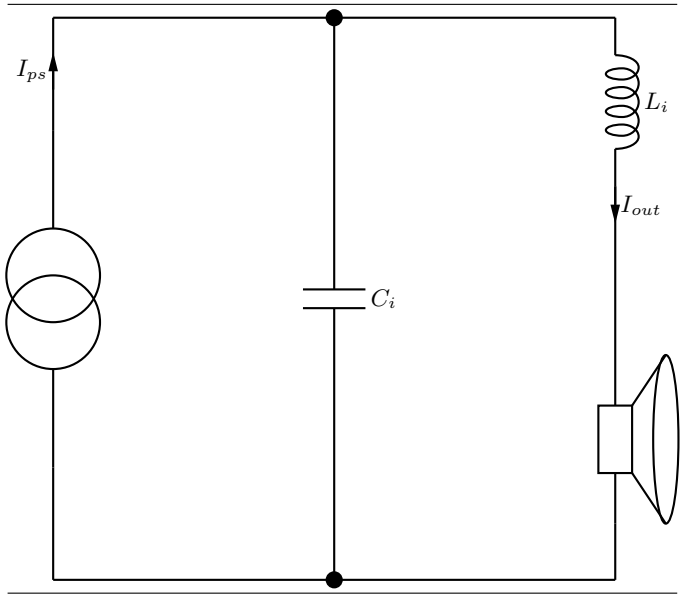
This leads to the damping d_v and time constant T_v as in equation IV.2.

Equation IV.2 Damping factor d_v and time constant T_v for voltage driven power stage (VDP) output filters

$$\begin{aligned} d_v &= \frac{1}{2R}\sqrt{\frac{L_v}{C_v}} \\ T_v &= \sqrt{L_v C_v} \end{aligned}$$

The respective transfer function for the current driven power stages (CDPs) output filter as shown in figure 10 is given in equation IV.3.

Fig. 10 Output filter for half bridge current driven power stage (CDP).



Equation IV.3 Transfer function of the current driven power stages (CDPs) output filter

$$\underline{H}_i(\underline{s}) = \frac{I_{out}}{I_{ps}} = \frac{1}{1 + \underline{s}RC_i + \underline{s}^2 L_i C_i}$$

This corresponding damping factor d_i and time constant T_i as presented in equation IV.4.

Equation IV.4 Damping factor d_i and time constant T_i for current driven power stage (VDP) output filters

$$\begin{aligned} d_i &= \tfrac{R}{2}\sqrt{\tfrac{C_i}{L_i}} \\ T_i &= \sqrt{L_i C_i} \end{aligned}$$

To make a fair comparison between both output filter configurations, the load R is set equally. Additionally the equations IV.5 set the same damping and time constant parameters for both configurations.

Equation IV.5 Setting the defining filter parameters equal.

$$\begin{aligned} d_v &\equiv d \equiv d_i \\ T_v &\equiv T \equiv T_i \end{aligned}$$

This in turn leads to design criteria for the values of the current driven power stages (CDPs) filter component values based on the equivalent filter for voltage driven power stage configuration (VDP) as given in equation IV.6.

Equation IV.6 Equivalent filter components in current driven power stage (CDP) mode.

$$\begin{aligned} L_i &= R^2 C_v \\ C_i &= \tfrac{L_v}{R^2} \end{aligned}$$

Taking a very typical configuration of an audio power amplifier into account, the components can be compared numerically as shown in table I

TABLE I Exemplary component values for a typical Class-D audio amplifier

component	VDP	CDP
resistor	4Ω	4Ω
inductor	20 µH	7.5 µH
capacitor	470 nH	1.25 µF

This comparison shows that the inductor shrinks in value and size, while the capacitors value increases. When taking into account that the inductors are in general bigger in size and weight than capacitors, this is very advantageous for compact and light weight designs, which is a common desire in electronics. Table II shows an exemplary size comparison from commercially available components for a 100 W amplifier (delivering 10 A peak current at 40 peak output voltage, which is giving the component stress).

TABLE II Exemplary filter size comparison

component	VDP	CDP
inductor	8134 mm^3	851 mm^3
capacitor	190 mm^3	475 mm^3
total	8324 mm^3	1326 mm^3

This yields an improvement in size by 84 %.
Comparing the voltage driven and the current driven half bridge converters with respect to the energy storage in the output filter components, the following equations apply:

Equation IV.7 The energy storage E in the output filter of both, voltage and current driven half bridge power stage. V and I is the output signal, which is supposed to be equal in both topologies for fair comparison. The ripple voltage across the capacitor and the ripple current through the inductor are neglected.

$$\begin{aligned} E_v &= E_{v_L} + E_{v_C} = \\ &\quad \tfrac{1}{2}L_v I^2 + \tfrac{1}{2}C_v V^2 \\ E_i &= E_{i_L} + E_{i_C} = \\ &\quad \tfrac{1}{2}L_i I^2 + \tfrac{1}{2}C_i V^2 \end{aligned}$$

Setting equations IV.6 into IV.7 and using ohms law across the load proofs the total amount of energy storage in current driven configuration E_i to be equal to the voltage driven configuration E_v:

Equation IV.8 Equal amount of energy is stored in the voltage driven and the current driven power stage.

$$E_i = \tfrac{1}{2}C_v V^2 + \tfrac{1}{2}L_v I^2 \equiv E_v$$

E. Novelty

The direct conversion from energy provided by a current source by means of specific switch and filter configurations is believed to be new. An especial focus is set on the fact that this conversion can be done in one stage only and the energy at the output can easily be

regulated. On top of that it is simple to provide protection features to this kind of circuit configurations and additionally it helps toward striving for low size and light weight electronics.
This document demonstrated, how to apply this novel principle to buck and boost power stages in half bridge and full bridge configuration. It can also be applied to further topologies, like buck-boost, super-buck and super-boost.

V. Experimental Results from a current driven Buck converter

A prototype of the current driven power stage (CDP) in half bridge buck configuration as previously described in section III-A was built. Figure 11 shows the rectangular waveform of the switched current of one of the converter legs.

Fig. 11 Single switch node of one leg of a half bridge CDP

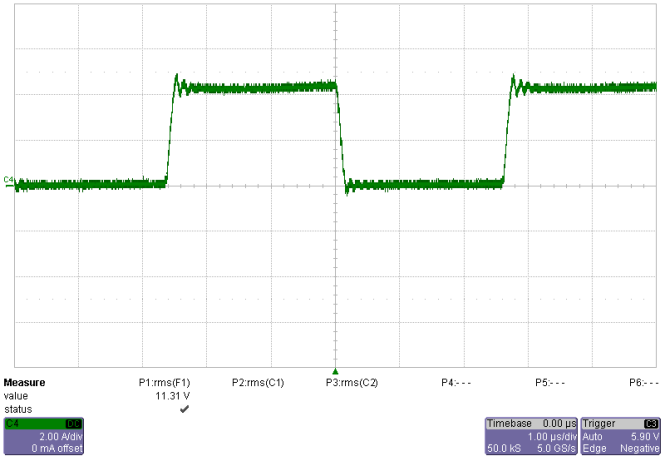
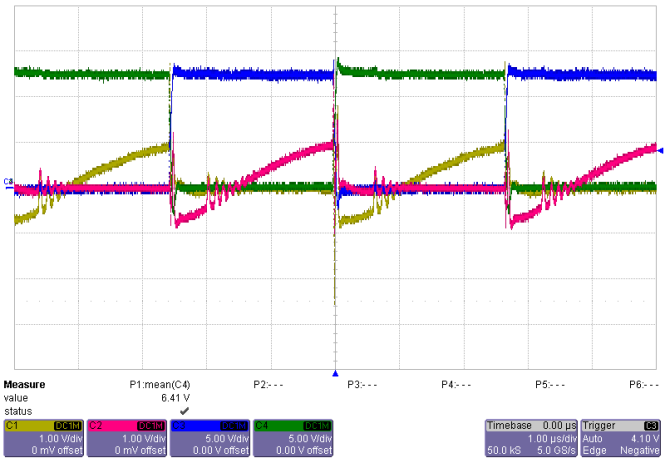


Figure 12 provides insight in both legs of the same converter (green and blue). Additionally both voltage ripple signals across the current sources are shown in red and yellow. The differential ripple voltage across the filter and load configuration is simply the difference between them.

Fig. 12 Both legs of the CDP and the resulting ripple voltage on the filter nodes



VI. Conclusion

After revisiting a number of voltage driven power stages, a new family of current driven power stages was introduced. Their operation was described and the advantages of the later ones in various applications was described. Finally the general idea - providing controlled energy directly from current sources - was verified by one of its specific implementation possibilities through experiment.

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B.13 A Self-Oscillating Control Scheme for a Boost Converter Providing a Controlled Current

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A Self-Oscillating Control Scheme for a Boost Converter Providing a Controlled Output Current

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Abstract

Most switched mode power supplies provide a regulated voltage at their output. However there are applications requiring a controlled current. Among others those are battery chargers, test equipment for converters driven by solar cells and light emitting diode (LED) drivers. This paper is describing a DC-DC power converter realizing such a current source.
The converter is based on a boost converter, supplied by a voltage source and acting as a current source. Through the boost converter the input voltage can be exceeded. The converter is providing a high control bandwidth based on a self-oscillating current loop. As additional practical features, soft start and output over voltage limitation are included and described in this paper.
The modulator, the control and the power stage are described in detail and verified by experiment.

Index Terms

Pulse width modulated power converters, Current supplies, Battery chargers, Solar energy, Current control, DC-DC power conversion, Switched mode power supplies

I. Introduction

Electrical energy sources are categorized into two major groups: voltage sources and current sources. When considering practical applications, mainly the first group is getting utilized: the AC mains are providing for example $230\ \mathrm{V}/50\ \mathrm{Hz}$ (Europe), $110\ \mathrm{V}/60\ \mathrm{Hz}$ (USA) or similar voltages in other parts of the world. Railway applications are supplied by voltages ranging from $650\ \mathrm{V}$ o $25\ \mathrm{kV}$ at frequencies $0\ \mathrm{Hz}$, $162/3\ \mathrm{Hz}$ and $50\ \mathrm{Hz}$ [1]. Automotive applications are driven by nominal voltages of either $12\ \mathrm{V}$ or $24\ \mathrm{V}$ direct current mainly. Telecommunication equipment is getting designed for $48\ \mathrm{V}$ operation and computer equipment as well as most integrated circuits are operated from DC voltages between $1.8\ \mathrm{V}$ and $12\ \mathrm{V}$. There is a tendency going to lower supply voltages for these kinds of applications to improve performance and efficiency of the devices. This tendency led in the past to high uncontrolled supply currents. However most applications stick to a controlled supply voltage and deal with the highly varying currents drawn by highly variable loads. Switched mode power supplies are therefore conventionally designed for providing a tightly regulated voltage and are enhanced by features protecting both, the supply and the load against excessive currents.

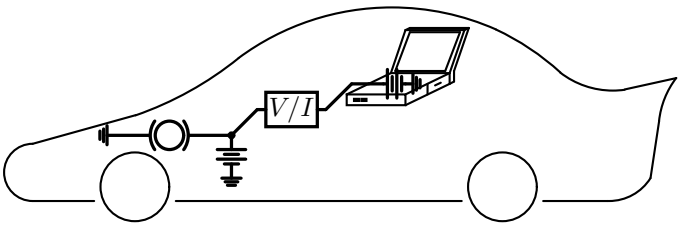


Fig. 1. Application for current boost converters: charging a laptop computer from a car battery

There are though some applications requiring a current source. Charging big capacitive components, like batteries, super capacitors and accumulators rely on a constant current. Some of those capacitive loads are getting charged by big inductive sources. An example application is a car generator and the battery in a car. The grid providing the AC mains voltage are mainly inductive as well.

If the source is not inductive, but rather capacitive it is difficult to charge another capacitive load from this source due to high currents flowing when connecting source and load. These can lead to excessive power dissipation in the equivalent series resistance in one or both of the capacitors and lead to thermal destruction. An example is the charge of a laptop computers battery or a cell phone battery. Additionally there are many times incompatibilities in voltages which require further power processing. Figure 1 shows such an application. A generator in a car is a source with high output impedance, due to the stator windings. This way it is providing a slowly varying current to charge the car battery up to 14.4 V. When this voltage is reached, the magnetic field in the generators core is reduced by a controlled stator voltage. As laptop computers are typically operated from batteries around 18 V to 20 V, the cars voltage is not enough to charge a notebook. A boost operation is therefore necessary. A voltage regulated boost converter however would not allow for controlled charging of the notebooks battery. In this paper, this is solved by regulating the output current of the converter as presented.

Another application for current sources are laboratory supplies for emulating a solar cell. The loads in this case are converters driven by the solar cells. As in the laboratory testing the full energy chain is not always available, the solar cells need to be replaced with another kind of current source. Usual laboratory supplies provide only regulated voltages. When running them in current limitation mode, this is only a very vague regulated mode, as its intention is to provide only a protection rather than a precise regulation. A current source as the presented boost current source in this paper can solve this problem as well.

Linear regulators like in [2] do not generate electromagnetic compatibility problems, however they have bad efficiency and do not have the capability of increasing the voltage. Switched mode circuits overcome the efficiency problem but not all of them are capable of increasing the input voltage to the desired battery voltage either as [3], [4] in DC-DC applications and [5], [6] in AC-DC applications. Some power converters usable as current source [7], [8], can increase the input voltage, however they require a current source on their input as well. Even using a boost technology does not guarantee to allow charging the battery to a higher voltage than the voltage source at the input of the converter as described in [9]. The maximum efficiency number in these publications for a comparable boost

converter to the one presented in this paper is $92\ \%$. Another capacitive load on a smaller power level is the gate capacitance of a MOSFET. This load has been dealt with in [10] to increase the efficiency of a boost converter.
Some boost converters require special compensation schemes for stabilizing the loop like current mode control and slope compensation as shown in [11]–[15], when regulating the boost inductors current to achieve a constant output voltage. Very fast transient responses can be achieved even at high power level, when regulating the current through an inductor as shown for a buck converter in [16]. Boost converters are therefore preferred used for power factor correction (PFC) applications [17]–[19], which require a controlled input current. In case of a boost converter this is its inductor current.
This paper will outline the specification of a boost converter, describe an unsymmetrical self-oscillating modulator, the loop transfer functions and utilize this design to meet the specifications. The output current of the boost converter is controlled tightly through a self-oscillating modulator to provide a constant current source. Experimental results and an outlook of possible further features proof the validity of theory.

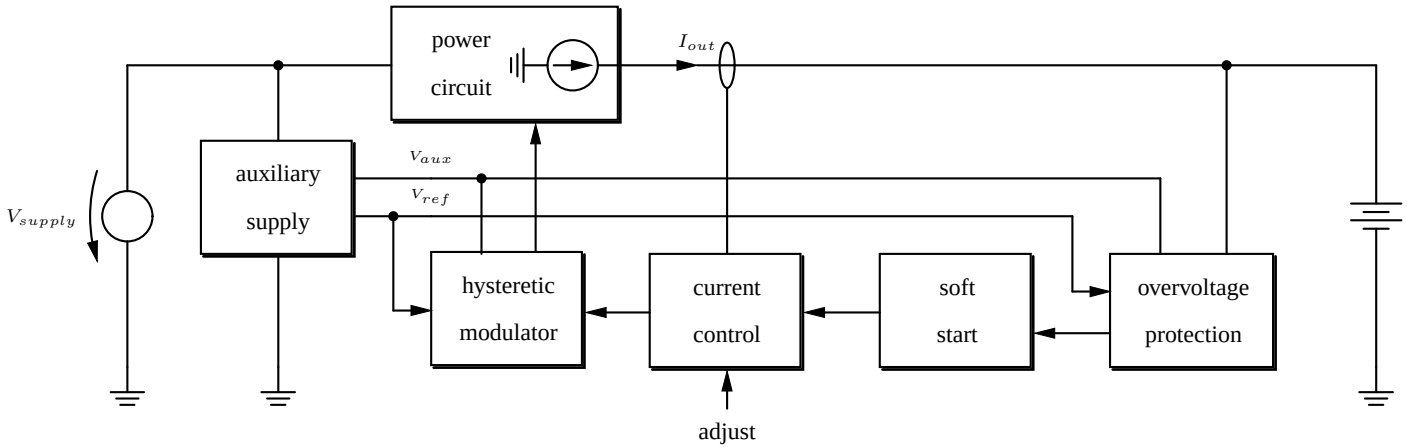


Fig. 2. Block diagram of the converter

II. Overview

A. Specification

A specific battery to be charged by the converter has a nominal voltage of 24 V. The maximum charge current is specified to 4 A. To avoid further charging, the converter shall provide an output over voltage protection. In case the battery voltage drops below the input voltage of the converter, the battery can be charged without control direct from the input of the converter which is regulated to a voltage between 9 V and 16 V. These specifications are limiting the load range of an equivalent resistive load to a range of $2.2\ \Omega$ to $6\ \Omega$.

B. Features

Figure 2 is giving an overview of the converter on a block diagram level.
The power circuit is supplied by a voltage source v_{supply} and controlled by a hysteretic modulator. The advantage

of a hysteretic modulator is, that it does not need an external clock generator. The supply voltage v_{supply} is also supplying an auxiliary supply, which is providing both, the supply voltage $V_{aux} = 5$ V as well as the reference voltage $V_{ref} = 3.3$ V for all the other blocks. The hysteretic modulator is deriving the duty cycle based on an error voltage, which is generated from the error amplifier in the current control block. This signal is derived from the PI regulator in this block after subtraction of the sensed output current of the power circuit from the external adjusted reference value. The control circuits start-up as well as its recovery after an over voltage event is provided by a soft start circuitry. The over voltage protection is clamping the soft start circuit in case of an over voltage event at the load by comparing the output voltage with the internal reference voltage of the converter.

III. Unsymmetrical self oscillating Modulator

For buck-derived switched power converters it is most desirable to provide an equal modulation range around a centered reference voltage. The switching characteristics of modulators built for those type of converters is extensively derived in [20]. Boost derived converters however have a nonlinear transfer function [21], whose gain is raising hyperbolic. For the above specified input and output voltage constellation, high duty cycles are not required. This fact can be taken into account, when choosing the reference voltage of a local self oscillating modulator as shown in figure 3.

A similar technique was applied by [22] for limiting the frequency variation of hysteretic self oscillating modulators.

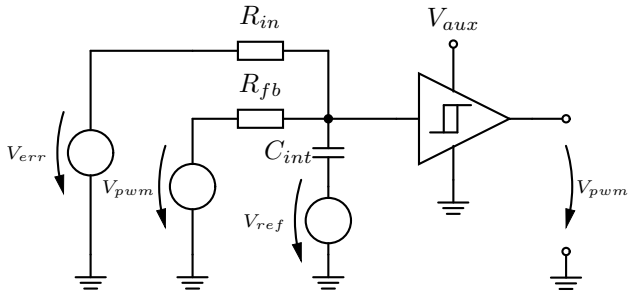


Fig. 3. Circuit diagram of a local hysteretic self oscillating modulator

Self oscillating on other variables than the local PWM-signal leads to other dependencies. This is exemplary shown for oscillation on the converters energy in [23] and on the boost inductors current in [24].

The Barkhausen oscillation criterion was profen to be not applicable for square wave oscillators such as self-oscillating modulators in [25]. As the switching frequency in self-oscillating modulators is changing [26], only an instantaneous switching frequency can be defined, i.e. for a given constant constellation of all relevant signals. Therefore the instantaneous switching parameters are derived under the assumption of DC input voltages.

For deriving the on- and off-times, the duty cycle range and the switching frequency of the modulator (switching parameters), the operation of the hysteretic modulator must be investigated. It is dependent on two signals: the hysteretic window and the carrier. The hysteretic window is generated by a voltage divider from the Pulse Width Modulation (PWM) signal v_{pwm} to the reference voltage V_{ref}. The carrier V_{car} is derived the same way, with

the difference that the signal is getting integrated by a capacitor and that the error amplifier output v_{err} is also influencing its charge.

A. Hysteretic window

First the hysteretic window is derived analytically. For the high state of the modulator v_{pwm}, it is equal to the comparators positive supply voltage V_{aux} and staying at the negative supply, which is ground, for a low output as described by 1.

$$v_{pwm}(t) = \begin{cases} V_{aux} & \forall\ v_{C_{int}}(t) < v_h(t) \\ 0 & \forall\ v_{C_{int}}(t) > v_h(t) \end{cases} \tag{1}$$

The hysteretic window V_h is following this signal instantaneously into its high state $V_{h_{high}}$ and $V_{h_{low}}$ respectively.

$$v_h(t) = \begin{cases} V_{h_{high}} & \forall\ v_{pwm}(t) = V_{aux} \\ V_{h_{low}} & \forall\ v_{pwm}(t) = 0 \end{cases} \tag{2}$$

Defining the voltage divider for the hysteretic window as k_h, those two states consist of a dynamical part and a DC-offset resulting into 3.

$$\begin{aligned} V_{h_{high}} &= \underbrace{k_h \cdot (V_{aux} - V_{ref})}_{\text{dynamic response}} + \underbrace{V_{ref}}_{\text{offset}} \\ V_{h_{low}} &= \underbrace{-k_h \cdot V_{ref}}_{\text{dynamic response}} + \underbrace{V_{ref}}_{\text{offset}} \end{aligned} \tag{3}$$

B. Carrier derivation

The carrier v_{car} is following the same stimulations, however with an individual delayed response from each of the sources and its starting condition. The starting condition is one of the static states of the hysteretic window. In case the time delay of the comparator is relevant for the expected timing of the modulator, the starting condition is going beyond those limits as described in [27]. This is not relevant for fast comparators as used in this case. The equivalent charging circuit consists of the passive part in figure 3 and includes the capacitor C_{int}, resistors R_{in}, R_{fb} as well as the voltages v_{err}, v_{pwm} and V_{ref}.

Ohms law and the node current equation at the common node of the three passive elements is leading to the differential equation of the capacitor voltage 4:

$$\begin{aligned} &v_{C_{int}}(t) + \tfrac{1}{C_{int}} \left(\tfrac{1}{R_{in}} + \tfrac{1}{R_{fb}} \right) \int v_{C_{int}}(t) \partial t = \\ &\tfrac{1}{C_{int}} \int \left(\tfrac{v_{err}}{R_{in}} + \tfrac{v_{pwm}}{R_{fb}} - \left(\tfrac{1}{R_{in}} + \tfrac{1}{R_{fb}} \right) \cdot V_{ref} \right) \partial t \end{aligned} \tag{4}$$

There are some expressions in this equation, which can be combined for deriving the switching parameters: $R_p \equiv R_{in} \parallel R_{fb}$, $\tau_p \equiv R_p \cdot C_{int}$, $\tau_{in} \equiv R_{in} \cdot C_{int}$, $\tau_{fb} \equiv R_{fb} \cdot C_{int}$. This way the differential equation 4 can be written as 5:

$$\frac{\partial\, v_{C_{int}}(t)}{\partial t} + \frac{v_{C_{int}}(t)}{\tau_p} = \frac{v_{err}}{\tau_{in}} + \frac{v_{pwm}}{\tau_{fb}} - \frac{V_{ref}}{\tau_p} \tag{5}$$

1) Dynamical Response: The dynamical part of a step response from a first order integrating system is well known to be an exponential function and the principle of superposition allows to combine the response from each of the three sources. The general solution of equation 5 must so be fulfilled by equation 6 and the remaining task is to find the parameters, which fit the actual application.

$$v_{C_{int}}(t) = A \cdot \left(1 - \mathrm{e}^{-\frac{t}{\alpha}}\right) \tag{6}$$

Inserting the general solution 6 into the differential equation 5 and comparing the general parameters A and α with the above defined problem specific parameters results into the solution for the dynamical response in 7.

$$\begin{aligned} A &= k_{in} \cdot v_{err} + k_{fb} \cdot v_{pwm} - V_{ref} \\ \alpha &= \tau_p \end{aligned} \tag{7}$$

The gain coefficients are hereby defined to $k_{in} \equiv \frac{\tau_p}{\tau_{in}}$ and $k_{fb} \equiv \frac{\tau_p}{\tau_{fb}}$.

2) Response of starting condition: Neglecting the time delay of the comparator, the step response of the system is starting at the instance in time, when the modulator acted, i.e. when a decision happened. This is always the case, when its inputs are crossing each other. As one of the inputs is the hysteretic window and the other one is the carrier signal, the decision point happens, when the carrier is reaching the hysteretic window and this constellation is also the starting point of the next transition and therefore step response. Assuming the last decision happened at a time t_d before the step responses initialization, the starting voltage v_{start} is defined as 8.

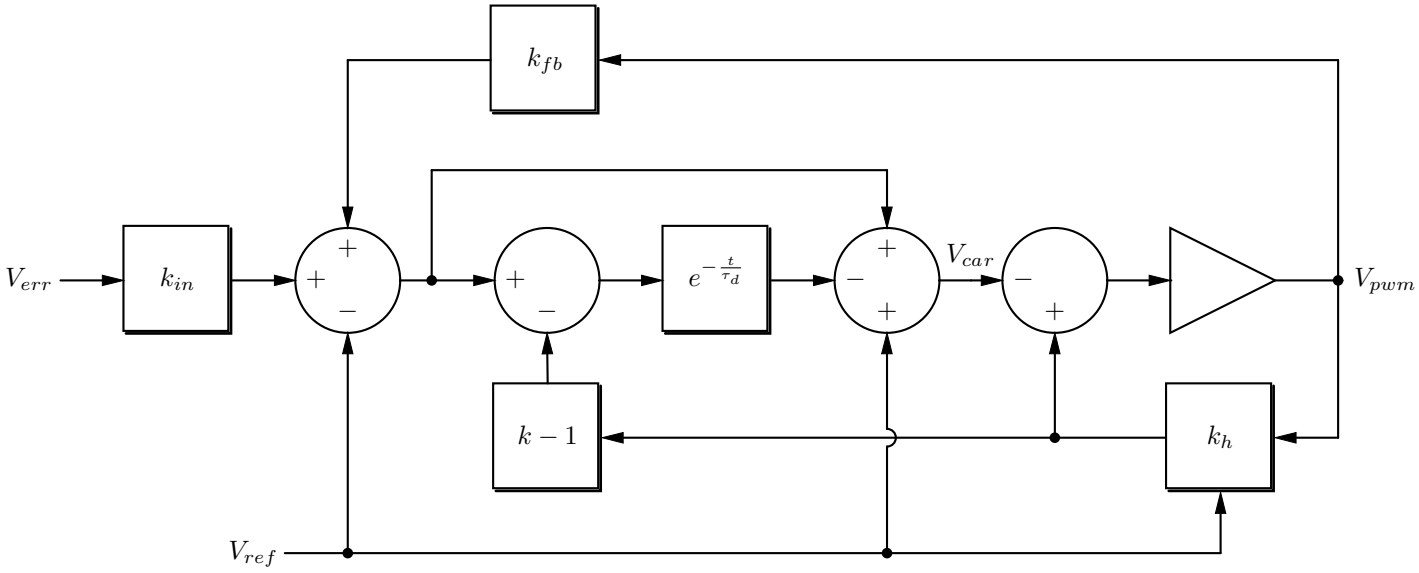


Fig. 4. Flow diagram for the derivation of the carrier and the resulting PWM signal in time domain.

$$v_{start} = V_h(t - t_d) = \begin{cases} V_{h_{low}} & \forall\ v_{pwm}(t) = V_{aux} \\ V_{h_{high}} & \forall\ v_{pwm}(t) = 0 \end{cases} \tag{8}$$

The initial voltage of the capacitor is discharging over time when all other influences are not taken into account. This fact is followed analytically by 9.

$$v_{C_{int}}(t) = B \cdot \mathrm{e}^{\frac{t}{\tau_p}} = \mathrm{e}^{\frac{t}{\tau_p}} \cdot (v_{start} - V_{ref}) \tag{9}$$

3) DC-Offset: The final superimposed part of the capacitors voltage as the carrier voltage for the modulator is the DC-offset provided by the static voltage source V_{ref}.

4) Superposition: Superimposing the dynamical response, the response of the starting condition and the offset voltage, while taking all simplifying parameters into account the final solution of the carrier signal is given by 10.

$$v_{C_{int}}(t) = \underbrace{A \cdot (1 - \mathrm{e}^{-\frac{t}{\tau_p}})}_{\substack{\text{response to} \\ \text{dynamic} \\ \text{stimulation}}} + \underbrace{B \cdot \mathrm{e}^{-\frac{t}{\tau_p}}}_{\substack{\text{response to} \\ \text{starting} \\ \text{condition}}} + \underbrace{V_{ref}}_{\text{offset}} \tag{10}$$

The parameter B is defined through equation 9. Breaking the complete equation down to the circuit parameters results into the analytical solution for the carrier signal and is visualized in figure 4.

C. Derivation of switching parameters

Knowing both, the carrier signal, a.k.a. the capacitor voltage $v_{C_{int}}$, and the hysteretic window analytically, the time duration of the PWM pulses can be derived. From this, the duty cycle d and the switching frequency f_{sw} is obvious. These parameters are called switching parameters here.

The first two switching parameters are the on time and the off time of the pulse train. Both can be derived from the crossing point of the carrier signal and the respective hysteretic window voltage, i.e. 10 needs to equal 3, leading to 11.

$$A \cdot (1 - \mathrm{e}^{-\frac{t}{\tau_p}}) + B \cdot \mathrm{e}^{-\frac{t}{\tau_p}} + V_{ref} \stackrel{!}{=} V_h \tag{11}$$

Solving this equation for the time t, the general solution for a decision point calculation – which is valid for both on and off transition – is 12.

$$t = -\tau_p \ln\left(\frac{1}{A - B}\left(A + v_{ref} - v_h\right)\right) \tag{12}$$

At this point of the timing parameter derivation the calculation needs to be split up into the two states of the PWM signal, because A, B and v_h (see equation 3) is different for the two conditions.

For the high condition the parameters A_{high} and B_{high} are valid as shown in 13.

$$\begin{aligned} A_{high} &= k_{in} \cdot v_{err} + k_{fb} \cdot V_{aux} - V_{ref} \\ B_{high} &= V_{h_{low}} - V_{ref} \end{aligned} \tag{13}$$

The second state is described by the parameters A_{low} and B_{low} for the low condition in 14.

$$\begin{aligned} A_{high} &= k_{in} \cdot v_{err} - V_{ref} \\ B_{high} &= V_{h_{high}} - V_{ref} \end{aligned} \tag{14}$$

This is resulting into the final on and off time calculation as described by 15.

$$\begin{aligned} t_{high} &= -\tau_p \ln\left(\frac{1}{A_{high}-B_{high}}\left(A_{high}+V_{ref}-v_h\right)\right) \\ t_{low} &= -\tau_p \ln\left(\frac{1}{A_{low}-B_{low}}\left(A_{low}+V_{ref}-v_h\right)\right) \end{aligned} \tag{15}$$

The other two switching parameters, switching frequency f_{sw} and duty cycle d are a trivial combination of the first two ones as given in 16.

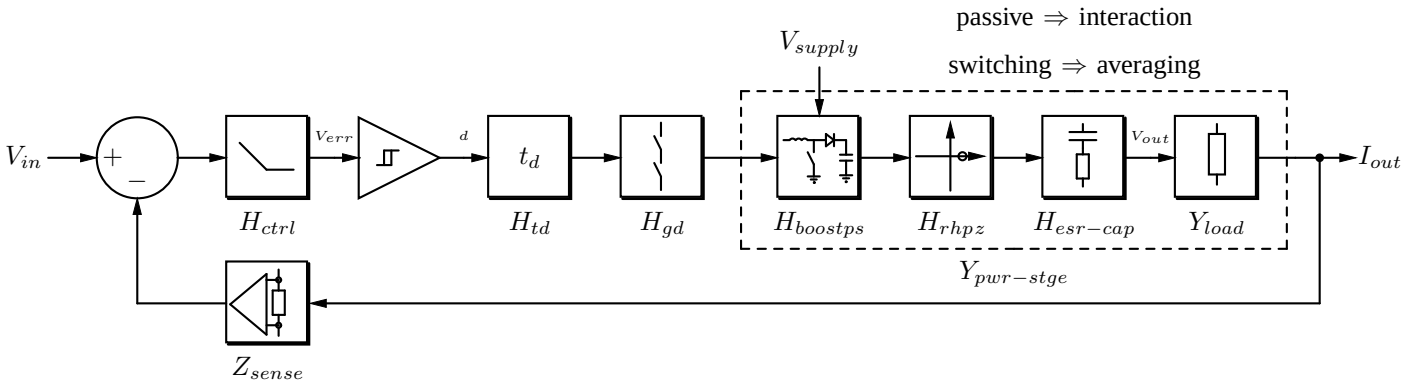


Fig. 5. Signal path diagram of the transfer function

$$\begin{aligned} f_{sw} &= \frac{1}{t_{high}+t_{low}} \\ d &= t_{high}\cdot f_{sw} \end{aligned} \tag{16}$$

These equations can be used to determine the design parameters like the reference voltage V_{ref}, which can be used to limit the duty cycle in one or the other direction – here for the boost converter setting an upper limit – and adjusting the switching frequency to the most desirable with respect to losses and electromagnetic compatibility (EMC) requirements.

In the actual case the duty cycle limitation is chosen to allow the converter to reach the required output voltage of $V_{out} = 24$ V even with the minimum input voltage of $V_{supply} \geq 9$ V. According to a simplified DC-transfer function of a boost converter the required duty cycle can be derived via 17.

$$d_{max} = 1 - \frac{V_{supply_{min}}}{V_{out}} \approx 62.5\% \tag{17}$$

The minimum duty cycle is reached when the error amplifier is leaving its linear operation region at around 1.5 V. This occurs, when the load impedance is getting so low, so that the required output voltage falls below the input voltage. In this case the switching operation stops and the boost inductor and the diode are taking all the current until either the output voltage is rising – which is the case when a capacitive load is connected – or a protection circuitry like a fuse or positive temperature coefficient (PTC) resistor is disconnecting the current flow.

IV. Control loop design

Another important consideration of boost converters is the control loop. Boost converters consist intrinsically out of tricky transfer functions, i.e. dynamically varying time constants. This section will therefore analyze each of the

parts of the actual designed boost converter and explain them before setting up the open and closed loop transfer functions. To provide a visual guide for this, figure 5 is meant to give an overview of the unique blocks and the order they are connected in the circuit.

It splits the converter into different functional blocks and distinguishes between two different types of blocks. Active blocks, which do not interact with each other and passive or partly passive blocks which influence each other. The later group is also the one, which has dynamically changing parameters. Those are derived in the following sections and plotted for different bias points – varying duty cycle d and supply voltage v_{supply} – as well as a the worst case dynamical response with both maximum duty cycle (equation 17) and maximum supply voltage $V_{supply_{max}} = 16$ V at the same time.

A. Time delay

The time delay t_d of all components in the circuit have been collected and modeled in one block. The main contributions are coming from the current sense circuit, the error amplifier, the gate drive circuit and the comparator, which adds up to around 2 µs. The transfer function of time delay is modeled according to [28] as 18.

$$\underline{H}_{t_d}(\underline{s}) = \mathrm{e}^{\underline{s} \cdot t_d} \tag{18}$$

Neither the supply voltage, nor the duty cycle has an influence on this transfer function, so it is considered static and quantitatively shown together with the other static parts of the loop in figure 6.

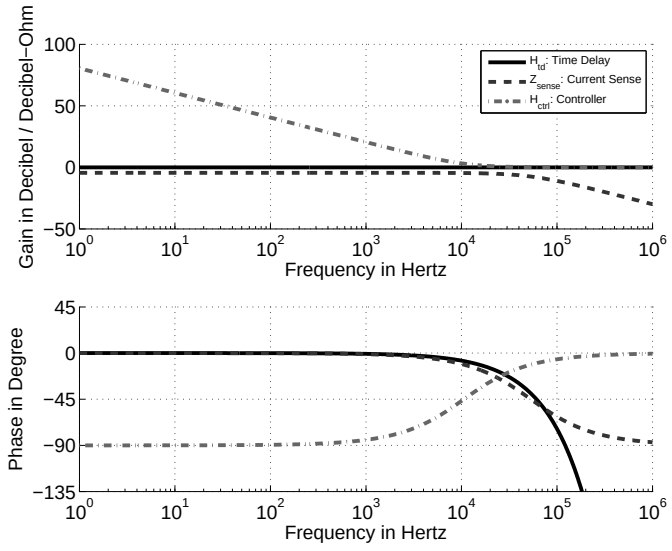


Fig. 6. Transfer functions of the static transfer functions, i.e. $\underline{H}_{td}$ to represent all time delays in the loop (consisting of current sense, error amplifier, gate driver and comparator), $\underline{Z}_{sense}$, representing active current sense including its anti-aliasing filter and $\underline{H}_{ctrl}$ as a visualization of the PI-regulator.

B. Gate Driver

The chosen gate driver is inverting. This was also taken into account when setting the reference voltage for the unsymmetrical self-oscillating modulator in the previous section. So equation 17 was actually realized for the off-time of the pulsed signal at the modulator output. The transfer function of the gate driver results into a trivial inversion as in 19.

$$\underline{H}_{gd}(\underline{s}) = -1 \tag{19}$$

C. Current Sensing

To control the current, it needs to be sensed and transfered to the voltage controlled error amplifier. Therefore a transfer impedance is required. As it is the current of the output capacitor and the contribution of the boost power stage, which is supposed to be regulated, there is no limitation in the change rate of the signal. This would be the case, if an inductor would have been added there. To avoid very fast transitions getting into the control loop through feedback, which can disturb the sampling of the signal at the comparator [29], a simple first order low pass with time constant τ_{alias} was employed to both, limit the change rate of the signal and suppress the switching artifacts. As the sensing is conducted by a small resistance R_{sense} for minimization of dissipation, the current sense circuitry is active and therefore providing gain G, which leads to the impedance in 20.

$$\underline{Z}_{sense}(\underline{s}) = G \cdot R_{sense} \frac{1}{1 + \underline{s}\tau_{alias}} \tag{20}$$

As the DC gain of the feedback network will dominate the closed loop gain of the converter, it is set so that a convenient inut voltage $V_{in} = 2.4\ \mathrm{V}$ yields to the desired output current $4.0\mathrm{A}$. The reference setting of $2.4\ \mathrm{V}$ can be derived from a either a static voltage divider from the auxiliary voltage V_{aux} or adjustable through a potentiometer from the same voltage. Figure 6 shows the DC gain therefore as $4.4\ \mathrm{dB}\Omega$.

D. Controller

The low frequency gain in the control loop is introduced after subtraction of the feedback signal from a control input voltage V_{in} by a state of the art proportional-integral (PI) controller as further described in [30]. The transfer function of the controller is given by 21 and plotted as one of the static transfer functions in figure 6.

$$\underline{H}_{ctrl}(\underline{s}) = \frac{1 + \underline{s}\tau_{PI}}{\underline{s}\tau_{in}} \tag{21}$$

E. Boost Power Stage

In [21], power converter transfer functions are split up in control-to-output and line-to-output. This is graphically represented in figure 5 with the dashed power stage box having two inputs. Control-to-output means the response of the output state space variable to the duty cycle command d and line-to-output describes the reaction of the system to the supply of the power stage v_{supply}. Several publications cope with the derivation of converters transfer functions via state space [23], [31], where for most applications the power components can be modeled ideally.

Therefore those models are also only valid up to the frequency, where the first parasitic component impacts the circuit. The following derivation of the actual boost converters power stage transfer functions was inspired by [32], [33], which are deriving those characteristics for a buck and a superbuck converter in peak current control mode including their first order parasitic components. In the actual case the output variable is the output current of the converter. So the state space equation for the switch being turned on take the form of 22 and for the switch being turned off 23 describes the behaviour of the circuit during the time, when the MOSFET is turned off. Note that the equation set can only be used for averaging to describe the low frequency reaction of the system, when the converter is operated in continuous conduction mode (CCM).

In the following derivation of the boost converters transfer functions, L is the boost inductor, C the output filter capacitor and R_C as well as R_L their equivalent series resistances. The state variables are the inductor current i_L and the capacitor voltage v_C. The converters output current i_R through the load resistor R is the output variable.

$$\begin{aligned} \frac{\partial\, i_L}{\partial t} &= \frac{v_{supply} - R_L \cdot i_L}{L} \cdot i_L \\ \frac{\partial\, v_C}{\partial t} &= -\frac{v_C}{(R+R_C)C} \\ i_R &= \frac{v_C + \frac{\partial v_C}{\partial t} R_C C}{R} \end{aligned} \tag{22}$$

$$\begin{aligned} \frac{\partial\, i_L}{\partial t} &= \frac{v_{supply} - R_L \cdot i_L - v_C - R_C C \frac{\partial\, v_C}{\partial t}}{L} \\ \frac{\partial\, v_C}{\partial t} &= \frac{R \cdot v_C - v_C + R_C C \frac{\partial\, v_C}{\partial t}}{RC} \\ i_R &= \frac{v_C + R_C C \frac{\partial v_C}{\partial t}}{R} \end{aligned} \tag{23}$$

Transferring the equations via LaPlace transformation into the frequency domain yields the linear time-variant circuit representation in 24 for both conditions, where subscript 1 denotes the switch being turned on, while subscript 2 describes the state, where the switch is turned off.

$$\begin{aligned} \underline{s} \begin{pmatrix} \underline{i}_L \\ \underline{v}_C \end{pmatrix} &= \overbrace{\begin{pmatrix} -\frac{R_L}{L} & 0 \\ 0 & \frac{-1}{(R+R_C)C} \end{pmatrix}}^{\underline{\mathbf{A}}_1} \begin{pmatrix} \underline{i}_L \\ \underline{v}_C \end{pmatrix} + \overbrace{\begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}}^{\underline{\mathbf{B}}_1} \underline{v}_{sply} \\ \underline{s} \begin{pmatrix} \underline{i}_L \\ \underline{v}_C \end{pmatrix} &= \overbrace{\begin{pmatrix} -\frac{R_L}{L} & -\frac{1+\underline{s}R_C C}{L} \\ \frac{1}{C} & -\frac{1+\underline{s}R_C C}{RC} \end{pmatrix}}^{\underline{\mathbf{A}}_2} \begin{pmatrix} \underline{i}_L \\ \underline{v}_C \end{pmatrix} + \overbrace{\begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}}^{\underline{\mathbf{B}}_2} \underline{v}_{sply} \end{aligned} \tag{24}$$

The matrix representation for description of the output current of the converter is equal in both states and shown in 25.

$$\overbrace{\underline{i}_R}^{\mathbf{y}} = \overbrace{\begin{pmatrix} 0 & \frac{1+\underline{s}R_C C}{R} \end{pmatrix}}^{\underline{\mathbf{C}}} \overbrace{\begin{pmatrix} \underline{i}_L \\ \underline{v}_C \end{pmatrix}}^{\mathbf{x}} + \overbrace{0}^{\underline{\mathbf{D}}} \quad \overbrace{\underline{v}_{sply}}^{\mathbf{u}} \tag{25}$$

The averaged state matrix $\mathbf{A}$ and input matrix $\mathbf{B}$ are derived by multiplying the according matrices with the time interval they are valid according to 26, where this time interval is simply described via duty cycle d.

$$\mathbf{A} = d \cdot \mathbf{A}_1 + (1-d) \cdot \mathbf{A}_2; \quad \mathbf{B} = d \cdot \mathbf{B}_1 + (1-d) \cdot \mathbf{B}_2 \tag{26}$$

The output matrix $\mathbf{C}$ was already declared in 25 independent on the state, the converter is in and the feedback matrix $\mathbf{D}$ is zero. Through 27 the final transfer function from supply voltage v_{supply} to output current i_R can be derived to 30.

$$\underline{Y}_{line_{pwr-stge}} = \underline{\mathbf{C}} \cdot \left(\underline{s}\mathbf{E} - \underline{\mathbf{A}}\right)^{-1} \cdot \underline{\mathbf{B}} \tag{27}$$

As the parasitics of filter and energy storage components are only punctually documented in their technical description, the equivalent series resistance of the electrolytic capacitor at the output (R_C) and the parasitic resistance of the inductor R_L was measured at room temperature across frequency. The results of the sweeps are shown in figure 7 and 8 respectively.

From equation 30 and both of the above measurements a quantitative representation of this transfer function can be plotted (figure 9).

Note that the DC-gain is lower than one as the transfer function describes an admittance $\underline{Y}$. Its interpretation is output current i_R divided by supply voltage v_{supply}, which leads correctly to -7.0 dBS, -11.1 dB and -12.0 dB for a desired output current of $i_R = 4.0\text{A}$ at the three bias points $v_{supply} = 9.0$ V, 14.4 V and 16.0 V.

The high frequency roll-off following closely a first order low-pass transfer function is a composition of a second order low-pass and a first order high-pass. The second order low-pass is mainly dominated by the two energy storage components L and C and the load resistor R as damping, while the high-pass is formed by the equivalent series resistance of the capacitor R_C and the capacitor C itself.

Despite its supply voltage the other input parameter which is influencing the behaviour of the power stage is the duty cycle. Neglecting second order effects, the variation of the supply voltage is orthogonal to the variation of the duty cycle and superposition allows to derive the duty cycle perturbations influence on the output current. Therefore $\mathbf{u}\left(\underline{s}\right)$ is set to zero and an adequate model for duty cycle variation is found, when allocating the state matrices dynamically and in dependency on the perturbation as in 28 around the DC bias point defined by $\mathbf{X}$ and $\mathbf{U}$.

$$\begin{aligned} \underline{s}\mathbf{x}\left(\underline{s}\right) &= \underline{\mathbf{A}}\mathbf{x}\left(\underline{s}\right) + \left\{\left(\underline{\mathbf{A}}_1 - \underline{\mathbf{A}}_2\right)\mathbf{X} + \left(\underline{\mathbf{B}}_1 - \underline{\mathbf{B}}_2\right)\mathbf{U}\right\} d\left(\underline{s}\right) \\ \mathbf{y}\left(\underline{s}\right) &= \underline{\mathbf{C}}\mathbf{x}\left(\underline{s}\right) + \left\{\left(\underline{\mathbf{C}}_1 - \underline{\mathbf{C}}_2\right)\mathbf{X} + \left(\underline{\mathbf{D}}_1 - \underline{\mathbf{D}}_2\right)\mathbf{U}\right\} d\left(\underline{s}\right) \end{aligned} \tag{28}$$

Considering that $\underline{\mathbf{B}}_1 = \underline{\mathbf{B}}_2$, $\underline{\mathbf{C}}_1 = \underline{\mathbf{C}}_2$ and $\underline{\mathbf{D}}_1 = \underline{\mathbf{D}}_2$ the state equations can be solved for the control to output transfer function $\underline{Y}_{ctrl_{pwr-stge}}$ in 29.

$$\underline{Y}_{ctrl_{pwr-stge}} = \underline{\mathbf{C}} \cdot \left(\underline{s}\mathbf{E} - \underline{\mathbf{A}}\right)^{-1} \cdot \left\{\left(\underline{\mathbf{A}}_1 - \underline{\mathbf{A}}_2\right)\mathbf{X}\right\} \tag{29}$$

$$\underline{Y}_{line_{pwr-stge}} = \frac{\frac{1}{1-d}}{R + \frac{R_L}{1-d} + \frac{R_L R}{R_C+R}\frac{d}{(1-d)^2}} \frac{1 + \underline{s}R_C C}{1 + \underline{s}\frac{R_C C + \frac{L+R_L R_C C}{R(1-d)} + \frac{dL}{(R+R_C)(1-d)^2} + \frac{R_L C}{(1-d)^2}}{1 + \frac{R_L}{R(1-d)} + \frac{dR_L}{(R+R_C)(1-d)^2}} + \underline{s}^2 \frac{LC}{(1-d)^2} \frac{R+(1-d)R_C}{R + \frac{R_L}{1-d} + \frac{R_L R}{R_C+R}\frac{d}{(1-d)^2}}} \tag{30}$$

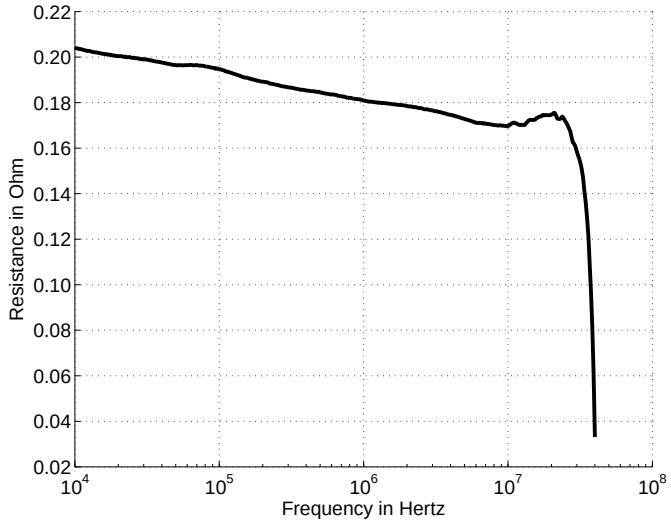


Fig. 7. Measured equivalent series resistance of output capacitor

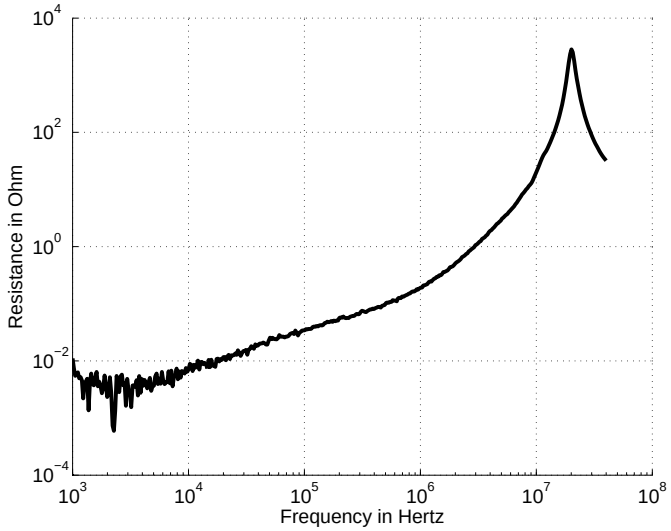


Fig. 8. Measured equivalent series resistance of boost inductor

The DC bias point $\mathbf{X}$ is obtained when setting $\underline{s} = 0$ in the first equation of 24 yielding 31.

$$\mathbf{X} = \begin{pmatrix} \frac{1}{R(1-d)} + \frac{d}{(R_C+R)(1-d)^2} \\ \frac{1}{1-d} \end{pmatrix} \frac{V_{supply}}{1+\frac{1}{R(1-d)}+\frac{dR_L}{(R_C+R)(1-d)^2}} \tag{31}$$

While [23], [34] consider the inductor and capacitor resistance statically, the control transfer function involves R_C and R_L into the dynamic response through the operating point. Setting these vectors into 29 solves the duty cycle to output current transfer function $\underline{Y}_{line_{pwr-stge}}$ to 33.

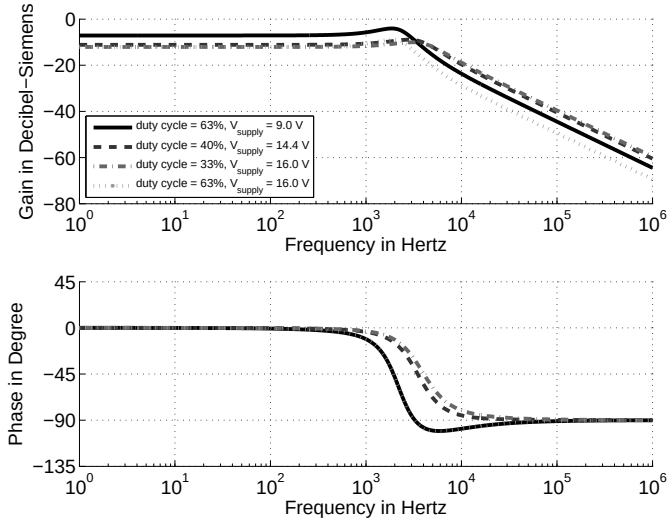


Fig. 9. Transfer function $\underline{Y}_{line_{pwr-stge}}$ of the output current from the boost power stage as a response to supply voltage variation including the parasitic resistances of the boost inductor and the output capacitor.

Figure 10 shows the corresponding reaction of the power stage to a duty cycle variation in form of a bode plot. These two system characteristics can be linearly superimposed, when second order effects are neglected, according to 32.

$$\begin{aligned} \underline{Y}_{pwr-stge}\left(\underline{s}\right) &= \underline{Y}_{line_{pwr-stge}}\left(\underline{s}\right)\cdot\underline{v}_{supply}\left(\underline{s}\right)+ \\ &\quad \underline{Y}_{ctrl_{pwr-stge}}\left(\underline{s}\right)\cdot\underline{d}\left(\underline{s}\right) \end{aligned} \tag{32}$$

The linear combination is visualized for several operating points in figure 11.

Note that this results have been derived under several neglects:

- *Averaging*: The dynamic transfer functions derived above are only valid for frequencies lower than the switching frequency. As the switching frequency is changing dynamically according to 16, the error made by averaging is getting bigger with decreasing switching frequency.
- *CCM*: The dynamic characteristics of the power stage are only valid in continuous conduction mode. If the

$$\underline{Y}_{ctrl_{pwr-stge}} = \frac{1-\frac{R_L}{(R_C+R)(1-d)^2}}{R(1-d)^2\left(1+\frac{R_L}{1-d}+\frac{RR_L}{R_C+R}\frac{d}{(1-d)^2}\right)^2}\cdot \frac{1+\underline{s}\frac{2(1-d)^2R_CRC-\frac{R_CR_LRC+RL}{R_C+R}+(1-d)R_CR_LC}{R(1-d)^2-\frac{RR_L}{R_C+R}}+\underline{s}^2\frac{(1-d)^2RR_C^2C^2-\frac{R_CRLC}{R_C+R}+(1-d)R_CC\left(R_CR_LC+L\right)}{R(1-d)^2-\frac{RR_L}{R_C+R}}+\underline{s}^3\frac{(1-d)R_C^2LC^2}{R(1-d)^2-\frac{RR_L}{R_C+R}}}{1+\underline{s}\frac{R_CC+\frac{L+R_LR_CC}{R(1-d)}+\frac{dL}{(R+R_C)(1-d)^2}+\frac{R_LC}{(1-d)^2}}{1+\frac{R_L}{R(1-d)}+\frac{dR_L}{(R+R_C)(1-d)^2}}+\underline{s}^2\frac{LC}{(1-d)^2}\frac{R+(1-d)R_C}{R+\frac{R_L}{1-d}+\frac{R_LR}{R_C+R}\frac{d}{(1-d)^2}}} \tag{33}$$

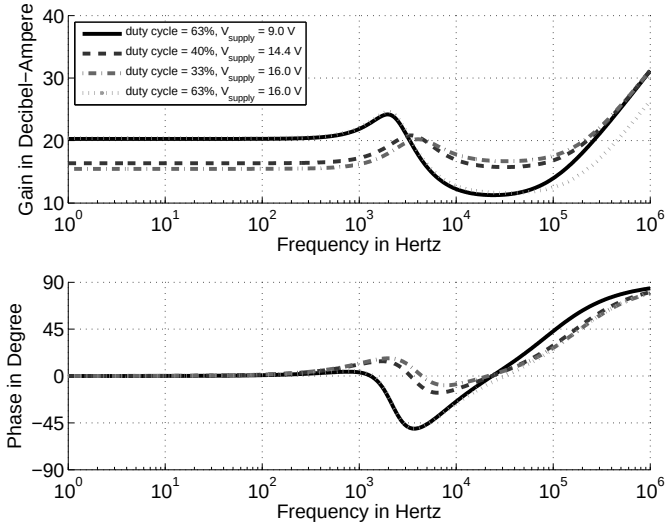


Fig. 10. Transfer function $\underline{Y}_{ctrl_{pwr-stge}}$ of the output current from the boost power stage as a response to duty cycle variation including the parasitic resistances of the boost inductor and the output capacitor.

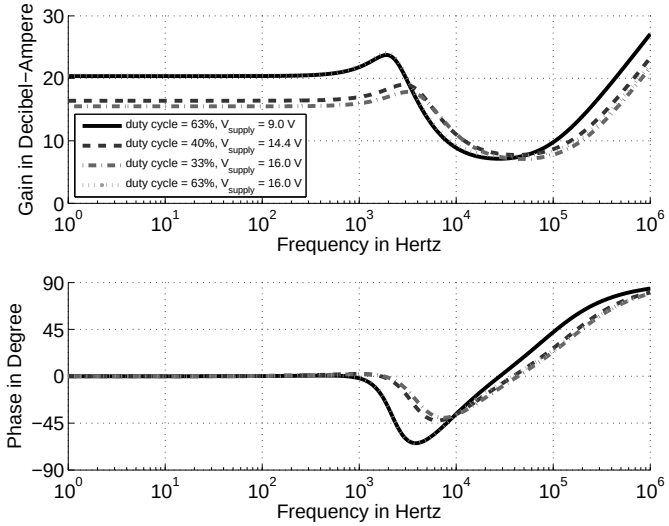


Fig. 11. The resulting transfer function for a current driving boost converter $\underline{Y}_{pwr-stge}$ as a linear superposition of its two input reactions.

converter is leaving the continuous conduction mode, due to decreasing switching frequency, a third state would need to be introduced. The state variables are then dependent on the natural oscillations of parasitic components of semiconductors and filter. Therefore second order parasitics (parasitic capacitance of boost inductor, equivalent series inductance of the electrolytic capacitor and nonlinear C_{oss} of the switches) would need to be taken into account.

- *Load*: The load was assumed to be resistive. If the parasitic components of the load start to interact in the

frequency range of interest, they would need be taken into the model. This could be the inductance of the wiring harness or – in case the battery to be charged has a small capacitance – the capacitance value of the battery itself.

- *Orthogonality of supply voltage and duty cycle*: In case the numerical value of the product of $\underline{v}_{supply}(\underline{s})$ and $\underline{d}(\underline{s})$ as the perturbations of supply voltage and duty cycle are not negligible within the allowed averaging period, their interaction is also contributing to the transfer function of the power stage as a secondary effect.

F. Resulting Transfer Functions and Stability Considerations

The product of all above shown transfer functions yields the open loop transfer function $\underline{H}_o$ according to 34.

$$\underline{H}_o(\underline{s}) = \underline{H}_{td}(\underline{s})\,\underline{H}_{gd}(\underline{s})\,\underline{Z}_{sense}(\underline{s})\,\underline{H}_{ctrl}(\underline{s})\,\underline{Y}_{pwr-stge}(\underline{s}) \tag{34}$$

As the modulator is not included in the model, the model is only relevant at low frequencies. When approaching

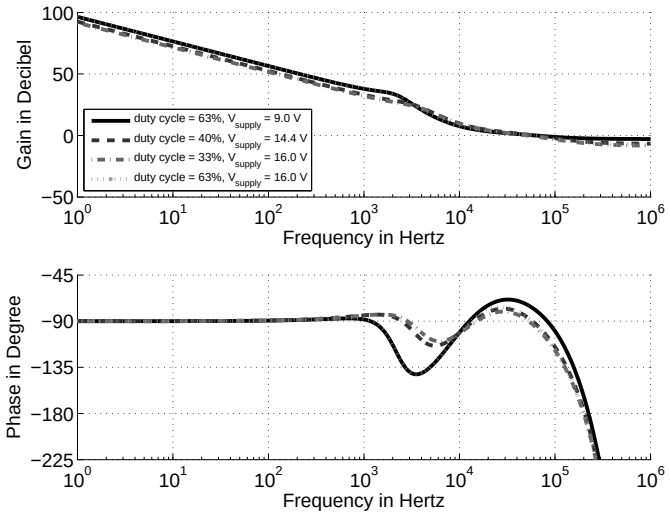


Fig. 12. The resulting open loop transfer function $\underline{H}_o(\underline{s})$.

the switching frequency small signal models have been described in [35]–[38].

The important result out of this bode diagram are the criteria for stability. For all conditions the phase margins are quantitatively given in table I and the gain margins are given in II.

Note that the minimum phase margin is not achieved at the frequency, where the open loop is running out of gain, but at a lower frequency. The minimum phase margin, located at a lower frequency than the zero crossing, is therefore the criterion to judge the stability of the converter.

As the gain margins are found above the switching frequency, their validity is doubtful according to the above described neglects.

condition d; V_{supply}	0 dB crossing frequency	phase margin at 0 dB crossing	min. phase margin
63 %; 9.0 V	63 kHz	101°	38°
40 %; 14.4 V	60 kHz	89°	66°
33 %; 16.0 V	51 kHz	91°	70°
63 %; 16.0 V	57 kHz	90°	38°

TABLE I

PHASE MARGIN OVERVIEW OF THE OPEN LOOP TRANSFER FUNCTION.

condition d; V_{supply}	$-180°$ crossing frequency	gain margin at $-180°$ crossing
63 %; 9.0 V	224 kHz	2.4 dB
40 %; 14.4 V	204 kHz	4.9 dB
33 %; 16.0 V	198 kHz	6.1 dB
63 %; 16.0 V	201 kHz	5.6 dB

TABLE II

GAIN MARGIN OVERVIEW OF THE OPEN LOOP TRANSFER FUNCTION.

Based on the open loop results, the closed loop transfer function can be derived according to block diagram 5 via equation 35.

$$\underline{H}_{closed}(\underline{s}) = \frac{\underline{H}_o(\underline{s})}{1 + \underline{Z}_{sense}(\underline{s})\,\underline{H}_o(\underline{s})} \tag{35}$$

This finally leads to the closed loop bode plot in figure 13.

V. EXCEEDING THE CONTROL LIMITS

Section IV is valid for certain load ranges. Whenever the battery is fully charged or completely discharged the control loop exits the linear range of the PI-controller and two other state descriptions are valid. Those are described in this section.

A. Undervoltage Limitation

For a low ohmic load, e.g. when a discharged battery is attached, the control loop is saturated and even the resulting duty cycle is zero, the power stage of the boost converter still conducts. This is a consequence of the inductor and the conducting diode in case the voltage at the output of the boost converter is lower than its input voltage. As this converter is designed for charging batteries, the output voltage does not stay constant but rises, as the battery is getting charged to the input voltage. At this instance the control loop is taking over, the output current

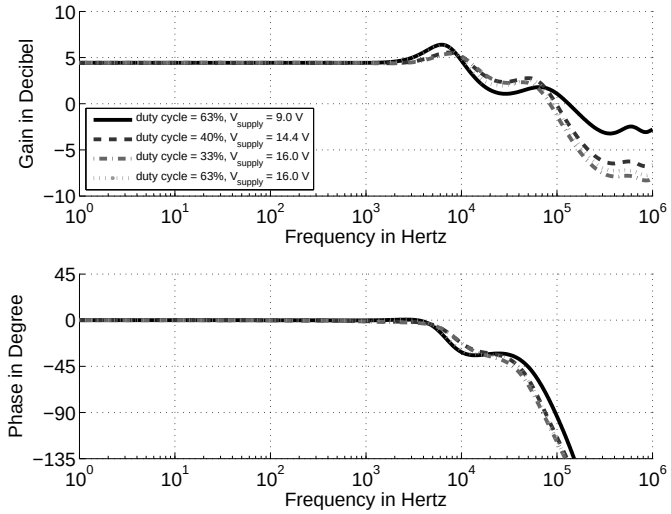


Fig. 13. The modeled closed loop transfer function $\underline{\underline{H}}_{closed}(\underline{s})$.

is regulated and the output voltage further rises so that the charging of the battery can continue under defined conditions.

In case of misuse, e.g. applying a low ohmic load, the voltage would not rise. The converter can be protected against damage in this case by designing a fuse or a positive temperature coefficient resistor (PTC) into the power path. Either one of those protection elements must be designed, to open the circuit as soon as the maximum stress of the rectifier diode and the boost inductor is reached. On the other hand, the protection devices shall not trigger with the high inrush current, when an empty battery is attached to the converter. For this event, the power path needs to be designed to withstand the worst case regular load, which is the largest capacitance, that shall get charged.

Another way of limiting the short circuit current is the usage of a synchronous rectifier and turn this transistor into a linear regulator for lower output voltages than input voltages. In this case a thermal protection circuit can be applied to it and the initial charging can be controlled.

B. Overvoltage Limitation

On the other end of the regulation range, the output voltage is exceeding the maximum battery voltage, i.e. the battery is completely charged. In this case the switching action can simply be stopped. It restarts as soon as the battery voltage drops below a certain value. The trigger limits for those two non-linear interactions with the current control loops have a hysteresis for debouncing the control abnormalities, which especially occur with very small load capacitances. This way a wide load range can be tolerated.

Whenever this over voltage protection (OVP) is getting activated, the current source nature of the converter is turned into a voltage source temporarily.

VI. Experimental Verification

The calculated and described boost converter has been built and the schematic of the power stage is given in figure 14.

The relevant comparisons to the above theoretical derivation are shown in this section.

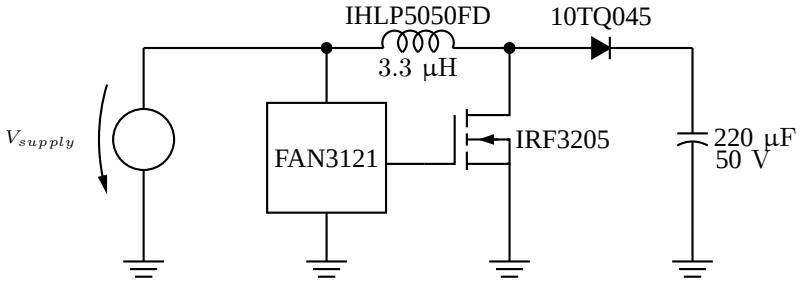


Fig. 14. Schematic of power stage.

A. Switching Parameters

In section III the switching parameters f_{sw} and d have been derived from the passive circuitry around the hysteretic comparator. For the given application, the values have been entered in the equation and the error amplifier output voltage v_{err} was chosen as parameter to plot the results in figure 15. There is a slight derivation with the offset of the two measured graphs compared to the predicted line from calculations. It is assumed that it is originated from the component tolerances. At quite low error voltage amplitudes the measurements are falling off faster than predicted. It was found that the output impedance of the reference voltage source V_{ref} was quite high. Therefore it had a non neglect able variation over the control range which also led to even more limited dynamical range on the low end.

The duty cycle limitation on the high end as adjusted through the analytical results in equation 17 was fulfilled tightly as can be seen in figure 16. On the low end of the modulation range, the switching action stopped slightly before the predicted point, however the tolerance is acceptable especially with respect to the low cost reference voltage generation.

B. Control

The duty cycle range is the limit for the linear control range, i.e. the range where the controller is regulating the output current to a set reference value. Figure 17 shows a load step from the undervoltage range, where the error amplifier is in negative saturation to the adjusted current value of 4 A. Load step responses within the linear regulation range are shown in figures 18 and 19. These diagrams, show the converter operating and the regulator response during a positive and a negative load step respectively. In both cases the controller is driven into saturation. When leaving either positive or negative saturation, the settling of the converter operation can be seen in both cases.

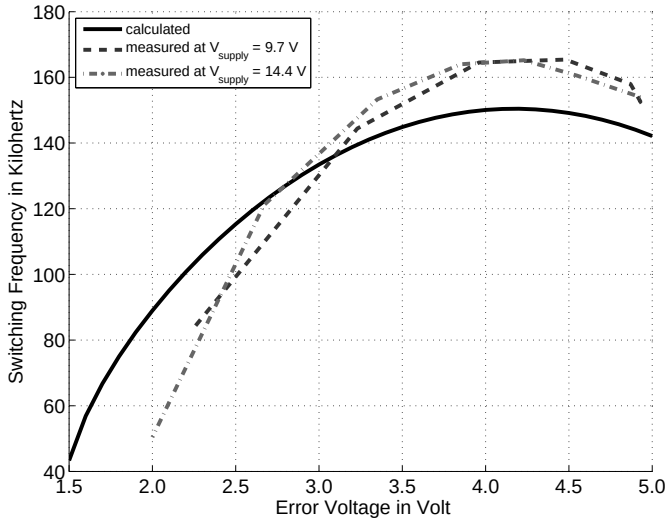


Fig. 15. The calculated switching frequency from equation 16 compared to the measured switching frequencies at two different supply voltages of the converter.

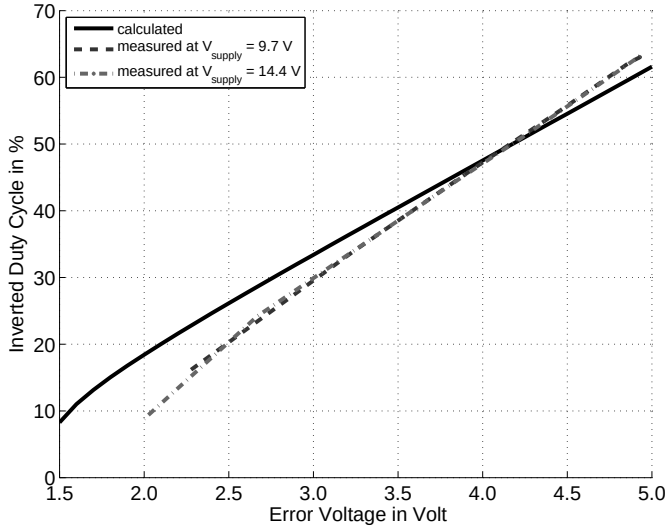


Fig. 16. The variation of the invertered duty cycle, i.e. the off-time in relation to the period, with changing error amplifier voltage for calculation results and measurement results at two different supply voltages.

C. Overvoltage Protection

The overvoltage protections (OVP) task is to avoid overcharging the battery. It is turning the converter off, whenever the upper hysteretic value of the OVP is reached and whenever the battery voltage is falling below the lower limit of the hysteresis, it is resposible for the converters restart. Through this voltage feedback the converter is operating in a bang bang regulated and slow voltage mode. However during the on-times of this voltage loop,

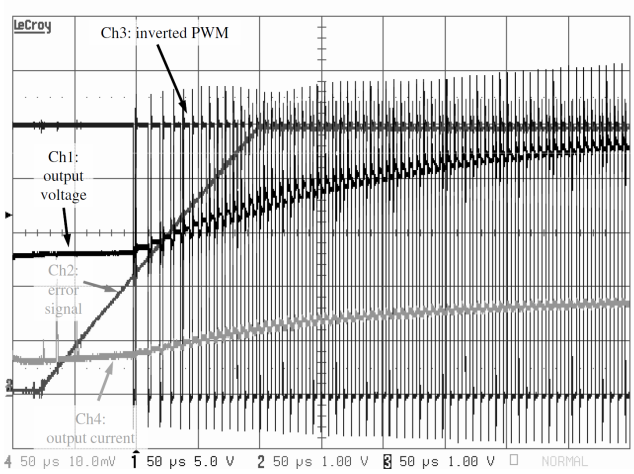


Fig. 17. A load step from output undervoltage lockout to full output power: yellow and green are output voltage and current.

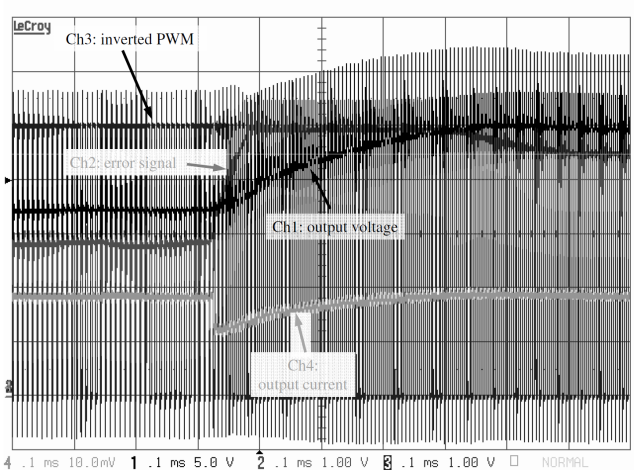


Fig. 18. The response of output current and output voltage to a load transition from light load ($R = 4\ \Omega$) to maximum load within regulation range ($R = 6\ \Omega$). Also shown is the response of the error amplifier and the inverted PWM signal in background.

the converter is operating as a current source. The action can be simulated by applying a high ohmic load, which will take the error amplifier out of the linear operation region as described in section V-B and therefore ensure that the output voltage would exceed the overvoltage protection limit, while the current loop is trying to keep the 4 A current at the output. A single overvoltage trigger and its soft recovery in to normal current source operation of the converter is shown in figure 20.

Figure 21 shows the voltage loop response and the current loop operation in the enabled period in dependency of the applied load impedance. This is leading to output currents from 3.9 A down to 0.5 A, while keeping the output voltage at the desired maximum.

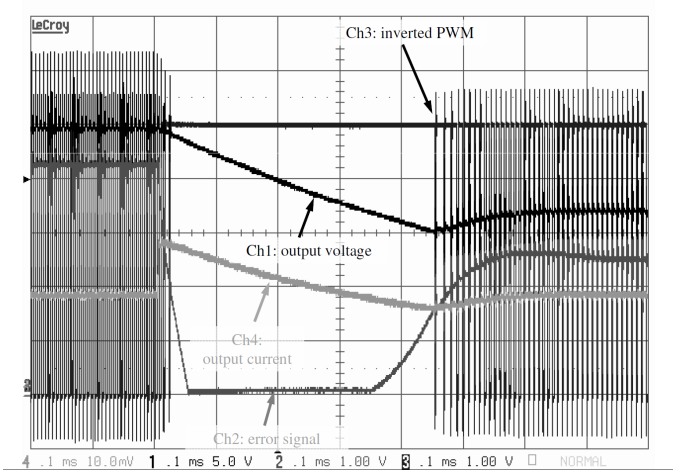


Fig. 19. The inverse transition to figure 18 from $R = 6\ \Omega$ to $4\ \Omega$.

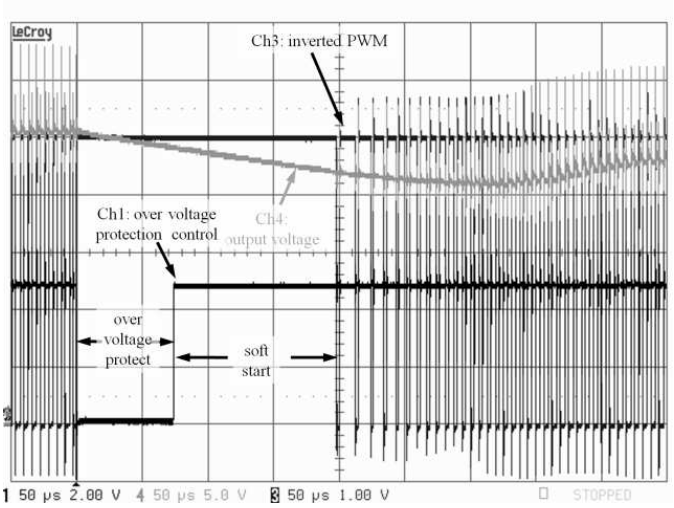
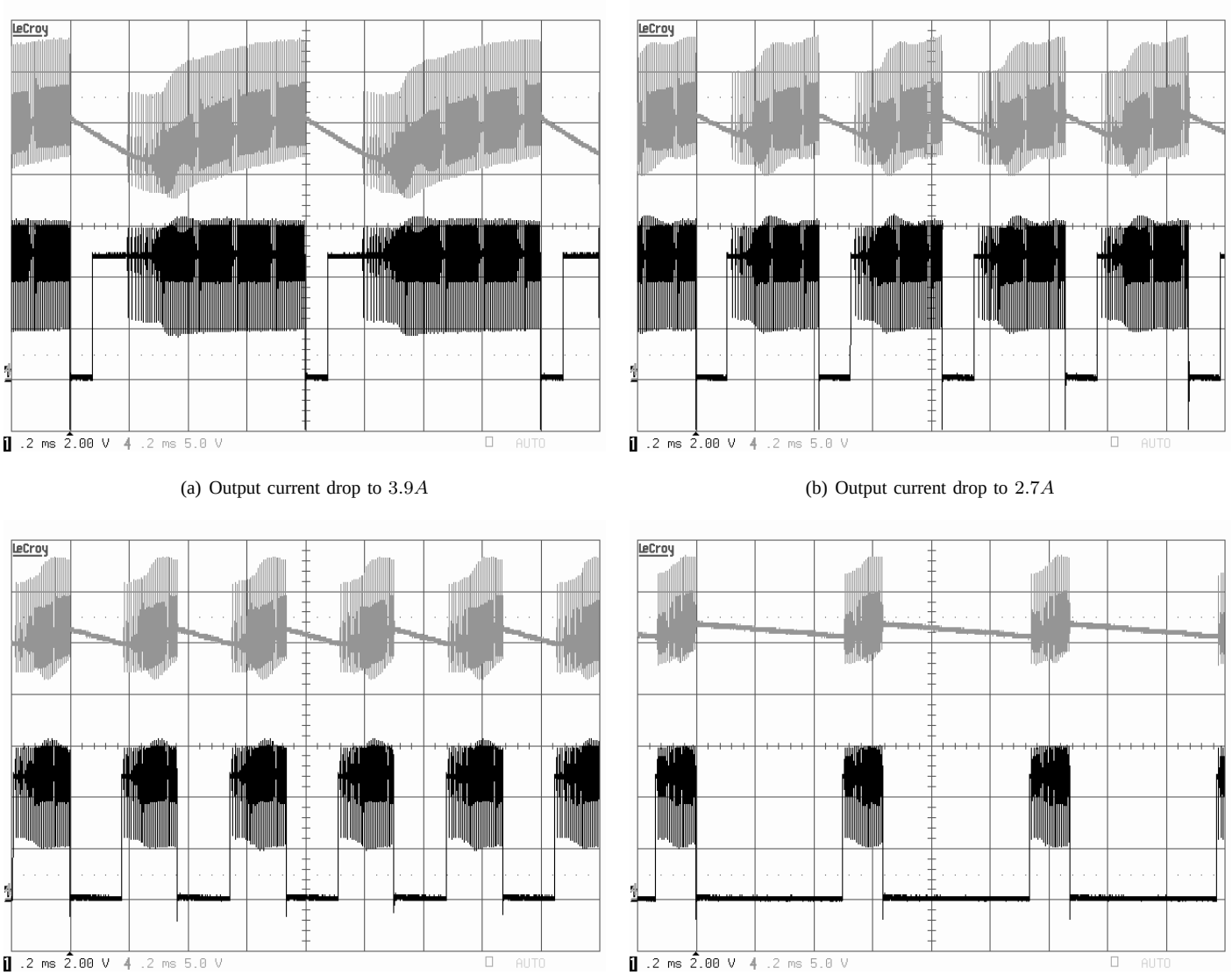


Fig. 20. Timing of the overvoltage protection and its hysteresis. Shown is the output voltage and the control signal from the overvoltage protection signal on oscilloscope channel 1 and the inverted PWM signal on channel 3 in the background.

D. Efficiency

The energy efficiency of the converter is dependent on the supply voltage. It is falling with decreasing supply voltage as the input current is rising, which is the main responsible parameter for the losses. Within the defined operation range as described in section II-A, the efficiency is beyond $91\ \%$. At the nominal input voltage of $14.4\ \mathrm{V}$ an efficiency higher than $93\ \%$ was achieved, which is $1\ \%$ more than described in previous publications as described in section I. The graphs in figure 22 are visualizing these numbers. All three graphs are cut off at the lower power range, when the converter left the switching operation range and the output voltage fell to the



(a) Output current drop to $3.9A$

(b) Output current drop to $2.7A$

(c) Output current drop to $1.6A$

(d) Output current drop to $0.5A$

Fig. 21. Overvoltage protection at different overload levels, where the upper signal on channel 4 is the output voltage and the lower one is the overvoltage protection trigger signal on channel 1.

input voltage. The efficiency in those areas is even higher, because no switching losses are contributing to the total dissipation. However that mode is not representative for a switched power converter.

The resulting thermal representation of the converter is shown in the figure 23. The hottest components in the picture are the sense resistors for the current feedback and the rectifier diode, followed by the output electrolytic capacitor and the power switch. A more quantitative but less precise representation of the loss distribution is shown in table III. These numbers where taken from an infrared thermometer.

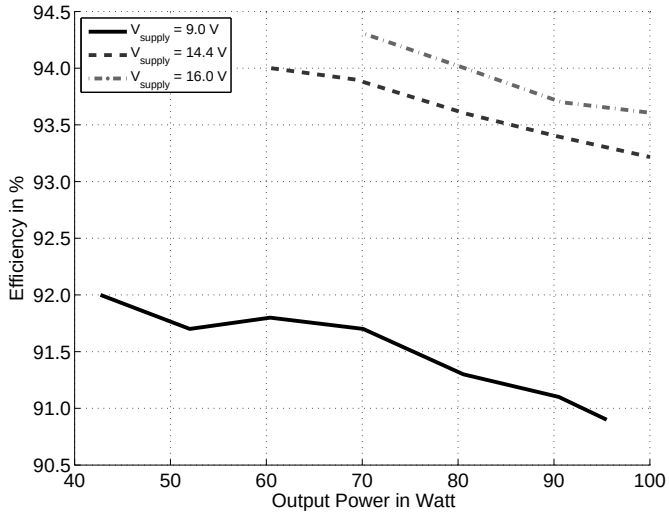


Fig. 22. Efficiency at normal operating conditions (within regulation limitations) for various supply voltages

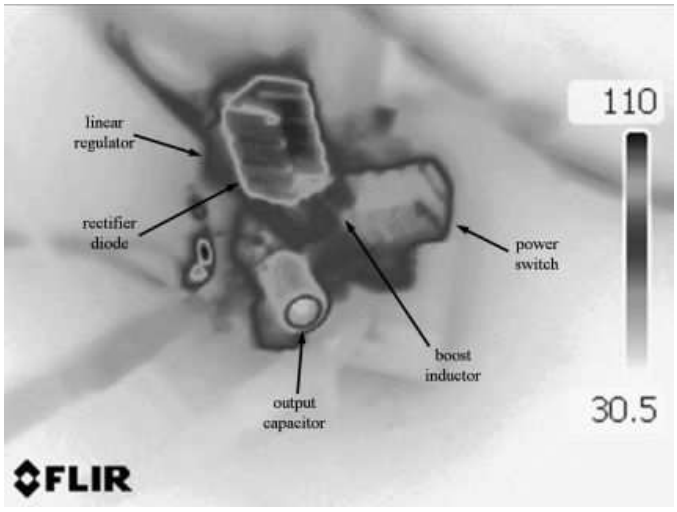


Fig. 23. Thermal photography of converter, while operating from a supply voltage $V_{supply} = 14.4$ V at an ouput power of $P_{out} = 100$ W (efficiency $\eta = 93$ %)

E. Reliability

As shown in the efficiency diagram 22, the converter was designed to barely fulfill the output power specification at the lowest supply voltage of $V_{supply} = 9$ V, which is the most economical design criteria. This however enables the converter to provide more power at higher input voltages. With disabled overvoltage protection, the converter was stress tested with accelerated voltage stress at the output. The converter passed this stress test and could operate also in steady state and thermal saturation up to the maximum input voltage by relying on the duty cycle limitation

spot	ϑ
rectifier diode	$96\ ^\circ\mathrm{C}$
power switch	$68\ ^\circ\mathrm{C}$
boost inductor	$84\ ^\circ\mathrm{C}$
output capacitor	$82\ ^\circ\mathrm{C}$
linear regulator for auxiliary voltage	$78\ ^\circ\mathrm{C}$
ambient	$60\ ^\circ\mathrm{C}$

TABLE III

TEMPERATURE θ ON THE SURFACE OF THE COMPONENTS MEASURED WITH AN INFRARED THERMOMETER.

from the unsymmetrical hysteretic controller. The efficiency in this area is further falling with increasing losses, however it stays under any condition beyond $91\ \%$ as visualized in figure 24.

Even there is no possibility to cut back on the cost of the power stage, because it is barely reaching the output

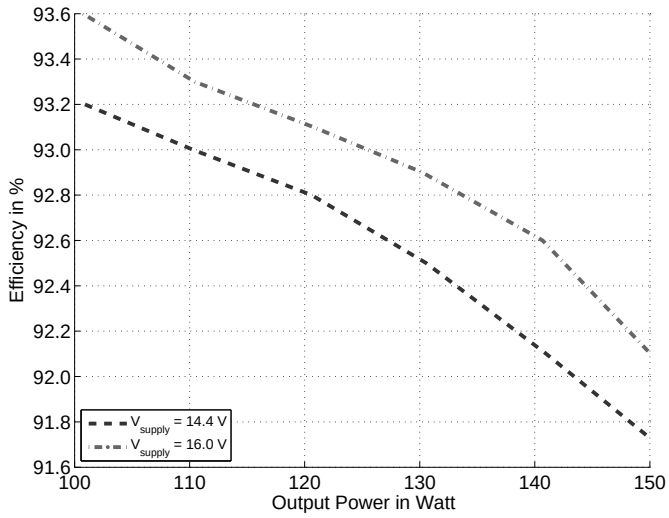


Fig. 24. Efficiency at extended output voltage conditions for normal and high input voltage conditions.

requirement at the lowest supply voltage, it might be possible to reduce cost on the mechanical design, as the converter could reach the thermal steady state also under those stress conditions.

F. Voltage-Current Characteristic

Finally a number of operating points where captured to record the voltage-current characteristic of the output of the boost converter. Figure 25 is showing those characteristics for various input voltages.

The left side of the diagram (constant output voltage, current following the load) is representing the undervoltage

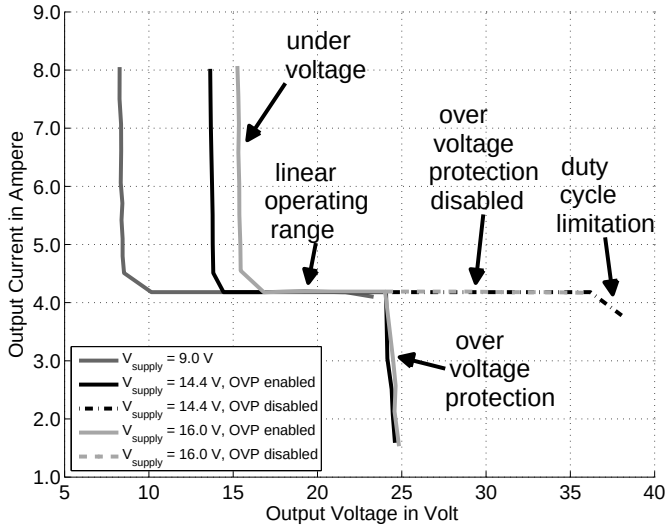


Fig. 25. Output characteristics under normal operating conditions and output stress test measured at different input voltages.

mode described in section V-A. The output voltage is following the input voltage at this point and the converter is not switching. With decreasing load resistance the current is rising and so are the conduction losses in the diode and the inductor. Therefore the voltage curve is slightly tilted to the left in the diagram with increasing stress.

During constant current operation the output current is under control of the current loop. In both, normal operation and stress test conditions all graphs overlap, which proofs the operation of the control loop. Only the graph for the low supply voltage $V_{supply} = 9$ V is bending toward the voltage-axis for high output voltages due to the duty cycle limitation.

With OVP enabled, i.e. under normal operating conditions, the graphs for $V_{supply} = 14.4$ V and $V_{supply} = 16$ V are cutting off precisely at the reached maximum output voltage and the converter is operating in OVP mode as a constant voltage source as described in section V-B.

Under stress conditions, i.e. with disabled OVP, the converter continues behaving like a constant current source at its output up to 35 V. At this point for the nominal supply voltage $V_{supply} = 14.4$ V the maximum duty cycle is reached and the current starts to drop as the graph for $V_{supply} = 9$ V does at the boundary of the specification.

VII. Outlook

The battery voltage of cars can drop to low voltages, when the engine is started. Dependent on the ambient temperature this condition can last for a longer time, than the energy storage components in this application can cover. It could therefore be of interest to operate the converter at low input voltages. Figure 26 shows the operation of the converter at $V_{supply} = 4.5$ V. Due to the duty cycle limitation the desired output current of 4 A can not be reached. A dynamical duty cycle limitation dependent on the input voltage could be added as another feature in the converter to ensure operation down to those supply voltage values.

Figure 27 is confirming that the power stage would be capable to operate with adequate efficiency beyond $85\ \%$

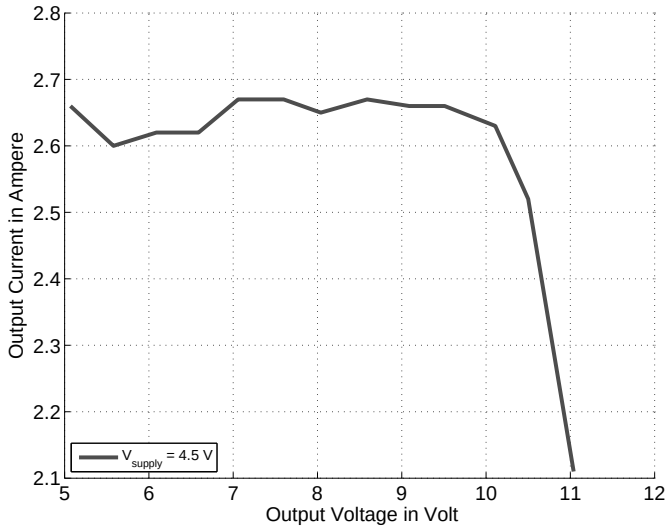


Fig. 26. Output characteristic at low input voltage.

down to low input voltages.

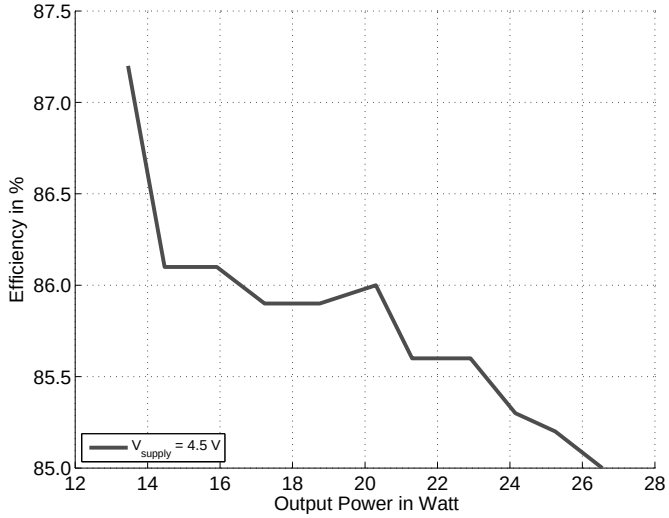


Fig. 27. Efficiency at low input voltage.

VIII. Conclusion

A switched power converter to charge a laptop computer battery from the energy net of a car was developed. After describing the specification and the demands for the supply, the solution was broken down into various features,

consisting of a boost power stage, controlled by a current loop through an unsymmetrical hysteretic modulator. Additionally an overvoltage protection feature and a soft start functionality was added.

Other applications targeted by the design are emulation of solar cells and general constant current sources.

The operation of the unsymmetrical modulator was described analytically in detail by analyzing the hysteretic window and the carrier generation. This led to the equations for the switching parameters on-time t_{on}, off-time t_{off}, switching frequency f_{sw} and the duty cycle d. This derivation was used to define the linear operating range of the control.

Next the control loop was broken down into the various blocks within the loop, consisting of a gate driver, the current sensing with its anti-aliasing filter, the traditional PI-controller and the power stage including its first order parasitic components. The results of this analysis where used to predict the stability of the system in terms of phase and gain margins.

The converter was designed in a matter that it could also operate beyond its regulation boundaries in output undervoltage and output overvoltage mode.

Through a prototype the described derivations where verified. Measurement of switching parameters gave good agreement with simulation, the control loops functionality was proven through load steps. Beyond the control the functionality in the under and overvoltage mode was shown through measurements. The efficiency of the converter within the specified operating range was found to exceed $90\ \%$. Under nominal operating conditions it exceeded $93\ \%$ at any point of load up to $100\ \mathrm{W}$. Beyond the specified operating range a reliability test proofed the capability of operation up to $150\ \mathrm{W}$ with efficiency beyond $91\ \%$ at any point. The output characteristic of the converter in all possible operation modes was captured and described.

Despite the relatively low switching frequency ($50\ \mathrm{kHz}$ to $160\ \mathrm{kHz}$) a fast step response (steady state is achieved after $400\ \mu\mathrm{s}$) was achieved, enabled by the high control bandwidth of the self oscillating control scheme.

Finally an outlook to a low operating voltage feature was given, which could further be included as another nonlinear interaction with the tightly controlled current loop.

The converter is working up to the specification and is useable to charge a laptop battery from the energy system of a car.

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