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Published in:
Microwave & Optical Technology Letters

Link to article, DOI:
10.1002/mop.27477

Publication date:
2013

Document Version
Publisher's PDF, also known as Version of record

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MILLIMETER-WAVE INP DHBT POWER AMPLIFIER BASED ON POWER-OPTIMIZED CASCODE CONFIGURATION

Tom K. Johansen,[1] Lei Yan,[1] Jean-Yves Dupuy,[2] Virginie Nodjiadjim,[2] Agnieszka Konczykowska,[2] and Muriel Riet[2]
[1] Department of Electrical Engineering, Technical University of Denmark, Ørsteds Plads, building 348, 2800 Kgs. Lyngby, Denmark; Corresponding author: tkj@elektro.dtu.dk
[2] III-V Labs, Joint Laboratory between Bell Labs, Thales Research and Technology and CEA/LETI, F-91461 Marcoussis, France

Received 16 August 2012

ABSTRACT: *This letter describes the use of a power-optimized cascode configuration for obtaining maximum output power at millimeter-wave (mm-wave) frequencies for a two-way combined power amplifier (PA). The PA has been fabricated in a high-speed InP double heterojunction bipolar transistor technology and has a total active emitter area of 68.4 μm2. The experimental results demonstrate a small signal gain of 9.8 dB and saturated output power of more than 18.6 dBm at 72 GHz with a peak power-added efficiency of 12%. The benefits of the power optimized cascode configuration over the standard cascode configuration at mm-wave frequencies are confirmed by both simulations and experimental results.* © 2013 Wiley Periodicals, Inc. Microwave Opt Technol Lett 55:1178–1182, 2013; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.27477

Key words: *heterojunction bipolar transistor; millimeter-wave; monolithic microwave integrated circuit; power amplifier*

1. INTRODUCTION

A bottleneck for emerging millimeter-wave (mm-wave) wireless communication systems in the E, W, and G-band is the availability of high power amplifiers (PAs) at these frequencies. Target specifications for PAs in mm-wave wireless systems are difficult to meet with silicon-based devices due to their low breakdown voltage and low-power density. Recently, a number of GaN high electron-mobility transistor (HEMT)-based E-band PAs demonstrating Watt-level output powers have been published [1, 2]. Despite the fact that mm-wave PAs based on heterojunction bipolar transistor (HBT) technologies reported to date delivers less output power than their HEMT counterparts, high-speed InP double heterojunction bipolar transistor (DHBT) technology is well-suited for power applications and allows a high level of integration [3]. Furthermore, the potential for power amplification beyond 200 GHz has recently been demonstrated using InP DHBT technology [4].

For mm-wave InP DHBT PAs, the cascode cell is typically the preferred configuration due to its higher power gain compared to the common-emitter (CE) and common-base (CB) configurations [3, 5–7]. At similar device bias conditions, the cascode cell should ideally be able to deliver twice the output power compared to a CE-based cell because the voltage swing from the two cascode devices sum together at the output. This condition, however, is rarely obtained in practice for two reasons. First, the output power is limited mainly by the saturation of the CB device. Second, the low impedance level seen toward the emitter of the CB device will lead to a nonoptimal loading of the CE device. As a result, the output power from the CE device is rather low as the optimal load-line trajectory is not achieved. In Ref. 8, it was proposed to use a small-valued capacitor at the base of the cascode cells CB device to delay its saturation by capacitive voltage division. It was also shown that inclusion of an additional inductance to form a complete interstage matching network between the devices resulted in an optimal output power for a distributed PA in the DC-12-GHz frequency range. The concept of interstage matching between devices can even be extended to multiple stacked devices. In Ref. 9, four interstage-matched SiGe HBT devices were used to implement a high voltage/high power architecture at 30 GHz. The high output power potential of this approach was proven using an experimental load-pull setup. The first fully integrated mm-wave PA using the interstage matching network to improve the output power of a three level FET stack at 60 GHz was recently reported in Ref. 10.

In this letter, it is described how the interstage matching concept can be applied to optimize the power performance of an InP DHBT cascode cell at mm-wave frequencies. A two-way combined PA targeting the lower E-band wireless frequency range (71-76 GHz) is designed using the power-optimized cascode configuration. The high-power density obtained from measurements on the PA confirms the benefits of the interstage-matched cascode over the standard cascode configuration at mm-wave frequencies. To the best of the authors' knowledge, our work represents the first InP DHBT-based PA and the highest operation frequency for any PA using the power-optimized cascode configuration.

2. InP DHBT TECHNOLOGY

The InP DHBT devices used in this work were fabricated in a triple mesa self-aligned process. The device technology features a hexagonal emitter with a drawn width of 0.7 μm and targets high-swing mixed-signal ICs for operation speed at 100 Gbit/s and above [11]. Multifinger devices with breakdown voltage of BV_{ceo}>4.75 V are available for power applications. The current gain (H_{21}) and maximum available/stable gain (MAG/MSG) for a three-finger device is shown in Figure 1. The three-finger device shows a cut-off frequency of $f_T \approx 258$ GHz and MAG $\approx$ 10.4 dB at 72 GHz when biased at $V_{ce} = 2.5$ V and $I_c = 45$ mA. This bias point was chosen to maximize the output power under class-A operation with the constraint of being well within the safe-operation area of the three-finger device. The multifinger devices have been modeled by combining individual single-finger device models with an external parasitic network. Each finger is modeled using the UCSD HBT model modified slightly for better adoption to the InP DHBT devices considered [12]. An excellent agreement between measured and modeled characteristics is shown in Figure 1, all the way up to the highest measurement frequency of 110 GHz.

3. CIRCUIT DESIGN

3.1. Interstage-Matched Cascode Cell

The cascode cell with the proposed interstage matching network is shown in Figure 2. The interstage matching network consists of a shunt capacitor C_p located at the base of the CB device and a series inductor L_s located between the CB and CE devices. Contrary to normal design practice, the shunt capacitor C_p do not act as an RF short at the design frequency but serve to

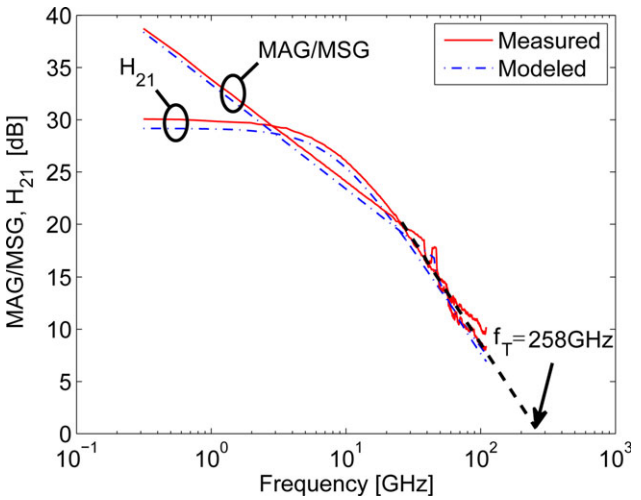

Figure 1 Measured and modeled maximum available/stable gain (MAG/MSG) and current gain (H_{21}) for three-finger InP DHBT device. The device is biased at $V_{ce} = 1.5$ V and $I_c = 45$ mA. The dashed line with slope 20-dB/decade represents the extrapolated H_{21} curve. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

reduce the voltage swing impressed across the base-emitter junction of the CB device. Furthermore, the shunt capacitor increases the real part of the impedance looking toward the CB device, whereas the inductance L_s increase its imaginary part. The resistance R_b ensures that the effect of C_p is not shorted by the decoupling capacitor at the base supply. To reduce its loading effect, it should be chosen according to $R_b \gg 1/\omega C_p$. The element values of the shunt capacitance C_p and series inductance L_s can be optimized for maximum output power using nonlinear simulations near the 1-dB compression point. Figure 3 shows the reflection coefficient Γ_i at 73.5 GHz for a standard cascode cell and a cascode cell with interstage matching using three-finger devices biased at $V_{cc} = 5.0$ V, $V_b = 3.35$ V, and $I_c = 45$mA. As observed, the effect of the interstage matching network is to move the reflection coefficient Γ_i to the location of the optimum load reflection coefficient for the CE device. The optimum values for the components in the interstage matching

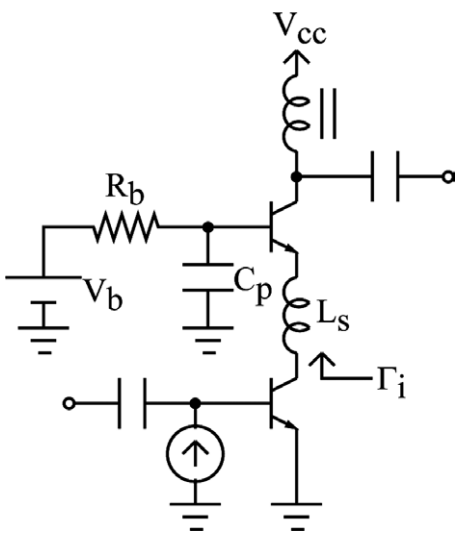

Figure 2 Schematic of cascode cell with interstage matching network. Γ_i represents the reflection coefficient between stages

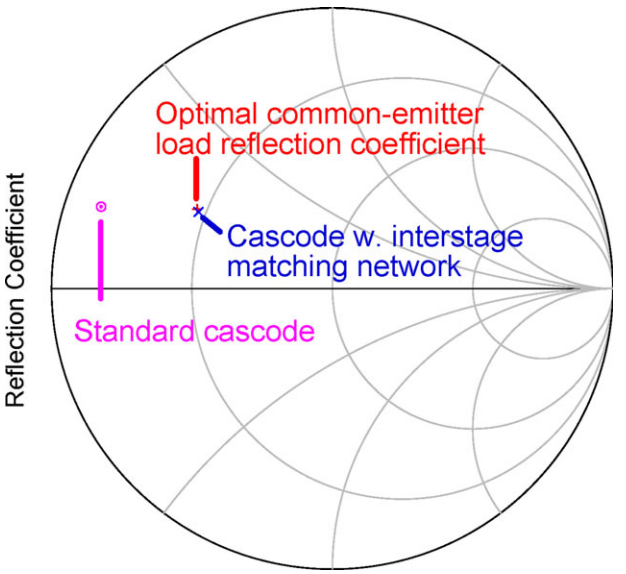

Figure 3 Reflection coefficient at 73.5 GHz for standard cascode cell (o) and cascode with interstage matching network (x). The optimal common-emitter load reflection coefficient at 73.5 GHz is also shown (+). [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

network are $C_p = 230$ fF, $L_s = 12$ pH, and $R_b = 110\ \Omega$. The capacitance value is easily realized on-chip using MIM capacitors, whereas the low inductance value can be implemented by using a fork structure. The benefits of the interstage-matched cascode cell on the large-signal performance are shown in Figure 4. Compared to the standard cascode cell, the interstage-matched cascode cell is seen to go into saturation at a higher output power level. This also has the effect of increasing the output power at the 1-dB compression point. The negative feedback effect caused by the shunt capacitor C_p reduces the linear power gain. However, the power gain at saturated power levels is actually higher for the interstage-matched cascode cell. Therefore, the interstage-matched cascode cell shows significantly higher peak power-added efficiency (PAE) compared to the standard cascode cell. Other benefits of the interstage-matched cascode cell are increased low-frequency stability due to the resistor R_b and reduced sensitivity toward layout parasitic inductance in the base access of the CB device due to the effect of the small-valued shunt capacitance C_p.

3.2. Two-Way Combined PA Design

To further increase the output power, multiple interstage-matched cascode cells can be combined in parallel. Figure 5 shows a two-way combined PA including matching structures at the input and output. Base-ballasting circuitry is included for thermal feedback. Small-valued resistors are placed between individual cells and into the bias line circuitry to prevent instabilities. A photograph of the two-way combined PA is shown in Figure 6. The chip size is 1.5×2.4 mm^2 including pads. The transmission lines are implemented as coplanar waveguides, and all the circuits were simulated using an EM-circuit cosimulation approach in Agilent ADS.

4. MEASUREMENT RESULTS

The performance of the PA has been measured on-wafer using 110-GHz GSG probes from GGB industries for the input and output. Bias for the chip was provided through decoupled DC

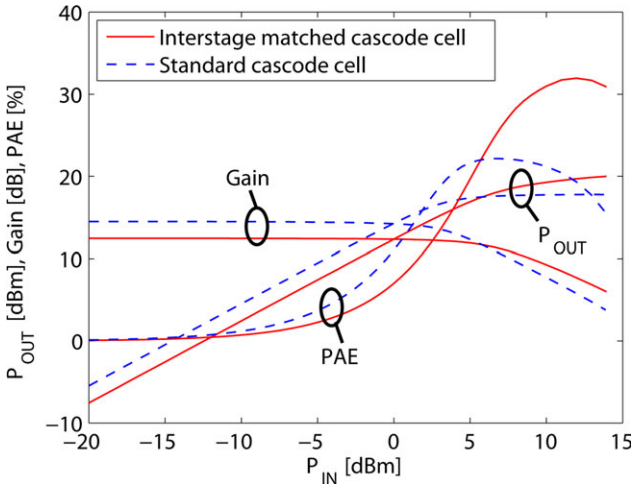

Figure 4 Simulated power gain, output power (P_{OUT}), and power added efficiency (PAE) at 73.5 GHz for standard cascode cell and cascode cell with interstage matching network. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

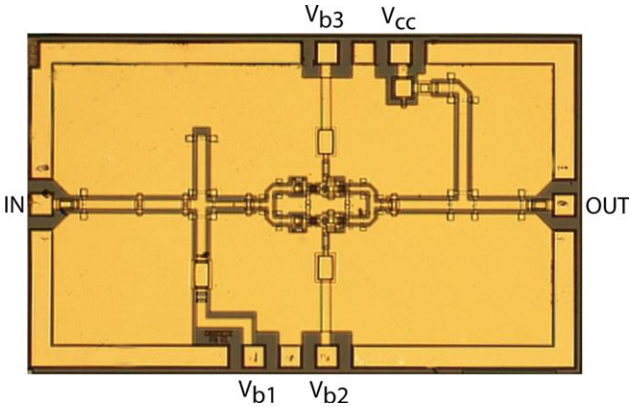

Figure 6 Microphotograph of fabricated two-way combined PA. The chip size is 1.5 × 2.4 mm^2. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

probes from cascade. During measurements, the circuit was biased from a 5 V supply, drawing a current of 90 mA. The bias voltage for the CB stage was set to 3.35 V. The small-signal performance was measured using an Anritsu ME7808B broadband vector network analyzer (VNA) calibrated to the probe tips using a calibration standard substrate. Figure 7 shows the measured and simulated *S*-parameters. Despite a slight downshift of the measured gain peak to 67.7 GHz, the PA still shows a gain larger than 8 dB in the lower E-band frequency range from 71 to 76 GHz. At 72 GHz, the measured gain is 9.8 dB while the input return loss is 11.5 dB. As the developed InP DHBT model was shown to be highly accurate under small-signal operation, the difference between measurement and EM-circuit co-simulation is believed to come from inaccuracy in the definition of the layer stack used for the EM simulation and influence from internal port parasitics.

The large-signal characterization of the PA was done using a custom-made setup able to deliver approximately +12 dBm of input power at the probe-tip in the lower E-band frequency range. The measured power is corrected for losses in the setup. Figure 8 shows the measured and simulated large-signal performance at 72 GHz. The saturated output power is expected to be somewhat larger than 18.6 dBm as it is seen that the input power is not sufficient to fully saturate the PA. Using a total active emitter area of 68.4 μm^2, the corresponding output power density is therefore at least 1.06 mW/μm^2. The measured PAE peaks around 12% at 72 GHz. The output power at 1-dB compression is around 17 dBm. The measured large-signal performance is reasonably well-predicted by the EM-circuit cosimulation approach.

For comparison purposes, a two-way combined PA using the standard cascode configuration was also implemented. Details related to the design and performance of the two-way combined PA using the standard cascode configuration including circuit schematic and chip photograph can be found in Ref. 13. The downshift in frequency for the standard cascode-based PA was observed to be somewhat larger compared to the PA with the interstage-matched cascode so its large-signal performance is measured at 69.6 GHz where the circuit is well-matched. Furthermore, the standard cascode-based PA is biased at a quiescent current of 77.8 mA in the experiment, which is around 15% lower than the quiescent bias current used for the PA with interstage-matched cascode. This was necessary to avoid thermally induced device breakdown during the large-signal measurements

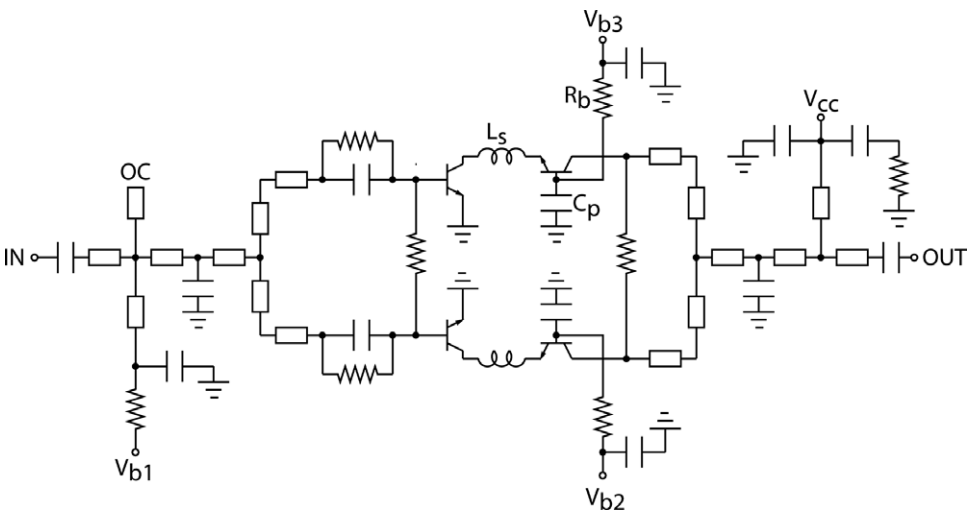

Figure 5 Schematic of two-way combined cascode cell with interstage matching employing three-finger devices

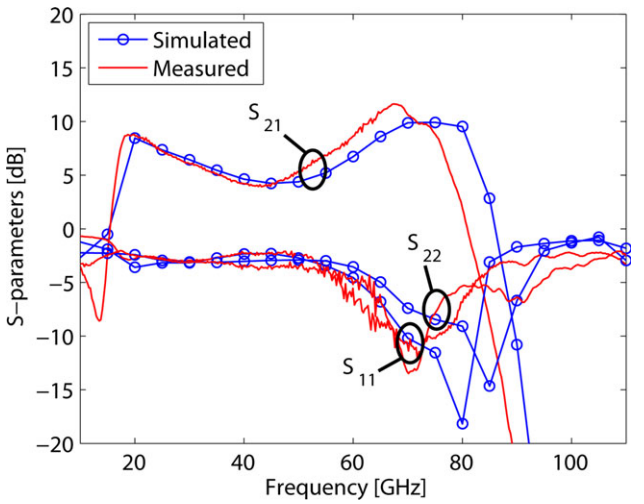

Figure 7 Measured and simulated small-signal performance of two-way combined PA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

where the supply current raises dynamically at high input power levels. The thermally induced device breakdown is believed to be caused by the early saturation of the CB device in the standard cascode configuration which also results in a large increase in the base current for this device. Table 1 compares the measured performance of the two implemented InP DHBT PA's. The benefits of the interstage-matched cascode configuration in terms of power gain, output power, and PAE for implementing mm-wave InP DHBT PAs are clearly seen. The higher output power for the PA with interstage-matched cascode configuration leads to almost a factor three improvement in the power density. From circuit simulations, the standard cascode configuration was expected to have larger small-signal gain than the interstage-matched cascode but the experimental results shows that this is not the case. Although part of this unexpected observation may be explained by the large frequency shift and low-quiescent bias current for the PA with standard cascode, the main reason for the reduction of the power gain is believed to come from the sensitivity toward parasitic inductance in the base access line

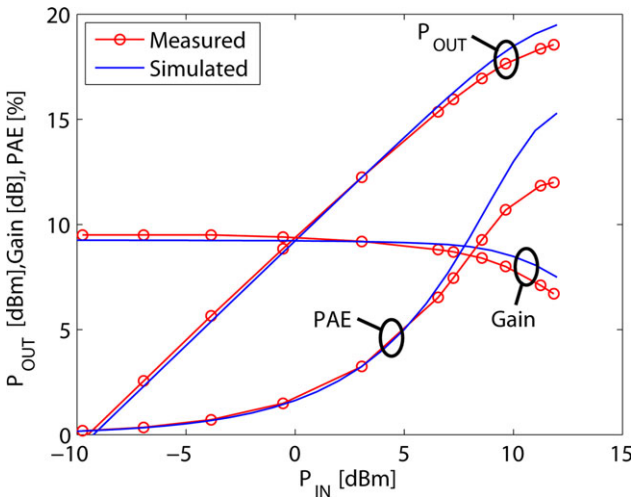

Figure 8 Measured and simulated large-signal performance at 72 GHz for two-way combined PA. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

TABLE 1 Comparison between Two-Way Combined PA's Employing Interstage Matched Cascode and Standard Cascode Configurations

PA Topology	Frequency (GHz)	Gain (dB)	P_{1dB} (dBm)	P_{sat} (dBm)	PAE (%)	Power Density (mW/μm^2)
Two-way combined interstage matched cascode	72.0	9.8	17.0	18.6	12.0	1.06
Two-way combined standard cascode	69.6	4.5	13.5	14.2	3.3	0.38

connecting to the three-finger CB device with its rather low impedance level. The interstage-matched cascode configuration is more robust against this parasitic inductance due to the effect of the small-valued shunt capacitance C_p.

5. CONCLUSION

In this letter, a two-way combined InP DHBT PA using power-optimized interstage-matched cascode configuration was reported. The PA demonstrates 9.8 dB of small signal gain at 72 GHz. The measured saturated output power at this frequency is larger than 18.6 dBm and it has a peak PAE of 12%. The high power gain, output power, and PAE obtained from the two-way combined PA clearly shows the benefits of the interstage-matched cascode configuration over the standard cascode for InP DHBT PAs at mm-wave frequencies. Furthermore, the PA with interstage-matched cascode configuration demonstrates better robustness against layout parasitics and thermal breakdown.

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SIXTY-GHz ON-CHIP BANDPASS FILTER DESIGNED WITH MULTIPLE SPLIT RING RESONATORS

Dayang A. A. Mat,[1,2] Ramesh K. Pokharel,[3] Rohana Sapawi,[1,2] Haruichi Kanaya,[1] and Keiji Yoshida[1]
[1] Graduate School of ISEE, Kyushu University, Fukuoka 819-0395, Japan; Corresponding author: dayangazra@gmail.com
[2] Department of Electronics, Faculty of Engineering, University Malaysia Sarawak, Kota Samarahan 94300, Sarawak, Malaysia
[3] E-JUST Center, Kyushu University, Fukuoka 819-0395, Japan

Received 24 August 2012

ABSTRACT: *This article describes the design of on-chip bandpass filter (BPF) with split ring resonators (SRRs) for millimeter wave application. SRR is one of the metamaterial structures commonly used in designing the passive component and is used to improve the performance of the device. In this design, the BPF is designed with two (2) and five (5) SRRs to analyze the effect of SRRs toward enhancing the performance of the BPF. The SRRs are constructed along the resonator line below the BPF structure on the second lowest metal. In this article, it is shown that the magnetic resonance frequency shifted and leaded to improvement in the insertion loss of BPF as the number of SRRs increased to five. For BPF with 5-SRRs, the insertion loss is 2.02 dB with return loss better than 30 dB, whereas for BPF with only 2-SRRs, the insertion loss is 3.29 dB with return loss better than 50 dB.* © 2013 Wiley Periodicals, Inc. Microwave Opt Technol Lett 55:1182–1185, 2013; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.27499

Key words: *bandpass filter; millimeter wave; insertion loss; return loss; SRRs*

1. INTRODUCTION

Up to now, unlicensed frequency band of 60 GHz has become great attention to many researchers. But, as the frequency increases, one will face serious signal loss in the passive device, resulting higher attenuation due to low resistivity of the silicon substrate. This would be very difficult for designers to implement the device, because it requires very high area and very large path loss. Due to this, several attempts had been made to reduce the losses as well as to shrink the chip size. Among other techniques, slow wave propagation technique is reliable, because it will provide higher quality factor (Q), low cost, and low attenuation to the design [1].

Consumers' demand of low cost, power efficient, reliable, and small form factor become increasing nowadays. To reduce cost and achieve compact size, high-level integrations are preferred. Power added efficiency (PAE) is an important metric in designing a power amplifier (PA) as a first step of designing a bandpass filter (BPF). It is a measure of PA's ability to convert the dc power of the supply into the signal power delivered to the load. PAE is maximized by minimizing the total power dissipation providing a desired output power to the system and can be summarized as Eq. (1).

$$\mathrm{PAE} = \frac{P_{\mathrm{out}}(\mathrm{dBm}) - P_{\mathrm{in}}(\mathrm{dBm})}{P_{\mathrm{dc}}(\mathrm{dBm})} \times 100 \tag{1}$$

BPF is a very important passive device in transmission system. Recently, many BPFs designed for 60 GHz waveband CMOS has been introduced by researchers [2–4]. However, these designs have several disadvantages such as high insertion loss, inadequate selectivity response, larger chip size, and wider bandwidth.

With the unique properties of negative $\mu_{\mathrm{eff}}(\omega)$ and negative $\varepsilon_{\mathrm{eff}}(\omega)$ concept, metamaterial structures become particular concern in millimeter-wave technology. Metamaterials can be defined as structures that provide electromagnetic properties not found naturally in media that provide enhancement of magnetic and dielectric properties [4]. Researches in metamaterial behavior can be categorized into two main approaches: split ring resonators (SRRs) as proposed in Ref. 5 and left and right hand (LH) theory in transmission line concept in Ref. 6. Theoretically, metamaterial ''substance'' was first proposed by Viktor Veselago in 1967 with left-handed criteria and ability to exhibit negative μ and ε. However, due to nonexistence of substances with $\mu < 0$, his theory could not be experimentally verified. Pendry et al. then introduced the SRRs medium and showed that metallic wires aligned along the direction of wave propagation could lead to negative permittivity ($\varepsilon < 0$) material [7]. Later, Smith et al. successfully achieved both negative parameters in GHz range using arrays of SRRs that form a ''left-handed'' medium [5].

In transmission line theory, LH-TL is implemented using series of capacitors and shunt inductances. This type of metamaterial is normally used in planar microstrip circuit devices. LHM has unique properties of materials especially in controlling electromagnetic waves and has negative refraction, opposite radiation pressure, backward propagation characteristic (opposite polarity of phase and group velocities), and ability to transform wave manipulation devices and system [7].

In this article, BPFs, as shown in Figure 1, are designed with 2-SRRs and 5-SRRs on pattern ground of the CMOS 0.18 μm technology. The SRRs are placed on the second lowest metal. It shows that the number of SRRs effects the performance of the BPF in terms of insertion and return losses. By placing 2-SRRs with distance apart, the insertion loss of BPF is 3.29 dB with return loss <59 dB. Meanwhile, for BPF with 5-SRRs, the insertion loss reduces to 2.02 dB with return loss <30 dB due to several factors that will be mentioned later.

2. BPF AND SRR

2.1. BPF

The proposed BPF used an open loop ring resonator, designed with total length of L_1 and L_2, which is half wavelength of the guided waves. Bottom silicon substrate loss tangent may cause electric coupling between the metal layer and the bottom loss substrate, which subsequently play down the performance of the microstrip line components at higher-frequency ranges. To avoid this phenomenon, bottom metal layer (M1) is used to construct the ground shield layer. Furthermore, the patterned ground