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A highisolation switch based on a standard GaAs process

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completed from a receiver and transmitter using the precreation of a plane reflection IVS.

3. ACCELERATION EFFECT

Runtime tests between general tree construction (GTC) that is dependent on the emitting source and child node construction (CNC) independent of the emitting source are performed for the ray tracing technique. The simulation equipment included a laptop computer with a Pentium IV 1.2 GHz single-core CPU. A ray path searching technique using the image-based viewing volume ray tube in Ref. 5 was used for the acceleration test. Except for diffraction, five reflections and one transmission order used for finding the ray path are defined. A comparison test shows that the CNC method improves the processing time by 50% compared to the simple GTC method shown in Figure 3.

4. RAY TRACING ACCURACY

With regard to 60 GHz channel measurements and ray tracing simulation evaluations, a modular measurement setup was built up. The setup consists of a transmitter, receiver, and vector network analyzer. The transmitter is composed of a millimeter transmitter horn antenna with an omni-directional, high-power amplifier (HPA) module and up-converter module. The receiver is composed of a millimeter receiver horn antenna with a 12° beamwidth, low-noise amplifier (LNA), and down-converter module [5]. We performed measurements in an office room of a commercial building. The office room is illustrated in Figure 4. The room size is 13.0 m in length, 8.6 m in width, and 2.7 m in height. A partition wall was installed in front of the transmitter antenna for non-line-of-sight (NLOS) measurement. The room included a compartment glass window and two metal doors and was enclosed within concrete walls. The room was not furnished with any equipment, as shown in Figure 4. The location of the transmitter was fixed, whereas the receivers were placed at 4000 different locations 1.8 to 9.8 m away with a 2 mm increment between each location from the transmitter starting point. The receiver location is required for measuring short term fading. The transmitter and receiver antenna heights used in the measurements were the same at 1.5 m. The accuracy of the indoor ray tracing simulation results takes into account the specific structural environment of the site and its electric parameters such as the permittivity of the walls and other objects. For an accurate evaluation, the measurement and prediction results of the provided ray tracing model are compared. The results include the received signal level in dBm according to the separation distance between the transmitter and receiver, as shown in Figure 5. Finally, the measurement results based on the distance between the transmitter and receiver are in slight agreement with the prediction results at the 60 GHz band.

5. CONCLUSIONS

This letter described an advanced acceleration technique for an optimization of accurate prediction software. For validation of the ray tracing model including the acceleration technique, the prediction and measurement results using the given ray tracing model were compared. The ray tracing prediction results showed reasonable agreement with our measurement results. Finally, the given acceleration technique speeds up the computation time of prediction software while maintaining accuracy.

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A HIGH-ISOLATION SWITCH BASED ON A STANDARD GaAs PROCESS

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ABSTRACT: *The design and evaluation of an ultra-wideband nonreflective single port single throw switch integrated circuit is described. The switch has a measured insertion loss of <1.2 dB and isolation of typically better than 70 dB from DC to 10 GHz. The developed circuit is intended for implementation in ultra-wideband microwave instruments and systems requiring high level of isolation.* © 2011 Wiley Periodicals, Inc. Microwave Opt Technol Lett 53:984–987, 2011; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.25906

1. INTRODUCTION

The effective way to improve the characteristics of a solid state switch, and in particular, its isolation is to tweak the technological process. Recently, several techniques have been proposed to optimize the technology for switching applications [1–6]. Most of those attempts focus on reducing parasitic elements of the transistor such as the drain-to-source capacitance and resistance. Often, such a technology optimization requires introducing additional process steps [2] and supplementary expenses. This option is not always available for the circuit designer, especially, if one has to use external fabrication capabilities. The commercially available foundry services provide very limited or often no access to the parameters of the technological process. It means that the integrated circuit developer have to rely on a circuit design using a standard technology.

Another problem arises when trying to integrate a microwave system on a single chip. The technological process, which has been optimized for switching circuits, often exhibits a degradation of other parameters, which are important for realization of the accompanying circuits. For example, gain and efficiency of the amplifier realized on such a process is lower when
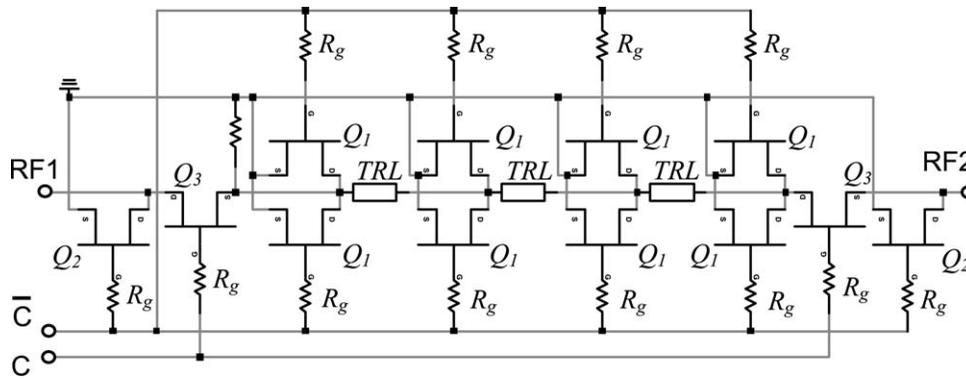
Figure 1 Circuit of the nonreflective SPST switch with symmetric shunt transistors. Q_1 4 × 50 μm; Q_2 2 × 20 μm; Q_3 20 × 45 μm; R_g = 4 kOhm

comparison with the standard process realization [4]. This problem might prevent realization of a complete system on a chip, which usually contains various circuits such as switches, amplifiers, mixers, oscillators, and so on.

This article outlines the applicability of standard monolithic microwave integrated circuit (MMIC) processes for realization of high performance switches. The fundamental tradeoffs between various requirements to be fulfilled in the design of an ultra-wideband switch are discussed. The strategies to overcome these limitations are indicated and demonstrated through a design example of a single port single throw (SPST) nonreflective switch based on a 0.18-μm GaAs pHEMT process [7].

2. DESIGN

The behavior of a transistor as a switch is well known and explicitly described in Refs. 8 and 9. At the drain-to-source voltage (Vds) equal to 0 V, the gate-to-source voltage (Vgs) defines the device impedance. The radio frequency (RF) signal path is drain to source and the gate is the control terminal. With enhancement mode transistors, such as those used in this design, Vgs = 0 V results in a high resistance signal path, and the transistor is off. For Vgs above the threshold voltage (Vt), the transistor has a low resistance signal path and the transistor is on. The use of enhancement rather than depletion mode transistors also allows to avoid a negative bias voltage.

The circuit topology that uses enhancement mode pHEMTs is shown in Figure 1. The circuit is a network with terminals RF1 and RF2 comprising the switch and terminals C and $\overline{C}$, respectively, providing the means of applying the control voltage.

A parasitic drain-to-source capacitance limits the high frequency isolation of the off-state transistor. A distributed topology is adopted to extend the operating frequency band. The shunt mounted transistors Q_1 are connected through the series high-impedance lines TRL, such that the combination of the series high-impedance lines and the shunt transistor off-state drain-to-source capacitance form a 50-Ω artificial transmission line. Thus, this structure has a low insertion loss in the frequency range of operation.

The switch isolation is provided by the on-state shunt transistors at high frequencies. At the same time, the off-state series transistors provide low-frequency isolation.

The control voltages are brought to the devices through 4 kΩ resistors R_g to maintain an RF open circuit at the gates and to provide a good isolation between RF and digital sections of the circuit.

The signals C and $\overline{C}$ control the state of the switch—on or off. The series transistors are controlled with signal $\overline{C}$ and the shunt transistors with signal C. Table 1 shows the complementary switching control of the SPST circuit.

The shunt mounted transistors Q_1 and Q_2 in the off-state are switched on and provide a low impedance path to ground. The corresponding series transistors Q_3 are switched off and at low frequencies they represent high impedance. At higher frequencies, the drain-to-source capacitance diminishes the isolation provided by the transistors. In the off-state of the switch, the devices Q_2 behave as low value resistors. The size of Q_2 is 2 × 20 μm, and it was chosen to provide an input impedance of the switch equal to 50 Ω.

The shunt mounted transistors Q_1 have a gate periphery of 4 × 50 μm, which gives a good compromise between insertion loss in on state and isolation in off state. Choosing the size of the series transistors (Q_3 in Fig. 1), 20 × 45 μm is a trade-off between better isolation but higher insertion loss (smaller device) or degraded isolation but reduced insertion loss (larger device).

3. REALIZATION AND MEASURED PERFORMANCE

Figure 2 shows the layout of the SPST switch. The chip size is 2 × 1 mm^2 and was not optimized for smallest chip size. The circuit also includes a control voltage driver to transform 0/+5 V to a complimentary control signals given in Table 1.

To further improve the isolation, the following isolation improvement techniques have been implemented: filtering of control lines, layout according to the proximity requirement, and implementation of the coplanar waveguide. In addition to that, the symmetric shunt transistors technique [10] has been realized. This technique refers to transistors Q_1. The use of a topology with one transistor to ground on each side of the RF transmission line provides higher isolation than the conventional switch design using a single transistor to ground on one side of the RF line. The simulated and measured performance of the complete SPST switch is shown in Figures 3 and 4. The simulation setup includes 500 μm long bonding wires. The measured on-wafer insertion loss is <1.2 dB to 10 GHz. The isolation is typically

TABLE 1 Truth Table for the SPST Switch

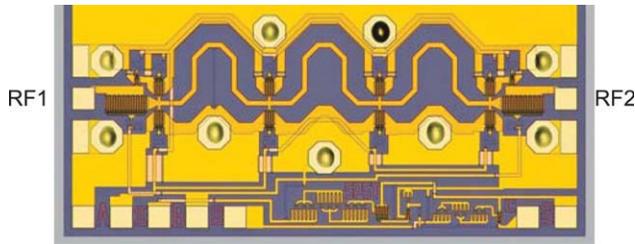| Control Input		Signal Path State
C	$\overline{C}$	RF1 to RF2
2 V	0 V	On
0 V	2 V	Off

Figure 2 Photograph of the SPST switch integrated circuit. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]
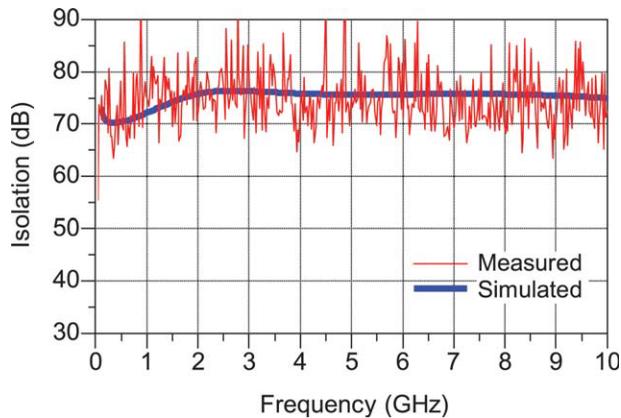

Figure 3 Simulated and measured isolation of the switch. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

better than 70 dB to 10 GHz. Unfortunately, the measured isolation is affected by the dynamic range of the measurement setup and is drowned in the noise floor, as it can be observed in Figure 3.

As to the switch power performance, the 1 dB compression point of the insertion loss is at 12 dBm input power, whereas the isolation degrades by 5 dB. The input-referred third-order intercept point is estimated to be 31 dBm.

The measured matching characteristics of the switch are shown in Figure 5. The magnitude of S_{11} is below -16 dB in on-state and -9 dB in off-state to 8 GHz. The matching of the
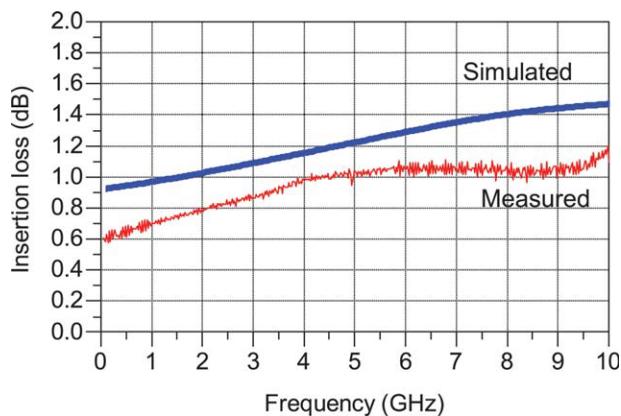

Figure 4 Simulated and measured insertion loss of the switch. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]
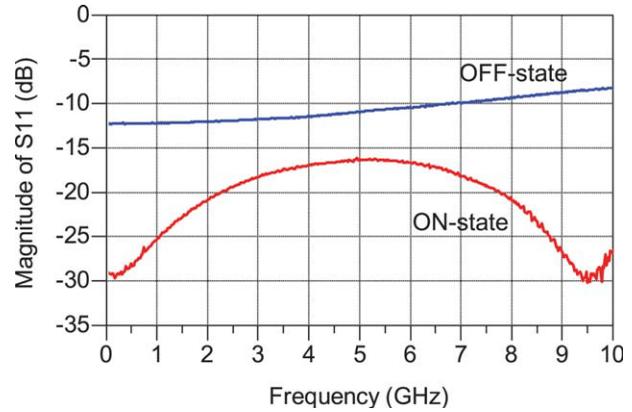

Figure 5 Measured magnitude of S_{11}. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

nonreflective switch in off-state can be considerably improved by adjusting the size of the transistors Q_2 (refer to Fig. 1) and taking into account the corresponding package type of the MMIC in case of packaging in the future.

4. CONCLUSION

The distributed topology allows for a low loss and high isolation in a switch circuit based on a standard MMIC processing. Such a topology provides an improved electrical performance in comparison with the standard series/shunt topology that, however, leads to a large chip size because of the nature of the distributed structures. The larger chip size also contributes to a better isolation, whereas circuits with small area prone to parasitic coupling between the input and output ports, particularly at high frequencies.

The parasitic drain-to-source capacitance of the shunt transistors in off-state can be effectively compensated by series inductors. The insertion loss of the overall switch circuit is sensitive to the quality factor of these inductors. For that reason, in the present realization, the inductors are realized in a form of high impedance transmission lines, although they occupy more space than the conventional planar inductors. The number of Q_1/TRL sections (refer to Fig. 1) is dictated by a trade-off between the bandwidth and insertion loss. More sections allow for a wider bandwidth but result in a higher insertion loss because each section introduces a certain amount of signal attenuation.

Matching of the switch in off-state can be realized using a single transistor, as it was done in this design (Q_2 in Fig. 1), or using a large transistor in series with a resistor. The second configuration usually provides a better reliability and stability of matching characteristics, but it also requires a larger chip area.

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RECTANGULAR SLOT ANTENNA DESIGN WITH TWO L-SHAPED SLITS FOR WLAN/ WIMAX APPLICATIONS

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ABSTRACT: *A novel coplanar rectangular slot antenna with dual band operation is proposed. By loading two dissimilar inverted L-shaped slit into the rectangular radiating element, broad impedance bandwidth at both lower and upper operating bands are achieved to allow the operation for 2.4/5.2/5.8 GHz wireless local area network and 2.6/3.5/5.5 GHz worldwide interoperability for microwave access bands. The design evolution of this proposed antenna by simulation is clearly demonstrated, and a prototype was fabricated and experimentally investigated. © 2011 Wiley Periodicals, Inc. Microwave Opt Technol Lett 53:987–991, 2011; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.25936*

1. INTRODUCTION

Amid different types of antenna designs for wide or broad band operation, the slot antenna design is one of the favorite candidates since it possesses the advantages such as simple structure, wide impedance bandwidth, and good bidirectional radiation characteristic [1–3]. Presently, the most employed feeding technique for slot antenna designated for wireless local area network (WLAN) operation is microstrip-fed [4] and coplanar waveguide
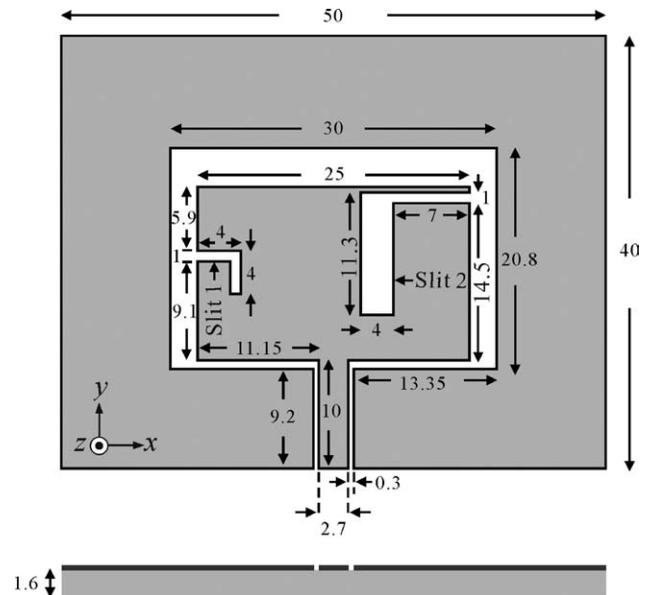

Figure 1 Geometry and dimensions of the proposed antenna (dimensions in mm)

(CPW)-fed [5]. As the CPW-fed slot antenna is generally easy to fabricate and exhibits wider impedance bandwidth than its microstrip-fed counterpart, such design is widely discussed in the antenna community [5]. In the past decade, many CPW-fed slot antennas with dissimilar shapes and sizes can be found in the open-literature [1–8], and among them, the rectangular (or square) slot shape is commonly used for broadband [1] or UWB [6–8] design.

In recent years, the increasing popularity in worldwide interoperability for microwave access (WiMAX) communication system has led to the design of slot antenna specifically catered only for WiMAX operation [9]. Furthermore, because of the rapid development in both WLAN and WiMAX wireless communications, the technique of incorporating the WiMAX operating band with the WLAN operating band to create a multiband slot antenna specifically designed for these applications are presently the most widely discussed topics [10, 11]. However, to achieve sufficient impedance bandwidth, complicating solution such as the fractal slot antenna design [10] or compelled to insert parasitic elements to the radiating element [11] are proposed.

Therefore, in this article, a CPW-fed rectangular slot antenna with simple configuration that excites two resonant modes at around 3.33 and 5.05 GHz is initially proposed. To enable both lower and upper operating bands to conform to the 10-dB impedance bandwidth specifications for WLAN and WiMAX operations, two dissimilar inverted L-shaped slits are loaded into both sides of the rectangular radiating element to create three additional resonant modes at around 2.13, 2.66, and 5.7 GHz, which results in exhibiting a lower and upper operating band that measured between 2.05 to 3.86 GHz and 4.38 to 5.88 GHz, respectively, along 2:1 voltage standing wave ratio (VSWR). Prototype of the proposed antenna with good performances over the dual operating bands was constructed and compared with the simulated data. The design flow of this proposed antenna via simulation and typical experimental results are demonstrated and discussed.

2. THE ANTENNA STRUCTURES

The geometry and dimensions of the proposed CPW antenna is presented in Figure 1. The coplanar ground plane with