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Keywords

«very high frequency power converter», «resonant converter», «zero voltage switching», «interleaved converters», «self-oscillating»

Abstract

This paper describes analysis and design procedure of an interleaved, self-oscillating resonant SEPIC converter, suitable for operation at very high frequencies (VHF) ranging from 30 MHz to 300 MHz. The presented circuit consists of two resonant SEPIC DC-DC converters, and a capacitive interconnection network between the switches which provides self-oscillating and interleaved operation. A design approach to ensure zero voltage switching (ZVS) condition of the MOSFET devices is provided.
To verify the proposed method, an 11 W, 50 MHz prototype was built using low-cost VDMOS devices and experimental results are presented. Peak achieved efficiency was 87%.

Introduction

A constant drive for miniaturization of power converters inevitably leads to increase of converter switching frequency. Reactive components scale down in both physical size and value, which permits use of power converters in applications with severe size constraints. This is especially beneficial regarding magnetic components, as they are typically the biggest contributors to the size of power converters. Inductance values required for operation at very high frequencies could easily be achieved with air core inductors, eliminating core loss entirely. For operation above 30 MHz, requirements for EMI filtering are significantly relaxed: EMI filters could be reduced to a few SMD components, or removed completely from a design. For some applications, for example LED drives, it is also beneficial if the power converter does not require electrolytic capacitors for voltage/current filtering, as they might limit the lifetime of LED lamps.

High switching frequencies impose new design challenges as well. With exception of very low power and voltage levels, hard-switched converters are unsuitable for operation at frequencies above a few MHz due to prohibitively large switching losses [1]. Generating signals for high-side switches is very difficult [2], which further limits topology selection, except in low-voltage converters [3]. Losses are further increased if hard gating is employed, which is exclusively the case for commercial DC-DC converters today.

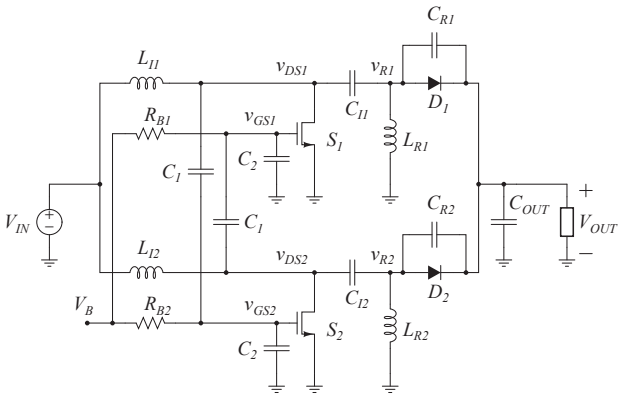

Fig. 1: Schematic of the interleaved, self-oscillating resonant SEPIC converter.

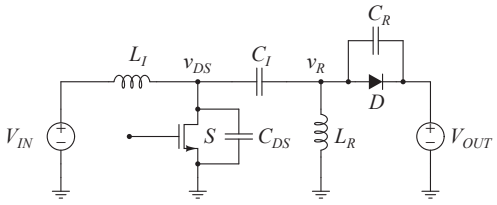

Fig. 2: Resonant SEPIC converter topology.

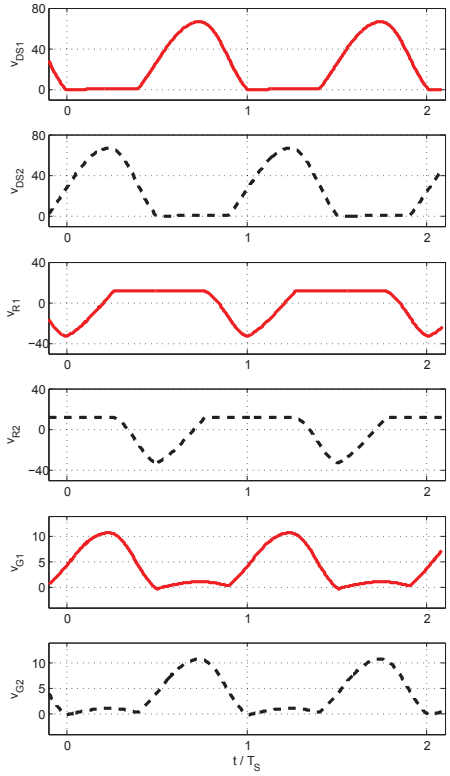

Fig. 3: Simulated waveforms of the drain, rectifier, and gate voltages of the interleaved self-oscillating resonant SEPIC converter; $V_{IN} = 24$ V and $V_{OUT} = 12$ V.

To work around these problems, resonant converter topologies need to be considered in order to minimize or eliminate some of the switching loss mechanisms. Resonant [4–6] or multiresonant [1, 7] gate driving techniques need to be employed as well, thereby reducing the gating loss by recovering portion of the energy from the gate capacitances. Since there are no gate driver solutions intended for operation above 30 MHz currently available on the market, gate drivers for VHF converters are typically developed using discrete components.

This paper presents a recently developed technique to achieve interleaved, self-oscillating operation of two resonant converters, suitable for power conversion at frequencies in VHF (30 MHz - 300 MHz) range, and a design procedure for a step-down resonant SEPIC converter utilizing aforementioned technique. A general structure of the proposed converter, as well as the interconnection network which provides self-oscillating behavior and interleaved operation, are described. Design procedure for the proposed converter is provided. Finally, experimental results of an 11 W, 50 MHz prototype are presented.

Proposed Converter

Fig. 1 shows the proposed converter topology. Two resonant SEPIC converters [7], as shown in Fig. 2, are coupled via capacitive interconnection network, which provides gate signal generation for driving the MOSFET devices. The circuit is symmetrical, and the gate voltages are in phase with the drain voltages of opposing MOSFETs due to capacitive voltage dividers; thus providing interleaved operation. Typical voltage waveforms of the interleaved resonant SEPIC converter are shown in Fig. 3.

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This section is organized as follows:

- topology and properties of the resonant SEPIC converter
- the interleaved converter topology
- the interconnection gate drive network
- converter startup

Resonant SEPIC Converter

Compared to the class E converter [4, 8], which has bulky input and output inductances, in resonant SEPIC converter topology all reactive components are part of the resonant tank and therefore are small in value. Furthermore, fewer inductors are necessary, as well as lower component count in general [**?**]. This is particularly important if we have in mind that at RF frequencies inductors typically have low Q factors due to skin and proximity effects, which increase conduction losses.

Due to presence of 5 resonant elements and 2 switching devices, even with ideal components the circuit in Fig. 2 is very difficult to describe analytically [7]. The situation is complicated even further due to nonlinearity of the parasitic capacitances of the semiconductor devices. To accurately predict the behavior of the circuit, a simulation program and precise component models are required.

It was observed that not all reactive elements are necessary for the correct circuit operation, although they will certainly appear in a physical prototype. The absolute minimum requirements are two inductors and two capacitors, either C_{DS} and C_I, or C_R and C_I. In Fig. 4 the 4-element resonant network seen from the drain terminal is shown, as well as two 3-element simplified networks; note that L_I is excluded since it remains the same in all three configurations. With the appropriate components choice, these networks may have exactly the same input impedance at all frequencies, which is the impedance seen by the drain terminals of the MOSFETs. Therefore, in the design process of the proposed interleaved converter, one of the 3-element networks can be used instead, thus reducing the number of unknowns in the design by one. The transformation between the networks in Fig. 4 is given in Table I. Capacitances and inductances are normalized with respect to $C_{I,1}$ and $L_{R,1}$. n and k are the capacitance ratios $C_{DS,1}/C_{I,1}$ and $C_{DS}/C_{I,1}$, respectively. Note that k must always be less than or equal to n. This transformation affects the output impedance of the network, which means that the output voltage and current have to be scaled as well in order to obtain identical circuit behavior. For example, if the 3-element network 1 is transformed into the 3-element network 2, output impedance is scaled down by a factor of $(1+n)^2$; equivalently, the output current is increased $1+n$ times, and the output voltage is decreased by the same factor.

Interleaved Resonant SEPIC Converter

In the case of the proposed converter from Fig. 1, it was found that the resonant/switching frequency may be approximately determined from:

$$f_S \approx \frac{1}{2\pi\sqrt{L_I(C_I + C_{DS,eq})}} \tag{1}$$

Capacitance $C_{DS,eq}$ is defined as the equivalent drain to source capacitance:

$$C_{DS,eq} = C_{OSS} + \frac{C_1(C_2 + C_{ISS})}{C_1 + C_2 + C_{ISS}} \tag{2}$$

The exact value of f_S also depends on duty cycle of the switch and the diode, which are not easy to predict - especially if nonlinear capacitances of the semiconductor components are taken into account. Nonetheless, equation (1) is a good starting point for the design procedure; reactive elements could be scaled up or down in order to adjust for desired output power or frequency. For example, increase in circuit capacitances N times would result with a converter with $\sqrt{N}$ lower switching frequency and $\sqrt{N}$ higher power output. If capacitances are scaled up and inductances are scaled down by the same factor,

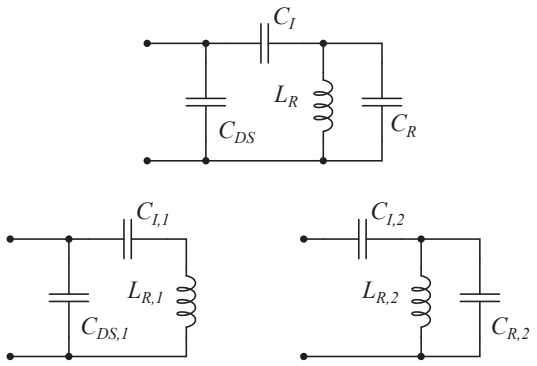

Fig. 4: Resonant network seen by the drain terminal of the MOSFETs, with the exclusion of the input inductor L_I; original (top) and two alternatives (bottom). The components of these networks may be chosen in such a way that all three circuits have the same input impedance.

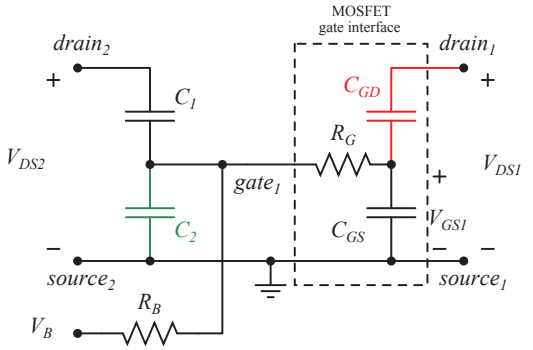

Fig. 5: A part of the interconnection network used with the resonant SEPIC converter to obtain the self-oscillating and interleaved operation. Voltage divider formed by C_1, C_{GS}, and C_2 (optional), determines the amplitude of the gate voltage. Note the parasitic feedback from the drain of the same MOSFET. Bias voltage for the gate terminal is provided through resistor R_B.

Table I: Network transformations.

	C_I	C_{DS}	C_R	L_I
original	$(1+n-k)\,C$	$k\,C$	$(1+n-k)\,(n-k)\,C$	$L/(1+n-k)^2$
alternative (1)	C	$n\,C$	—	L
alternative (2)	$(1+n)\,C$	—	$n\,(1+n)\,C$	$L/(1+n)^2$

the switching frequency would remain the same and the power output would increase N times.

As it was observed in [7], the waveforms do not deviate significantly with change of voltage transformation ratio M, and this also holds true for the interleaved self-oscillating SEPIC converter. This property is very useful, since it allows easy change of specifications with only minor adjustments to the converter components.

Interconnection Network

Several gate drive techniques are described in the literature, and in that sense RF DC-DC converters may be separated into two major groups: oscillator-driven [1,2,5,7] and self-oscillating converters [4,6].

The interconnection network from the drain of S_2 to the gate of S_1 is shown in Fig. 5. C_1 and C_2, together with the gate capacitance of the MOSFET C_{GS}, form a capacitive voltage divider, thus generating the signal for driving the other switch.
Gate resistors R_{B1} and R_{B2} provide biasing for the MOSFET gates. During the converter startup, R_{B1} and R_{B2} form $R-C$ time constants with the gate capacitances of S_1 and S_2. In order to reduce the startup time, these time constants should be different, or alternatively, independent bias voltages should be used.

If resistance R_G is small compared to impedance of the MOSFET input capacitance C_{ISS} (which is usually the case), then the gate voltage v_{GS} is approximately given as:

$$v_{GS}(t) = \frac{C_1}{C_1+C_2+C_{GD}+C_{GS}}\,v_{DS,AC}(t) + \frac{C_{GD}}{C_1+C_2+C_{GD}+C_{GS}}\,v_{DS,AC}(t) + V_B \qquad (3)$$

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The first term in (3) represents feedback from the drain voltage of the opposing MOSFET. The second term is due to parasitic capacitance C_{GD} and is undesirable. The operation point of the switch in the OFF-state might shift into the saturation region and produce significant losses, which also shortens the switch lifetime or, in more severe cases, the switching device may be destroyed. Therefore, it is recommended to use switches with small C_{GD} capacitance in the design, and the feedback network needs to provide enough gain in the primary feedback. This is done by appropriate sizing of C_1 and C_2. Additional benefit of having nonzero C_2 in the circuit which helps suppressing parasitic high frequency oscillations on the gate, which may appear due to stray inductances in the circuit. However, increase of C_1 and C_2 is limited by ZVS condition. C_I needs to be at least two times larger than $C_{DS,eq}$ in order to achieve ZVS operation.

There are some drawbacks to this technique. In order to obtain circuit symmetry at VHF frequencies, layout needs to be symmetrical and the circuit components should have low tolerances. Since there is a purely capacitive signal path from drain to gate terminals, any parasitic inductance in the circuit might introduce ringing in the gate voltage waveforms. As well as in [6], this self-oscillating scheme shows lower dependency of output power with the bias voltage compared to [9]. Therefore it is reasonable to consider burst-mode control scheme [1, 5, 7, 10] for the proposed converter, which is a subject of further research.

Converter Startup

Start-up of the circuit is achieved by setting the gate bias voltage slightly above the MOSFET threshold voltage, so the switching devices enter saturation mode. A simplified AC equivalent of the inverter side is shown in Fig. 6. The MOSFETs are modeled as voltage controlled current sources.

The loop formed by the MOSFETs and the capacitive voltage dividers is unstable; hence, amplitudes of the drain (and consequently, gate) voltages increase. This increase is bounded by the fact that the MOSFETs eventually start entering the ohmic region, thus limiting the effective gain in the loop. In the steady state, the MOSFETs do not enter saturation region.

Typical startup gate and drain waveforms are shown in Fig. 7, as a response to a step change in V_B at $t = 0.2$ µs. Until the oscillations start, the response of the gate voltages is described completely by time constant τ_G defined as

$$\tau_G = R_B(C_{ISS} + C_{DG} + C_1 + C_2) \tag{4}$$

and ends when the MOSFETs enter saturation. For the circuit in Fig. 6 to be unstable, the following condition has to be satisfied:

$$g_m \, Q \, Z_0 > \frac{1}{x} \tag{5}$$

where Q is the Q-factor of the resonant tank, Z_0 is the reactance of the inductors/capacitors at the resonant frequency, g_m is the MOSFET transconductance, and x is the scaling factor of the capacitive voltage divider in (3). For a given switching frequency and power level, g_m, Q, and Z_0 should be maximized in order to minimize the transient time.

Design Procedure

A method was proposed in [7] which relies on separate design of the inverter and rectifier stages. However, that procedure has been found unsuitable for the self-oscillating interleaved converter design. As it was discussed in the previous section, it is very difficult to determine the switching frequency a priori due to complexity of circuit operation. More importantly, it is not guaranteed that a converter designed to operate at a certain frequency might not operate at that particular frequency when used in the interleaved

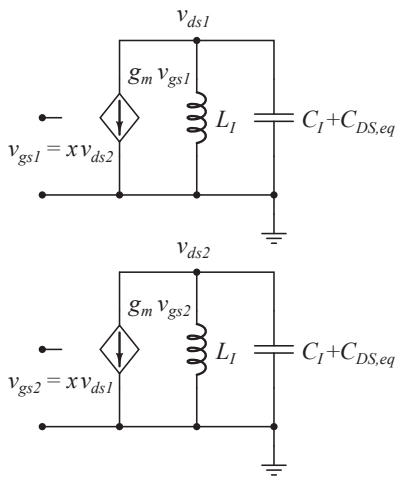

Fig. 6: Simplified AC equivalent circuit of the inverter stages during startup process. The MOSFETs, while in saturation, are modeled as voltage controlled current sources.

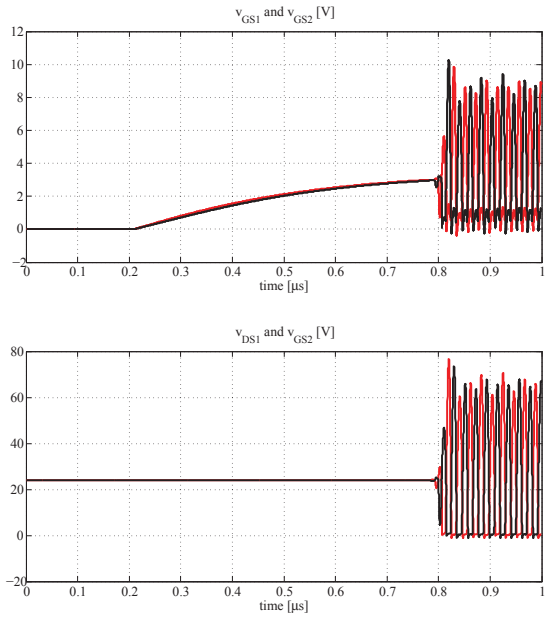

Fig. 7: Gate (top) and drain (bottom) waveforms during the converter startup.

design. Therefore, a direct synthesis method is proposed in this section.

The design procedure starts from specifications for output power P_{OUT}, switching frequency f_S, and input voltage V_{IN}. Required component values will be finally determined from the output power P_{OUT} specification by scaling of the reactive components. At this stage of the design process, initial values for C_R and L_R are $C_R = 0$ and $L_R = 1.5L_I$.

Capacitance C_1 is directly determined from (3):

$$C_1 = (C_2 + C_{GS} + C_{GD}) \frac{V_{GS,max}}{V_{DS,max} - V_{GS,max}} \tag{6}$$

where C_2 may be chosen arbitrarily as long as it does not yield high capacitance value for C_1. For low voltage applications or when the C_{GS} is large, C_2 may be omitted. The ratio between the SEPIC "flying" capacitance C_I and equivalent drain to source capacitance $C_{DS,eq}$ is a limiting factor for ZVS operation; a good initial value for C_I was found to be at least 2-3 $C_{DS,eq}$. The transformation provided in Table I should be applied to include C_R in the final design. After C_I is selected, input inductance L_I is determined from (1):

$$L_I = \frac{1}{(2\pi f_S)^2} \frac{1}{C_I + C_{DS,eq}} \tag{7}$$

Inductor L_R is then adjusted as necessary to reach ZVS operation. Impedance scaling is then applied to obtain desired frequency and output power.

The peak drain voltage $V_{DS,max}$ is expected to be around 3 times higher compared to V_{IN}. Therefore, the MOSFET has to be chosen with a voltage rating higher than $V_{DS,max}$.

Nonlinearities of the parasitic capacitances may influence the final result, and for that reason accurate modeling is beneficial. Nevertheless, even with the simple models of the transistors and diodes reasonable accuracy is obtainable.

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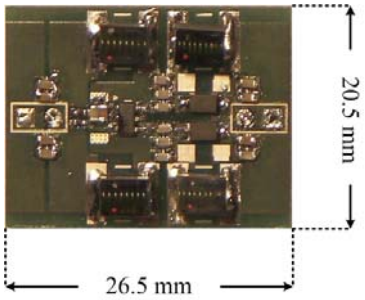


Fig. 8: Experimental DC-DC converter.

Table II: Converter component values.

Component	Value
L_I	Coilcraft air-core 82 nH
L_R	Coilcraft air-core 120 nH
C_1	C0G 13 pF
C_2	-
C_I	C0G 80 pF
$C_{S,EXT}$	-
C_{IN}	C0G 8 uF
C_{OUT}	C0G 8 uF
S	Fairchild FDC8602
D	NXP PMEG6010

Experimental Results

Experimental setup was built to verify the proposed design procedure (see Fig. 8). The DC-DC converter specifications are as follows:

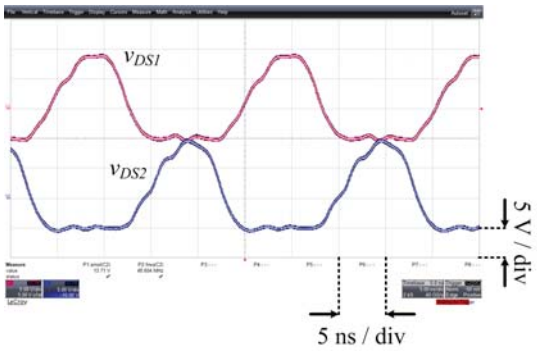
- input voltage $V_{IN} = 24$ V
- output voltage $V_{OUT} = 11$ V
- output current $I_{OUT} = 1$ A
- switching frequency $f_S = 50$ MHz

A complete list of components used is presented in Table II.

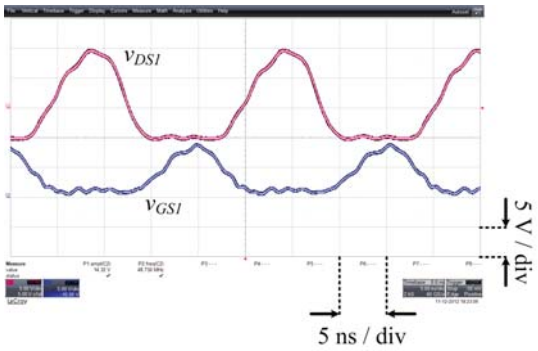
The MOSFET device to be used in the design needs to be able to withstand at least 3 times the input voltage. Therefore, 100 V rated devices were considered, and FDC8602 dual MOSFET from Fairchild Semiconductor was chosen since it offered a good balance between $R_{DS,on}$ and parasitic capacitances C_{ISS} and C_{OSS}. On the other hand, the downsides are the presence of the stray inductance and high thermal resistance of the package. Experimental voltage waveforms of the designed converter are provided in Fig. 9. Note the high-frequency ringing due to finitely small inductances of the component packages and PCB traces.

The circuit shows little tolerance to non-symmetry, therefore direct measurements with a 9.5 pF oscilloscope probe would disturb the operation of the converter, especially of v_D and v_R nodes. The measurements of these nodes were obtained through 2.7 pF capacitance instead (see Fig. 10), which gives the scaling factor of 0.22 and removes the DC component from the waveform. With input voltage of 24 V, expected peak voltage across the MOSFETs should be around 72 V. In Fig. 9a, peak-to-peak v_{DS} voltages are 15 V. This gives $V_{DS,max}$ of 68 V which matches well with expectations.

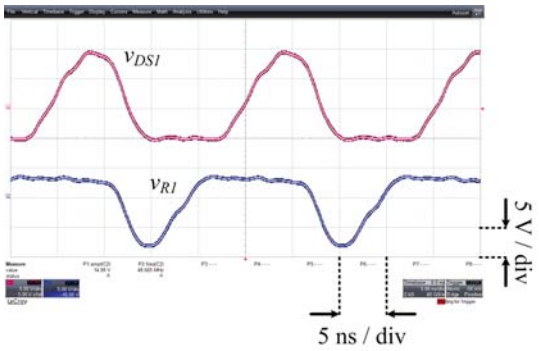
v_{GS} was designed to have 10 V peak-to-peak value. In Fig. 9b the direct measurement is provided, and it can be observed that the amplitude is close to 8 V, indicating the influence of the probe capacitance. Measured switching frequency was 48.7 MHz when the probe was connected to the board via 2.7 pF capacitor. The frequency is 5 % off the target value, which is accredited mainly to the simplicity of the model and equation (1).



(a) Drain voltages $v_{DS1}(t)$ and $v_{DS2}(t)$



(b) Drain and gate voltages $v_{DS1}(t)$ and $v_{GS1}(t)$



(c) Drain and rectifier voltages $v_{DS1}(t)$ and $v_{R1}(t)$

Fig. 9: Experimental waveforms of the prototype converter.

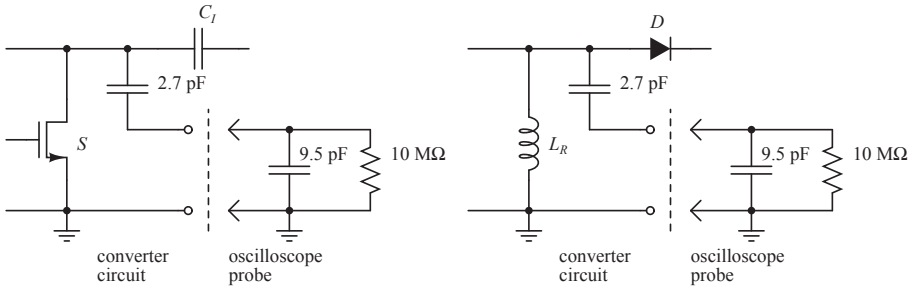


Fig. 10: Measurement setup for drain (left) and rectifier (right) voltages.

Conclusion and Future Work

This paper presents a gate driving scheme which provides self-oscillating and interleaved operation of two resonant SEPIC converters. The only components of the gate drive which do not belong to the converter topology are two capacitors and two biasing resistors. These components are typically small in size, which makes this gate drive method very component and space efficient. A design procedure for the interleaved SEPIC converter has been proposed, and experimental results have verified its effectiveness. A 50-MHz, 11 W converter has been designed and implemented, using only low-cost diodes and VDMOS switches. The peak achieved efficiency was 87%.

The circuit layout needs to be as symmetrical as possible in order to achieve optimal operation. Output power is not significantly influenced by variation of the gate bias voltage. As part of the ongoing re-

search, implementation of the burst-mode control with this gate driving technique will be investigated, for which this gate drive technique shows promising results.

As this paper has demonstrated, it is possible to obtain acceptable efficiency, small converter size, and low cost in VHF power conversion.

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