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Low Power Very High Frequency Resonant Converter with High Step Down Ratio

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Abstract—**This paper presents the design of a resonant converter with a switching frequency in the very high frequency range (30-300MHz), a large step down ratio and low output power. This gives the designed converters specifications which are far from previous results. The class E inverter and rectifier have been selected for the prototype and the circuits are analyzed and simulated. Three different power stages are implemented based on different design parameters. The first prototype is with a switch with small capacitances, the second one is with a switch with low on resistance and the last one is with a large input inductor. The power stages are designed with the same specs and efficiencies from $60.7 - 82.9\%$ are achieved.**

I. INTRODUCTION

When designing power converters it is always a goal to reduce the price and the physical size, i.e. increase the power density. The development of Switch Mode Power Supplies (SMPS) has made it possible to increase the power density significantly, but it is limited by the size of the passive energy storing components (inductors and capacitors). The value and size of these is however dependent on the switching frequency. By increasing the switching frequency it will hence be possible to reduce the size of SMPSs further.

Traditional SMPS topologies like Buck and Boost are hard switching, this means the MOSFET is switching while energy is stored in the output capacitance. The result is that energy is dissipated in the MOSFET every time it turns on. Although this introduces losses in the converter, it is not critical for converters switching at $50 - 400kHz$. But when the frequency is increased to the Very High Frequency (VHF) range $(30 - 300MHz)$ the dissipated power get almost 1000 times larger. This amount of energy would ruin the efficiency and require extreme cooling of the MOSFET. This leads to the development of resonant converters.

In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. For the last two decades (since 1988 [1]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for DC/DC converters. With this type of converters it is possible to achieve Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS). In this case the MOSFET turns on when the voltage and/or current across/through it is zero. Theoretically this should eliminate switching losses if the switching is done instantaneously and at exactly the right time. This is not practically achievable, but even with slight deviations from the ideal case very high efficiencies can be achieved.

Increasing the switching frequency has several benefits beside reducing the size. As already mentioned the size of the passive components depends on the switching frequency. This gives a reduction in size, but also in cost as smaller components are generally cheaper. If the frequency is increased enough, some of the components can even be left out as they can be constituted by the parasitic parts of other components (this will be explained further in section II and III). An increase in switching frequency will also make it easier to comply with EMI requirements, as switching harmonics can easily be filtered out by small and cheap filters.

With a switching frequency in the VHF range, it will also be possible to achieve very fast responses. However in order to fully benefit from this, an efficient and fast control loop has to be implemented. This still seems to be a big challenge as some of the best results are still achieved using burst mode (or cell modulation) as in [2], [3]. Due to the high switching frequency the converter will reach steady state after just a few μs, this makes it possible to use an array of small converters and switch them on and off as needed. In this way each converter is designed to operate with a defined load/output. This makes the design much easier as resonant inverters are generally very load depended.

The fact that resonant inverters are load depended, makes it very hard to achieve good performance at varying loads. Furthermore resonant inverters need a large load impedance to operate in the ideal situation (having both ZVS and ZCS). This makes them well suited for boost type converters, but making a buck type is a bit more challenging. The most commonly used way to overcome this challenge is to add an autotransformer at the output, in that way the load impedance seen by the inverter is increased [2], [4], [5]. Another way to achieve low output voltage is to use an array of converters with the input in series and the output in parallel as in [6].

The most commonly used inverter is the class E, however several other topologies exist. Some of the research results are summed up in table I. From the table it is seen that very high efficiencies are achievable for the inverters, up to 97%. However for the complete converters the efficiency drops around 10%, with a maximum at 91%.

From table I it is also seen that the converters have limited

Inverters						
Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class DE	5.3	330	N/A	1154	89	1999 [7]
Class E	1	128	N/A	366	96.6	2006 [8]
Class ϕ_2	1	129	N/A	526	97.1	2006 [8]
Class ϕ_2	30	160	N/A	330	93.7	2007 [9]
Class E	1	129	N/A	322.7	97	2007 [10]
Class E	100	9	N/A	6.8	82	2011 [11]

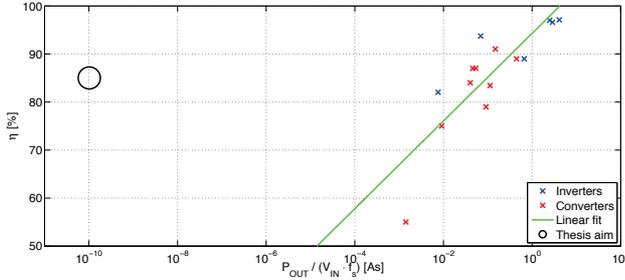| Converters						
Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class E	1	20	25	8.9	89	1989 [12]
Class ϕ_2	30	165	33	265	87	2006 [2]
Class E	100	11	12	10	75	2006 [13]
Class ϕ_2	30	150	33	180	84	2008 [4]
Class ϕ_2	10	170	75	250	91	2009 [5]
Class ϕ_2	30	165	33	225	87	2009 [5]
Class ϕ_2	30	330	50	900	79	2009 [6]
Class E	100	12	23.7	1.7	55	2010 [14]
Push-Pull ϕ_2	30	140	65.4	471.9	83.4	2010 [15]

Fig. 1. Relation between $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$ and η.

gains, with a step down of 6.6 times and an step up of 2 being the largest. As already stated the large reductions are not produced solely by the converter, but with different ways to make the load impedance appear larger. By further inspection a connection between $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$ and η can be seen, this relation is shown in figure 1. It seems that it is problematic to have a high input voltage and switching frequency while having a low output power and still keep the efficiency high.

This paper will cover the design of a VHF power converter with a low voltage and power output. This will require a huge reduction in voltage and a combination of output power, input voltage and switching frequency unlike any of the previous results. This will put the converter in the area marked in figure 1, as it is seen this is very far from the results achieved by previous researchers (the specs for the converter is given in table II).

f_S	V_{IN}	V_{OUT}	P_{OUT}	R_L
$30 - 300MHz$	50V	5V	1W	25Ω

As the load is given it is believed that the first step should be to design the rectifier and then design the inverter for the given input and load. It is also possible to design the inverter to a given load and then use different resistance compression networks to make the impedance of the rectifier match [16], [17], [18]. Though this is a solution often used, it is believed that it will increase the complexity of the converter unnecessarily and possibly reduce the achievable efficiency, size, and price.

Section II will cover the selection and design of a resonant rectifier for the given load and output power level. Then a resonant inverter will be designed for the input voltage and load impedance in section III. Experimental results from three different power stages will be shown in section IV. Finally section V summarises and concludes the paper.

II. RESONANT RECTIFIERS

The purpose of the rectifier is to convert the AC current from the inverter to a DC output. Just as the MOSFET has an output capacitance, the diode has a junction capacitance. In order not to burn this energy in the diode, it is important that the transition is made smoothly, so the capacitance is discharged before the diode turns on.

As stated in section I, it is difficult to achieve high efficiency if the input voltage and switching frequency are high and the output power low. The switching frequency is therefore set to 30MHz for the initial design. If good results are achieved with this frequency, it might be increased further in order to minimize the converter.

Though there are several ways to do this, only the most commonly used class E rectifier will be considered here. The class E rectifier is a rather simple circuit, consisting of a diode, two capacitors, and an inductor as shown in figure 2.
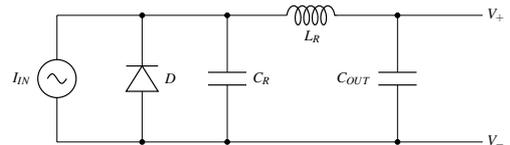

Fig. 2. Schematic of the class E rectifier.

For now it will be assumed that the output capacitance is infinite, so the output voltage is constant, and the diode is assumed to be ideal, i.e. no forward voltage drop, no junction capacitance and no reverse current.

In this case the rectifier will appear resistive at the switching frequency, if the resonance frequency of L_R and C_R are set to this frequency. This will make the design of the inverter a bit simpler, as most design formulas are for a resistive load.

The scaling of the two components will determine the duty cycle of the diode, D_D. As the forward voltage drop of a diode increases with the current running through it, it is desirable to keep D_D as high as possible. However as the diode is connected to the output through an inductor, the average

voltage across it has to be V_{OUT}. Hence a high D_D will lead to a high peak voltage across the diode.

In order to select D_D, and thereby the scaling of the resonating components, the values of real components has to be considered. All the considered inverters has a capacitor at the output insuring a pure AC path, without this there would be a direct DC path from input to output and it would be impossible to reduce the voltage. The average current through the diode, will therefore be the same as the output current.

With the forward voltage drop of a standard schottky diode being around $0.5V$ (10% of the output voltage), it is crucial to use a diode with low forward voltage drop. Fairchilds MBR0520L has one of the lowest forward voltages availible, max $385mV$, and can handle a reverse voltage of $20V$. With this diode, the diode loss will be up to $77mW$ or 7.7% of the output power. This clearly limits the maximum achievable efficiency and fits very well with the $\approx 10\%$ efficiency drop, seen in section I when going from an inverter to a complete converter.

A way to reduce the losses could be to use a synchronous rectifier, this will eliminate the forward voltage loss. This will however require an additional MOSFET, with the following need for gate drive and control.

If $D_D = 0.5\%$ is chosen, the peak diode voltage will be $3.562 \cdot 5V = 17.81V$ leaving a little margin up to the maximum. With this D_D the value of C_R should be $67.5pF$ and the value of L_R should be $417nH$ [19].

The inductor and output capacitor composes a 2nd order lowpass filter. In order to get maximum 1% (or $50mV$) ripple at the output, the 20V AC needs to be attenuated by $52dB$ which leads to a cut of frequency of $1.5MHz$ and a output capacitance of $27nF$.

The inductor has, as expected, a DC current of $0.2A$ (the output current with 1W and 5V) and on top of that an AC current with an amplitude of $120mA$. The DC resistance of the inductor is estimated to $25m\Omega$ and the AC resistance to $330m\Omega$ (these values are based on an air core inductor with a diameter of $6mm$ and 8 turns of $0.4mm$ wire). The loss caused by the inductor can then be calculated to $1mW$ due to DC losses and $2.4mW$ due to AC losses.

This is 0.34% of the output power and these resistances are based on a relatively large air core inductor. The Equivalent Series Resistance (ESR) of ceramic capacitor in the sizes used here, will be less than $200m\Omega$ [20] and the currents running through them are smaller than than the current in the inductor. The loss caused by them will thus not be significant. Furthermore the parasitic capacitance of the diode can account for C_R. Actually the parasitic capacitance of the chosen diode is $65pF$ at $5V$ reverse voltage fitting almost perfectly with the calculated value.

To sum up, the class E rectifier is a simple circuit which can be made of only 3 components. The selection of the diode is crucial in order to get a decent efficiency and even with the best diodes available, the diode losses will be significant. But as long as an inductor with low ESR is chosen, the total loss in the rectifier should be below $100mW$.

III. Resonant inverters

As mentioned in section I, a resonant inverter is used in order to eliminate switching losses. Either ZVS or ZCS can be achieved and in some special cases both. Generally ZVS will eliminate losses due to parasitic capacitances and ZCS will eliminate losses due to parasitic inductance. For MOSFETs and diodes in power applications the capacitances causes the dominating loss, ZVS will therefore be the main criteria.

However in some cases it is, as mentioned, possible to achieve both ZVS and ZCS switching (also called ZVS and zero slope switching, ZDS). If this can be achieved the exact timing of the switching is less important, as the voltage across the MOSFET will be zero for a small amount of time.

If only ZVS can be achieved, the MOSFET needs to turn on, at exactly the point where the voltage across it hits zero. If it switches just a little to early, there will be energy stored in the capacitor causing switching losses. If it switches a little too late, the drain source voltage will go below zero and the body diode will start to conduct which also gives losses.

The most commonly used resonant inverter is the class E, a schematic of it is shown in figure 3. It consists of a single MOSFET, two inductors, and two capacitors. In optimum operation L_{IN} is an infinite choke providing a pure DC input current. The resonant circuit (L_{RC} and C_{RC}) are inductive at the switching frequency and the inverter is designed to have both ZVS and ZDS.
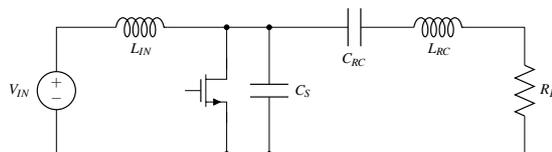

Fig. 3. Schematic of the class E inverter.

As already mentioned ZVS and ZDS switching can only be achieved in very specific situations. According to [22] and [23] this can only be achieved if:

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{V_{IN}^2}{P_{OUT}}$$
$$f_{S,max} = \frac{P_{OUT}}{2 \cdot \pi \cdot C_S \cdot V_{IN}^2} \tag{1}$$

With $50V$ input, $1W$ output, and a switching frequency of $30MHz$, this would require a load impedance of $1.44k\Omega$ and an output capacitance of $2.1pF$. From equation 1 it is seen that there is a special combination of f_S, V_{IN} and P_{OUT} which makes it possible to operate in the optimum situation. Similar equations can be found for other topologies [22] and this is the reason for the dependence seen in figure 1.

A MOSFET with an output capacitance of $2.1pF$ for this voltage level and switching frequency is not available, they have minimum 10 times that. Furthermore the impedance is very far from the input impedance of the rectifier. It will therefore not be possible to achieve both ZVS and ZDS switching. However it is still possible to achieve ZVS and thereby

high efficiency as long as the transitions of the MOSFET is controlled well.

If the drain source voltage of the MOSFET is assumed to be a half sine wave when it is off and zero when it is on, the peak voltage across the MOSFET will be:

$$V_{IN} = \int V_{DS} = V_{DS,peak} \frac{2 \cdot (D-1)}{\pi}$$

$$\Updownarrow$$

$$V_{DS,peak} = V_{IN} \frac{\pi}{2 \cdot (D-1)} \qquad (2)$$

The RMS value of a half wave rectified sine wave is:

$$V_{DS,rms} = V_{DS,peak} \sqrt{\frac{D}{2}} \qquad (3)$$

And the RMS value of the output voltage is:

$$V_{OUT,rms} = \sqrt{P_{OUT} \cdot R_L} \qquad (4)$$

According to [2] the reactance of the resonance circuit can now be determined by:

$$X_{RC} = R_L \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \qquad (5)$$

By combining equation 2, 3, 4, and 5, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = R_L \cdot \sqrt{\frac{V_{IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{OUT} \cdot R_L} - 1} \qquad (6)$$

It is desirable to keep the duty cycle low in order to reduce the peak voltage across the MOSFET. However due to turn on and off times and delays, it is decided to keep it close to 50%. From equation 2 it is found that a duty cycle of 45% will give a peak voltage of $142.8V$, leaving a little headroom if a $150V$ MOSFET is used. Using this value along with the previous results the needed reactance is found to be 326Ω. If a capacitor of $680pF$ is used, the value of the inductor becomes $1.77\mu H$.

The next step is to determine the values of L_{IN} and C_S. In order to minimize losses it is preferable to keep L_{IN} large, thus large AC currents running in and out of the converter and thereby causing unnecessary losses are avoided. If the input choke is assumed infinite, the next step is to calculate the value of C_S. C_S and the resonance circuit should resonate at a frequency with a period of:

$$T_R = 2 \cdot (1-D) \cdot T_S \Leftrightarrow f_R = \frac{f_S}{2 \cdot (1-D)}$$

If the reactance of C_S is the same as the reactance of the resonant tank (with opposite operational sign) at f_R the circuit will resonate at this frequency. However as the capacitor is only used when the MOSFET is off, it has to be scaled by 1-D:

$$C_S = \frac{1-D}{2 \cdot \pi \cdot f_R \cdot X_R} \qquad (7)$$

With the specifications for this converter this would require a MOSFET with an output capacitance of maximum $10.9pF$. At the moment the MOSFETs with lowest output capacitances, C_{OSS}, which are able to switch in the MHz range and handle $150V$, has an output capacitance of $\approx 20pF$ at 50V. It is therefore necessary to reduce the input inductor in order to increase C_S. The effective capacitance of the output capacitor is $\frac{C_S}{1-D} = 36.4pF$, hence the total inductance of the resonance circuit and the input inductor should be $936nH$. Knowing the values of L_{RC} and C_{RC} the input inductance can be calculated to $2.91\mu H$.

From a simulation the RMS current through the inductors and the MOSFET is found to be; $I_{IN,rms} = 102mA$, $I_{FET,rms} = 165mA$ and $I_{OUT,rms} = 208mA$.

If the MOSFET has a $R_{ON,max} = 1.2\Omega$, this will give a conduction loss in the MOSFET of up to 33mW. The AC resistance of the inductors is estimated to $100m\Omega$, thus they will have a combined loss of 5.37mW. As for the rectifiers the losses in the capacitors are assumed to be negligible. Thus the total loss in the class E inverter is estimated to $\approx 38mW$.

The complete circuit with the class E inverter and class E rectifier can be seen in figure 4. With the loss calculated for the two parts the combined efficiency will be 88% excluding gate drive and gateing losses.
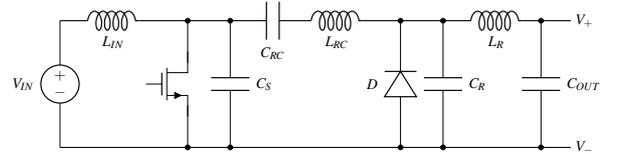

Fig. 4.   Schematic of the class E inverter and class E rectifer.

IV. EXPERIMENTAL RESULTS

In section III the IRF5802 MOSFET were introduced and used for calculations and loss estimates. However several MOSFETs which can be used for this application exist, two of the best suited are compared in table III.

TABLE III
COMPARISON OF MOSFET CHARACTERISTICS
($R_{ds(on)}$ AT $V_{GS} = 10V$ AND CAPACITANCES AT $V_{DS} = 50V$).

Component	V_{DSS}	I_D	$R_{DS(on)}$	C_{ISS}	C_{OSS}
FDN86246	150V	0.9A	1.2Ω	85pF	18pF
IRF5802	150V	1.6A	359mΩ	180pF	28pF

In section III an output capacitance of $10.9pF$ was found ideal. As the voltage waveform across the MOSFET and C_S is given by V_{IN}, f_S and D, the currents (and thereby losses) in L_{IN}, C_S and the MOSFET scales with the value of C_S. It is therefore desirable to keep the value of C_S as close to this as possible in order to achieve high efficiency.

Comparing the two MOSFETs, the FDN86246 has much lower on resistance than the IRF5802. However the output

capacitance is higher and will as mentioned increase the currents and thus reduce the benefit of the low on resistance. Assuming the waveform across the MOSFET is the same using the two MOSFETs, the current using the FDN86246 will be $\frac{C_{FDN86246}-C_{IRF5802}}{C_{IRF5802}} = 142\%$ larger than using the IRF5802. The on resistance will be reduced by $\frac{R_{IRF5820}-R_{FDN86246}}{IRF5802} = 70.1\%$. Combining this gives a total loss reduction of 27.4%, using the estimated loss found in section III this correspond to $9mW$. Furthermore the increased current will also give losses in the input inductor, again using the estimate from section III the increased loss is found to $1.42 \cdot 5.37mW = 7.63mW$. Hence the total loss difference using the two MOSFET is estimated to be less than $2mW$. The increased capacitance will however also make the timing of the switching more important, as a larger amount of energy will be stored in the capacitor and burned in the MOSFET if the switching is just a little wrong.

Based on the analysis above, the MOSFET from IRF are found most suited. But as they are very close, prototypes using both will be made to compare them further.

This next subsections will cover the results obtained with three different power stages. The first power stage is the one which has been designed in the previous sections, the second power stage is with the MOSFET with lower $R_{DS(ON)}$ and the last power stage is with a large input inductor and higher output power, this should, as described in section III, give a higher efficiency.

A. MOSFET with low C_{OSS}

A power stage with the components selected in sections II and III was implemented. Just as the case were when going from calculated values to simulations, slight adjustments had to be made. The tuning procedure was, first to tune the inductor in the output filter to make it resistive at the switching frequency. Once that was done, the inverter was added to the design and a low voltage was applied. It was seen that the converter was not ZVS switching as the output capacitance of the MOSFET was not discharged when it switched on.

In order to get it to discharge faster the values of the input and resonant inductors had to be lowered. First the resonant inductor was lowered to give the desired output power and then the input inductor was adjusted to make the converter ZVS. As the output capacitance of the MOSFET is $20pF$, measuring with a probe with $10pF$ capacitance changes the switching a lot. This ruins the tuning and ZVS is thus not achieved, some waveforms have been measured and they are shown in figure 5. As it is seen the drain voltage has a small break when the MOSFET is switched on, this is due to the $10pF$ added by the probe.

So for the final fine tuning a thermal camera was used to measure the temperature of the MOSFET, it was then assumed that the MOSFET was ZVS when the temperature rise was lowest. Even though this is not a solid proof of ZVS, a low temperature rise comes from low power loss and thus the best tuned circuit. The efficiency was measured to 71.5% (see table IV).
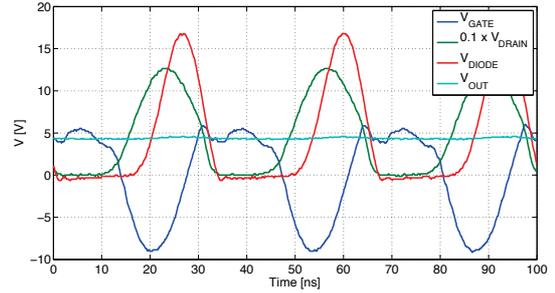

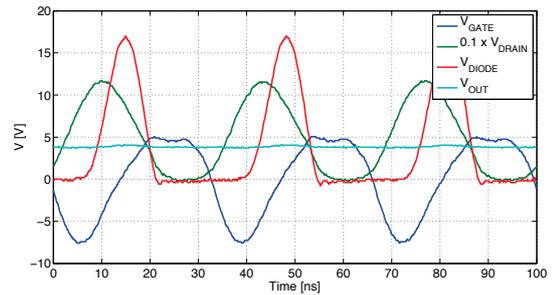Fig. 5. Measurements on the prototype with low C_{OSS}.

Fig. 6. Measurements on the prototype with large input inductor.

B. MOSFET with low R_{ON}

When the MOSFET was selected, the FDN86246 was found to be equally good to the IRF5802. The biggest difference between the two was on resistances and parasitic capacitances. A prototype was implemented using the FDN86246 in a circuit almost identical to the one used for the previous converter. A few turns was removed from the input inductor in order to make the converter ZVS with the increased output capacitance.

Due to the higher output capacitance more energy is stored and if the switch is switched at a few volts instead of zero, much more energy will be burned in the on resistance. Furthermore the AC current in the input inductor is larger which also increases the losses. The total efficiency of the converter was measured to 60.7%.

C. With large input inductor

As explained in section III, the highest efficiency should be achieved with a large input inductor (DC input current). To test this a prototype was made with the IRF5802, but this time with a $6.5\mu H$ input inductor. Then the resonance circuit and the load was adjusted in order to get ZVS and $5V$ output.

The increased output power makes the current through the MOSFET closer to that seen for the ideal class E inverter. Thereby the loss due to slight deviations in the timing of the switching becomes smaller.

The waveforms shown in figure 6 clearly shows that the converter is not ZVS when probes are placed at the gate and drain. Furthermore the voltage drops below $4V$, however removing the probes makes the output voltage increase to $5.0V$.
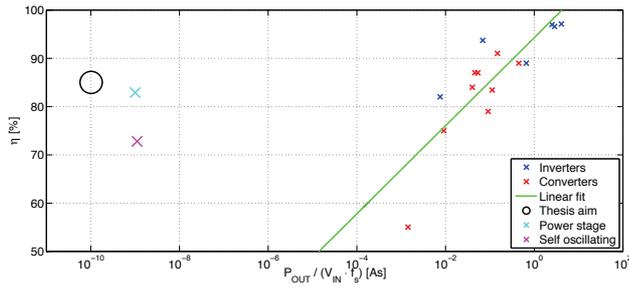
Fig. 7. The achieved $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor and η next to previous results.

When tuned, the output power of the circuit became $1.53W$ and the efficiency was measured to 82.9%. This efficiency is without gate drive, but it is still among the best results achieved by previous researchers. Furthermore the $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor explained in section I is much smaller than for any of the previous converters.

D. Summary of experimental results

The efficiency achieved for the three power stages is shown in table IV. From the three prototypes it is seen that good efficiencies can be achieved just by having ZVS. However the larger the current through the MOSFET is at the switching instant, the more important becomes the timing of the switching and losses increase.

TABLE IV
MEASUREMENTS ON POWER STAGES.

Converter	f_S [MHz]	I_{IN} [mA]	V_{OUT} [V]	R_L [Ω]	η [%]	T_{Mos} [°C]	T_{Dio} [°C]
Low C_{OSS}	30	28	5.00	25	71.5	55.3	52.2
Low R_{ON}	29	32	4.93	25	60.7	65.1	53.2
Large L_{IN}	30	37	5.00	16.3	82.9	46.2	50.5

It has been shown that VHF converters with a very low $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor can be made with high efficiency, the best even had an efficiency of 82.9% which puts it among the best VHF converters. For comparison the results achieved for the power stages are shown i figure 7. The efficiency is not as high as wanted and the factor is a little lower than desired for one of the prototypes due to the higher output power. However seen next to previously achieved results they are very close.

V. CONCLUSION

The theoretical design of the resonant converter was considered in section II and III. Several different topologies were considered and based on complexity and efficiency estimates a class E inverter and rectifier was chosen.

Three different power stages were made; one with a MOSFET with the lowest available output capacitance, one with a MOSFET with low on resistance, and one with increased output power allowing a large input inductor. All the converters had $50V$ input and $5V$ output and the achieved efficiencies were between 60.7% and 82.9%. This shows that it is possible

to make low power very high frequency converters with high step down ratio.

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